Colour Television **Chassis**

Q549.2E
LA

Service
Service
Service

ELITE CORE
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090317

Service Manual

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2009-May-08

PHILIPS

1. Revision List

Manual xxxx xxx xxxx.0

- First release.

Manual xxxx xxx xxxx.1

- **All Chapters:** the following sets to the manual: see Table 2-1 Described Model numbers.
- **Chapter 5:** paragraph 5.8.10 PCI bus added.
- **Chapter 6:** paragraph 6.6 Service SSB delivered without main software loaded added.

2. Technical Specifications and, Connections

Index of this chapter:

2.1 Technical Specifications
2.2 Directions for Use
2.3 Connections
2.4 Chassis Overview

Notes:

- Figures can deviate due to the different set executions.
- Specifications are indicative (subject to change).

2.1 Technical Specifications

For on-line product support please use the links in Table 2-1. Here is product information available, as well as getting started, user manuals, frequently asked questions and software & drivers.

Table 2-1 Described Model numbers

CTN	Styling	Published in:
32PFL9604H/12	Elite Core	3122 785 18310
32PFL9604H/60		3122 785 18310
37PFL9604H/12		3122 785 18310
37PFL9604H/60		3122 785 18311
56PFL9954H/12		3122 785 18311

2.2 Directions for Use

You can download this information from the following websites:
http://www.philips.com/support
http://www.p4c.philips.com

2.3 Connections

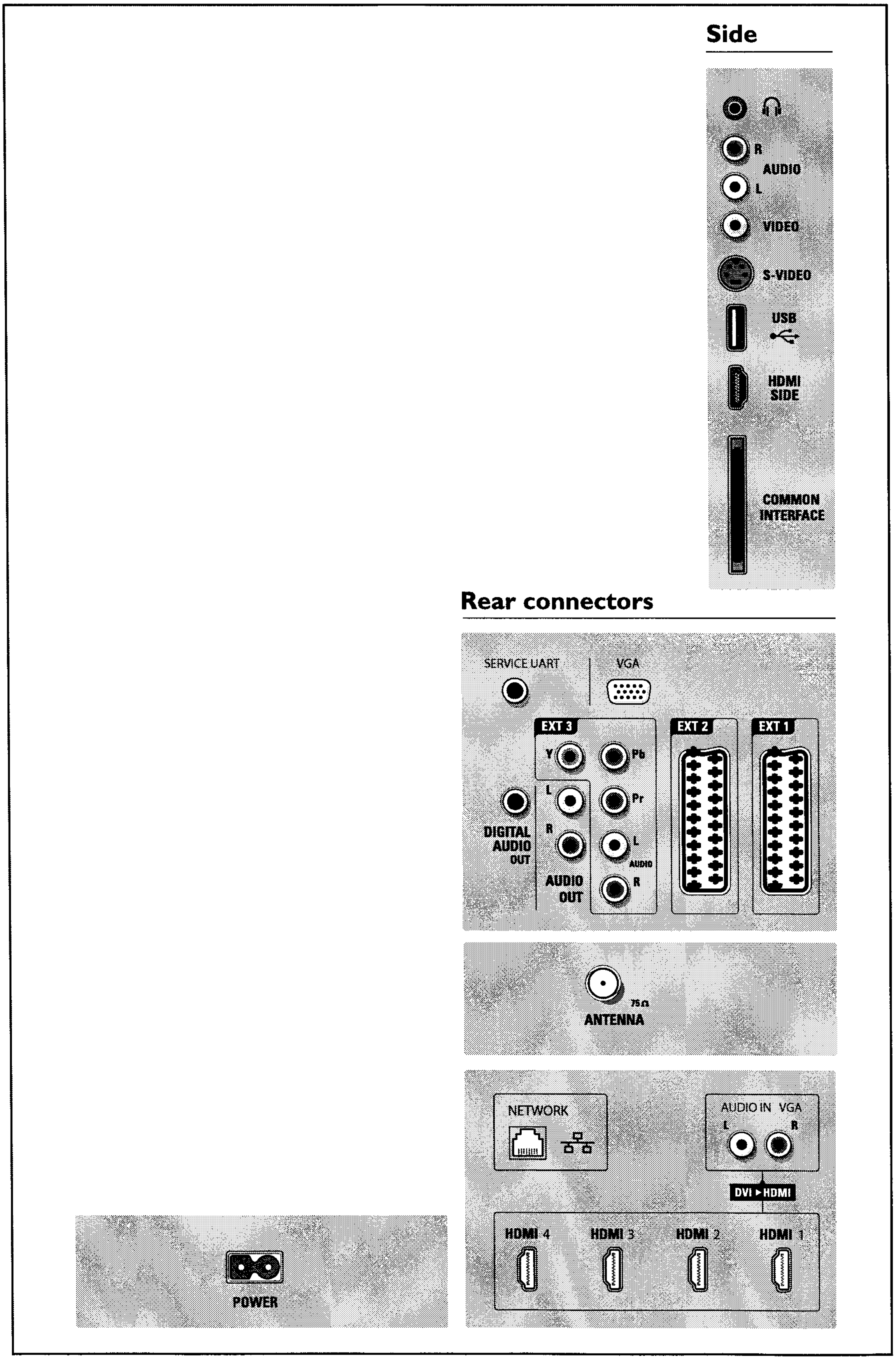
Side
R
AUDIO
L
VIDEO
S-VIDEO
USB
HDMI SIDE
COMMON INTERFACE
Rear connectors
SERVICE UART
VGA
EXT 3
EXT 2
EXT 1
Y
Pb
L
Pr
R
L
AUDIO
R
DIGITAL AUDIO OUT
AUDIO OUT
75Ω
ANTENNA
NETWORK
AUDIO IN VGA
L
R
DVI ▸ HDMI
HDMI 4
HDMI 3
HDMI 2
HDMI 1
POWER

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Figure 2-1 Connection overview

Note: The following connector colour abbreviations are used (acc. to DIN/IEC 757): Bk= Black, Bu= Blue, Gn= Green, Gy= Grey, Rd= Red, Wh= White, Ye= Yellow.

2.3.1 Side Connections

Head phone (Output)

Bk	- Head phone	32 - 600 ohm / 10 mW	◎

Cinch: Video CVBS - In, Audio - In

Rd	- Audio R	0.5 V_{RMS} / 10 kohm	→⊖◎
Wh	- Audio L	0.5 V_{RMS} / 10 kohm	→⊖◎
Ye	- Video CVBS	1 V_{PP} / 75 ohm	→⊖◎

S-Video (Hosiden): Video Y/C - In

1	- Ground Y	Gnd	⏚
2	- Ground C	Gnd	⏚
3	- Video Y	1 V_{PP} / 75 ohm	→⊖
4	- Video C	0.3 V_{PP} / 75 ohm	→⊖

USB2.0

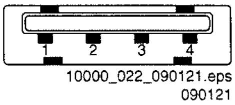


Figure 2-2 USB (type A)

1	- +5V		⊖→
2	- Data (-)		→⊖⊖→
3	- Data (+)		→⊖⊖→
4	- Ground	Gnd	⏚

HDMI: Digital Video, Digital Audio - In (see HDMI 1, 2, 3 & 4 - Rear Connections)

Common Interface

68p - See diagram B07A SSB: CI: PCMCIA Connector →⊖⊖→

2.3.2 Rear Connections

Service Connector (UART)

1	- Ground	Gnd	⏚
2	- UART_TX	Transmit	⊖→
3	- UART_RX	Receive	→⊖

VGA: Video RGB - In

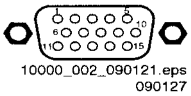


Figure 2-3 VGA Connector

1	- Video Red	0.7 V_{PP} / 75 ohm	→⊖
2	- Video Green	0.7 V_{PP} / 75 ohm	→⊖
3	- Video Blue	0.7 V_{PP} / 75 ohm	→⊖
4	- n.c.		
5	- Ground	Gnd	⏚
6	- Ground Red	Gnd	⏚
7	- Ground Green	Gnd	⏚
8	- Ground Blue	Gnd	⏚
9	- +5V_{DC}	+5 V	→⊖
10	- Ground Sync	Gnd	⏚
11	- n.c.		
12	- DDC_SDA	DDC data	→⊖
13	- H-sync	0 - 5 V	→⊖
14	- V-sync	0 - 5 V	→⊖
15	- DDC_SCL	DDC clock	→⊖

Cinch: S/PDIF - Out

Bk	- Coaxial	0.4 - 0.6V_{PP} / 75 ohm	⊖→◎

Cinch: Audio - Out

Rd	- Audio - R	0.5 V_{RMS} / 10 kohm	⊖→◎
Wh	- Audio - L	0.5 V_{RMS} / 10 kohm	⊖→◎

EXT3: Cinch: Video YPbPr - In, Audio - In

Gn	- Video Y	1 V_{PP} / 75 ohm	→⊖◎
Bu	- Video Pb	0.7 V_{PP} / 75 ohm	→⊖◎
Rd	- Video Pr	0.7 V_{PP} / 75 ohm	→⊖◎
Rd	- Audio - R	0.5 V_{RMS} / 10 kohm	→⊖◎
Wh	- Audio - L	0.5 V_{RMS} / 10 kohm	→⊖◎

EXT1 & 2: Video RGB - In, CVBS - In/Out, Audio - In/Out

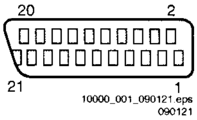


Figure 2-4 SCART connector

1	- Audio R	0.5 V_{RMS} / 1 kohm	⊖→
2	- Audio R	0.5 V_{RMS} / 10 kohm	→⊖
3	- Audio L	0.5 V_{RMS} / 1 kohm	⊖→
4	- Ground Audio	Gnd	⏚
5	- Ground Blue	Gnd	⏚
6	- Audio L	0.5 V_{RMS} / 10 kohm	→⊖
7	- Video Blue	0.7 V_{PP} / 75 ohm	→⊖⊖→
8	- Function Select	0 - 2 V: INT 4.5 - 7 V: EXT 16:9 9.5 - 12 V: EXT 4:3	→⊖
9	- Ground Green	Gnd	⏚
10	- n.c.		
11	- Video Green	0.7 V_{PP} / 75 ohm	→⊖
12	- n.c.		
13	- Ground Red	Gnd	⏚
14	- Ground P50	Gnd	⏚
15	- Video Red	0.7 V_{PP} / 75 ohm	→⊖
16	- Status/FBL	0 - 0.4 V: INT 1 - 3 V: EXT / 75 ohm	→⊖
17	- Ground Video	Gnd	⏚
18	- Ground FBL	Gnd	⏚
19	- Video CVBS/Y	1 V_{PP} / 75 ohm	⊖→
20	- Video CVBS	1 V_{PP} / 75 ohm	→⊖
21	- Shield	Gnd	⏚

Aerial - In

-	- IEC-type (EU)	Coax, 75 ohm	⫟

RJ45: Ethernet (if present)

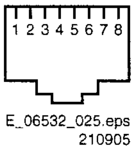


Figure 2-5 Ethernet connector

1	- TD+	Transmit signal	⊖→
2	- TD-	Transmit signal	⊖→
3	- RD+	Receive signal	→⊖
4	- CT	Centre Tap: DC level fixation	
5	- CT	Centre Tap: DC level fixation	
6	- RD-	Receive signal	→⊖
7	- GND	Gnd	⏚
8	- GND	Gnd	⏚

Cinch: Audio - In (VGA/DVI)

Rd	- Audio R	0.5 V_{RMS} / 10 kohm	→◎
Wh	- Audio L	0.5 V_{RMS} / 10 kohm	→◎

HDMI 1, 2, 3 & 4: Digital Video, Digital Audio - In

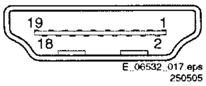


Figure 2-6 HDMI (type A) connector

1	- D2+	Data channel	→
2	- Shield	Gnd	⏚
3	- D2-	Data channel	→
4	- D1+	Data channel	→
5	- Shield	Gnd	⏚
6	- D1-	Data channel	→
7	- D0+	Data channel	→
8	- Shield	Gnd	⏚
9	- D0-	Data channel	→
10	- CLK+	Data channel	→
11	- Shield	Gnd	⏚
12	- CLK-	Data channel	→
13	- Easylink/CEC	Control channel	⇄
14	- n.c.		
15	- DDC_SCL	DDC clock	→
16	- DDC_SDA	DDC data	⇄
17	- Ground	Gnd	⏚
18	- +5V		→
19	- HPD	Hot Plug Detect	→
20	- Ground	Gnd	⏚

2.4 Chassis Overview

Refer to chapter Block Diagrams for PWB/CBA locations.

3. Precautions, Notes, and Abbreviation List

Index of this chapter:

3.1 Safety Instructions
3.2 Warnings
3.3 Notes
3.4 Abbreviation List

3.1 Safety Instructions

Safety regulations require the following **during** a repair:

- Connect the set to the Mains/AC Power via an isolation transformer (> 800 VA).
- Replace safety components, indicated by the symbol ⚠, only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard. Of de set ontploft!

Safety regulations require that **after** a repair, the set must be returned in its original condition. Pay in particular attention to the following points:

- Route the wire trees correctly and fix them with the mounted cable clamps.
- Check the insulation of the Mains/AC Power lead for external damage.
- Check the strain relief of the Mains/AC Power cord for proper function.
- Check the electrical DC resistance between the Mains/AC Power plug and the secondary side (only for sets that have a Mains/AC Power isolated power supply):
  1. Unplug the Mains/AC Power cord and connect a wire between the two pins of the Mains/AC Power plug.
  2. Set the Mains/AC Power switch to the "on" position (keep the Mains/AC Power cord unplugged!).
  3. Measure the resistance value between the pins of the Mains/AC Power plug and the metal shielding of the tuner or the aerial connection on the set. The reading should be between 4.5 MΩ and 12 MΩ.
  4. Switch "off" the set, and remove the wire between the two pins of the Mains/AC Power plug.
- Check the cabinet for defects, to prevent touching of any inner parts by the customer.

3.2 Warnings

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD ⚠). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are connected with the same potential as the mass of the set by a wristband with resistance. Keep components and tools also at this same potential.
- Be careful during measurements in the high voltage section.
- Never replace modules or other components while the unit is switched "on".
- When you align the set, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

3.3 Notes

3.3.1 General

- Measure the voltages and waveforms with regard to the chassis (= tuner) ground (⏚), or hot ground (⏚), depending on the tested area of circuitry. The voltages and waveforms shown in the diagrams are indicative. Measure them in the Service Default Mode with a colour bar signal and stereo sound (L: 3 kHz, R: 1 kHz unless stated otherwise) and picture carrier at 475.25 MHz for PAL, or 61.25 MHz for NTSC (channel 3).
- Where necessary, measure the waveforms and voltages with (⊓⊓) and without (⊗) aerial signal. Measure the voltages in the power supply section both in normal operation (①) and in stand-by (⏻). These values are indicated by means of the appropriate symbols.

3.3.2 Schematic Notes

- All resistor values are in ohms, and the value multiplier is often used to indicate the decimal point location (e.g. 2K2 indicates 2.2 kΩ).
- Resistor values with no multiplier may be indicated with either an "E" or an "R" (e.g. 220E or 220R indicates 220 Ω).
- All capacitor values are given in micro-farads ($\mu = \times 10^{-6}$), nano-farads ($n = \times 10^{-9}$), or pico-farads ($p = \times 10^{-12}$).
- Capacitor values may also use the value multiplier as the decimal point indication (e.g. 2p2 indicates 2.2 pF).
- An "asterisk" (*) indicates component usage varies. Refer to the diversity tables for the correct values.
- The correct component values are listed on the Philips Spare Parts Web Portal.

3.3.3 Spare Parts

For the latest spare part overview, consult your Philips Spare Part web portal.

3.3.4 BGA (Ball Grid Array) ICs

Introduction

For more information on how to handle BGA devices, visit this URL: http://www.atyourservice-magazine.com. Select "Magazine", then go to "Repair downloads". Here you will find Information on how to deal with BGA-ICs.

BGA Temperature Profiles

For BGA-ICs, you **must** use the correct temperature-profile. Where applicable and available, this profile is added to the IC Data Sheet information section in this manual.

3.3.5 Lead-free Soldering

Due to lead-free technology some rules have to be respected by the workshop during a repair:

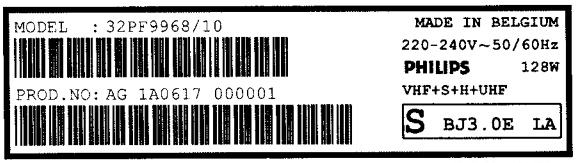
- Use only lead-free soldering tin. If lead-free solder paste is required, please contact the manufacturer of your soldering equipment. In general, use of solder paste within workshops should be avoided because paste is not easy to store and to handle.
- Use only adequate solder tools applicable for lead-free soldering tin. The solder tool must be able:
  - To reach a solder-tip temperature of at least 400°C.
  - To stabilize the adjusted temperature at the solder-tip.
  - To exchange solder-tips for different applications.
- Adjust your solder tool so that a temperature of around 360°C - 380°C is reached and stabilized at the solder joint. Heating time of the solder-joint should not exceed ~ 4 sec. Avoid temperatures above 400°C, otherwise wear-out of tips will increase drastically and flux-fluid will be destroyed. To avoid wear-out of tips, switch "off" unused equipment or reduce heat.
- Mix of lead-free soldering tin/parts with leaded soldering tin/parts is possible but PHILIPS recommends strongly **to avoid** mixed regimes. If this cannot be avoided, carefully clear the solder-joint from old tin and re-solder with new tin.

3.3.6 Alternative BOM identification

It should be noted that on the European Service website, “Alternative BOM” is referred to as “Design variant”.

The **third digit** in the serial number (example: AG**2**B0335000001) indicates the number of the alternative B.O.M. (Bill Of Materials) that has been used for producing the specific TV set. In general, it is possible that the same TV model on the market is produced with e.g. two different types of displays, coming from two different suppliers. This will then result in sets which have the same CTN (Commercial Type Number; e.g. 28PW9515/12) but which have a different B.O.M. number.
By looking at the third digit of the serial number, one can identify which B.O.M. is used for the TV set he is working with.
If the third digit of the serial number contains the number “1” (example: AG**1**B033500001), then the TV set has been manufactured according to B.O.M. number 1. If the third digit is a “2” (example: AG**2**B0335000001), then the set has been produced according to B.O.M. no. 2. This is important for ordering the correct spare parts!
For the third digit, the numbers 1...9 and the characters A...Z can be used, so in total: 9 plus 26= 35 different B.O.M.s can be indicated by the third digit of the serial number.

Identification: The bottom line of a type plate gives a 14-digit serial number. Digits 1 and 2 refer to the production centre (e.g. AG is Bruges), digit 3 refers to the B.O.M. code, digit 4 refers to the Service version change code, digits 5 and 6 refer to the production year, and digits 7 and 8 refer to production week (in example below it is 2006 week 17). The 6 last digits contain the serial number.



MODEL : 32PF9968/10
MADE IN BELGIUM
220-240V~50/60Hz
PHILIPS 128W
PROD.NO: AG 1A0617 000001
VHF+S+H+UHF
S BJ3.0E LA

10000_024_090121.eps
090121

Figure 3-1 Serial number (example)

3.3.7 Board Level Repair (BLR) or Component Level Repair (CLR)

If a board is defective, consult your repair procedure to decide if the board has to be exchanged or if it should be repaired on component level.
If your repair procedure says the board should be exchanged completely, do not solder on the defective board. Otherwise, it cannot be returned to the O.E.M. supplier for back charging!

3.3.8 Practical Service Precautions

- **It makes sense to avoid exposure to electrical shock.** While some sources are expected to have a possible dangerous impact, others of quite high potential are of limited current and are sometimes held in less regard.
- **Always respect voltages.** While some may not be dangerous in themselves, they can cause unexpected reactions that are best avoided. Before reaching into a powered TV set, it is best to test the high voltage insulation. It is easy to do, and is a good service precaution.

3.4 Abbreviation List

0/6/12	SCART switch control signal on A/V board. 0 = loop through (AUX to TV), 6 = play 16 : 9 format, 12 = play 4 : 3 format
AARA	Automatic Aspect Ratio Adaptation: algorithm that adapts aspect ratio to remove horizontal black bars; keeps the original aspect ratio
ACI	Automatic Channel Installation: algorithm that installs TV channels directly from a cable network by means of a predefined TXT page
ADC	Analogue to Digital Converter
AFC	Automatic Frequency Control: control signal used to tune to the correct frequency
AGC	Automatic Gain Control: algorithm that controls the video input of the feature box
AM	Amplitude Modulation
AP	Asia Pacific
AR	Aspect Ratio: 4 by 3 or 16 by 9
ASF	Auto Screen Fit: algorithm that adapts aspect ratio to remove horizontal black bars without discarding video information
ATSC	Advanced Television Systems Committee, the digital TV standard in the USA
ATV	See Auto TV
Auto TV	A hardware and software control system that measures picture content, and adapts image parameters in a dynamic way
AV	External Audio Video
AVC	Audio Video Controller
AVIP	Audio Video Input Processor
B/G	Monochrome TV system. Sound carrier distance is 5.5 MHz
BLR	Board-Level Repair
BTSC	Broadcast Television Standard Committee. Multiplex FM stereo sound system, originating from the USA and used e.g. in LATAM and AP-NTSC countries
B-TXT	Blue TeleteXT
C	Centre channel (audio)
CEC	Consumer Electronics Control bus: remote control bus on HDMI connections
CL	Constant Level: audio output to connect with an external amplifier
CLR	Component Level Repair
ComPair	Computer aided rePair
CP	Connected Planet / Copy Protection
CSM	Customer Service Mode
CTI	Color Transient Improvement: manipulates steepness of chroma transients
CVBS	Composite Video Blanking and Synchronization
DAC	Digital to Analogue Converter
DBE	Dynamic Bass Enhancement: extra low frequency amplification
DDC	See “E-DDC”
D/K	Monochrome TV system. Sound carrier distance is 6.5 MHz
DFI	Dynamic Frame Insertion
DFU	Directions For Use: owner's manual
DMR	Digital Media Reader: card reader
DMSD	Digital Multi Standard Decoding
DNM	Digital Natural Motion

DNR	Digital Noise Reduction: noise reduction feature of the set
DRAM	Dynamic RAM
DRM	Digital Rights Management
DSP	Digital Signal Processing
DST	Dealer Service Tool: special remote control designed for service technicians
DTCP	Digital Transmission Content Protection; A protocol for protecting digital audio/video content that is traversing a high speed serial bus, such as IEEE-1394
DVB-C	Digital Video Broadcast - Cable
DVB-T	Digital Video Broadcast - Terrestrial
DVD	Digital Versatile Disc
DVI(-d)	Digital Visual Interface (d= digital only)
E-DDC	Enhanced Display Data Channel (VESA standard for communication channel and display). Using E-DDC, the video source can read the EDID information form the display.
EDID	Extended Display Identification Data (VESA standard)
EEPROM	Electrically Erasable and Programmable Read Only Memory
EMI	Electro Magnetic Interference
EPLD	Erasable Programmable Logic Device
EU	Europe
EXT	EXTernal (source), entering the set by SCART or by cinches (jacks)
FDS	Full Dual Screen (same as FDW)
FDW	Full Dual Window (same as FDS)
FLASH	FLASH memory
FM	Field Memory or Frequency Modulation
FPGA	Field-Programmable Gate Array
FTV	Flat TeleVision
Gb/s	Giga bits per second
G-TXT	Green TeleteXT
H	H_sync to the module
HD	High Definition
HDD	Hard Disk Drive
HDCP	High-bandwidth Digital Content Protection: A “key” encoded into the HDMI/DVI signal that prevents video data piracy. If a source is HDCP coded and connected via HDMI/DVI without the proper HDCP decoding, the picture is put into a “snow vision” mode or changed to a low resolution. For normal content distribution the source and the display device must be enabled for HDCP “software key” decoding.
HDMI	High Definition Multimedia Interface
HP	HeadPhone
I	Monochrome TV system. Sound carrier distance is 6.0 MHz
I^2C	Inter IC bus
I^2D	Inter IC Data bus
I^2S	Inter IC Sound bus
IF	Intermediate Frequency
IR	Infra Red
IRQ	Interrupt Request
ITU-656	The ITU Radio communication Sector (ITU-R) is a standards body subcommittee of the International Telecommunication Union relating to radio communication. ITU-656 (a.k.a. SDI), is a digitized video format used for broadcast grade video. Uncompressed digital component or digital composite signals can be used. The SDI signal is self-synchronizing, uses 8 bit or 10 bit data words, and has a maximum data rate of 270 Mbit/s, with a minimum bandwidth of 135 MHz.
ITV	Institutional TeleVision; TV sets for hotels, hospitals etc.
LS	Last Status; The settings last chosen by the customer and read and stored in RAM or in the NVM. They are called at start-up of the set to configure it according to the customer's preferences
LATAM	Latin America
LCD	Liquid Crystal Display
LED	Light Emitting Diode
L/L'	Monochrome TV system. Sound carrier distance is 6.5 MHz. L' is Band I, L is all bands except for Band I
LPL	LG.Philips LCD (supplier)
LS	Loudspeaker
LVDS	Low Voltage Differential Signalling
Mbps	Mega bits per second
M/N	Monochrome TV system. Sound carrier distance is 4.5 MHz
MIPS	Microprocessor without Interlocked Pipeline-Stages; A RISC-based microprocessor
MOP	Matrix Output Processor
MOSFET	Metal Oxide Silicon Field Effect Transistor, switching device
MPEG	Motion Pictures Experts Group
MPIF	Multi Platform InterFace
MUTE	MUTE Line
NC	Not Connected
NICAM	Near Instantaneous Compounded Audio Multiplexing. This is a digital sound system, mainly used in Europe.
NTC	Negative Temperature Coefficient, non-linear resistor
NTSC	National Television Standard Committee. Color system mainly used in North America and Japan. Color carrier NTSC M/N= 3.579545 MHz, NTSC 4.43= 4.433619 MHz (this is a VCR norm, it is not transmitted off-air)
NVM	Non-Volatile Memory: IC containing TV related data such as alignments
O/C	Open Circuit
OSD	On Screen Display
OTC	On screen display Teletext and Control; also called Artistic (SAA5800)
P50	Project 50: communication protocol between TV and peripherals
PAL	Phase Alternating Line. Color system mainly used in West Europe (color carrier= 4.433619 MHz) and South America (color carrier PAL M= 3.575612 MHz and PAL N= 3.582056 MHz)
PCB	Printed Circuit Board (same as “PWB”)
PCM	Pulse Code Modulation
PDP	Plasma Display Panel
PFC	Power Factor Corrector (or Pre-conditioner)
PIP	Picture In Picture
PLL	Phase Locked Loop. Used for e.g. FST tuning systems. The customer can give directly the desired frequency
POD	Point Of Deployment: a removable CAM module, implementing the CA system for a host (e.g. a TV-set)
POR	Power On Reset, signal to reset the uP
PTC	Positive Temperature Coefficient, non-linear resistor
PWB	Printed Wiring Board (same as “PCB”)

PWM	Pulse Width Modulation
QRC	Quasi Resonant Converter
QTNR	Quality Temporal Noise Reduction
QVCP	Quality Video Composition Processor
RAM	Random Access Memory
RGB	Red, Green, and Blue. The primary color signals for TV. By mixing levels of R, G, and B, all colors (Y/C) are reproduced.
RC	Remote Control
RC5 / RC6	Signal protocol from the remote control receiver
RESET	RESET signal
ROM	Read Only Memory
RSDS	Reduced Swing Differential Signalling data interface
R-TXT	Red TeleteXT
SAM	Service Alignment Mode
S/C	Short Circuit
SCART	Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs
SCL	Serial Clock I^2C
SCL-F	CLock Signal on Fast I^2C bus
SD	Standard Definition
SDA	Serial Data I^2C
SDA-F	DAta Signal on Fast I^2C bus
SDI	Serial Digital Interface, see "ITU-656"
SDRAM	Synchronous DRAM
SECAM	SEequence Couleur Avec Mémoire. Color system mainly used in France and East Europe. Color carriers= 4.406250 MHz and 4.250000 MHz
SIF	Sound Intermediate Frequency
SMPS	Switched Mode Power Supply
SoC	System on Chip
SOG	Sync On Green
SOPS	Self Oscillating Power Supply
SPI	Serial Peripheral Interface bus; a 4-wire synchronous serial data link standard
S/PDIF	Sony Philips Digital InterFace
SRAM	Static RAM
SRP	Service Reference Protocol
SSB	Small Signal Board
STBY	STand-BY
SVGA	800 x 600 (4:3)
SVHS	Super Video Home System
SW	Software
SWAN	Spatial temporal Weighted Averaging Noise reduction
SXGA	1280 x 1024
TFT	Thin Film Transistor
THD	Total Harmonic Distortion
TMDS	Transmission Minimized Differential Signalling
TXT	TeleteXT
TXT-DW	Dual Window with TeleteXT
UI	User Interface
uP	Microprocessor
UXGA	1600 x 1200 (4:3)
V	V-sync to the module
VESA	Video Electronics Standards Association
VGA	640 x 480 (4:3)
VL	Variable Level out: processed audio output toward external amplifier
VSB	Vestigial Side Band; modulation method
WYSIWYR	What You See Is What You Record: record selection that follows main picture and sound
WXGA	1280 x 768 (15:9)
XTAL	Quartz crystal
XGA	1024 x 768 (4:3)
Y	Luminance signal
Y/C	Luminance (Y) and Chrominance (C) signal
YPbPr	Component video. Luminance and scaled color difference signals (B-Y and R-Y)
YUV	Component video

4. Mechanical Instructions

Index of this chapter:

4.1 Cable Dressing and Taping
4.2 Service Positions
4.3 Assy/Panel Removal
4.4 Set Re-assembly

Notes:

- Figures below can deviate slightly from the actual situation, due to the different set executions.

4.1 Cable Dressing and Taping

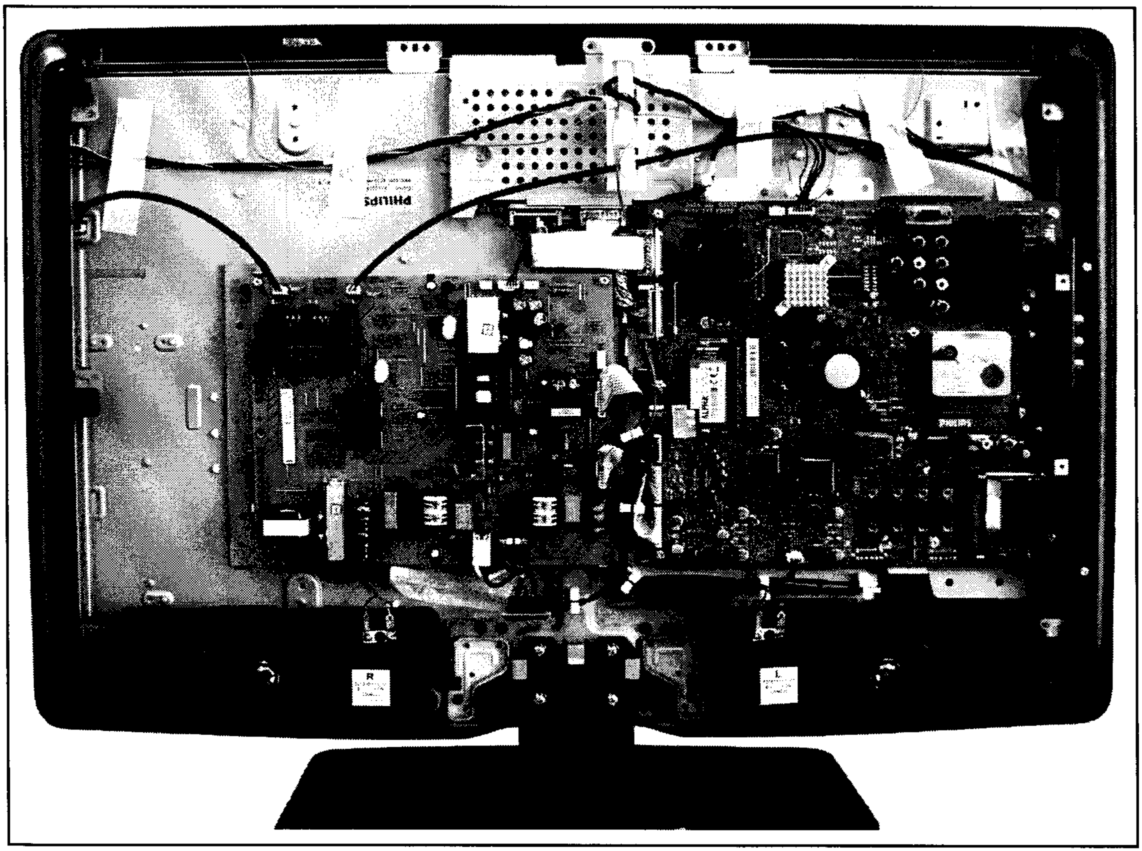


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Figure 4-1 Cable dressing 32”

4. Mechanical Instructions

Index of this chapter:

4.1 Cable Dressing and Taping
4.2 Service Positions
4.3 Assy/Panel Removal
4.4 Set Re-assembly

Notes:

- Figures below can deviate slightly from the actual situation, due to the different set executions.

4.1 Cable Dressing and Taping

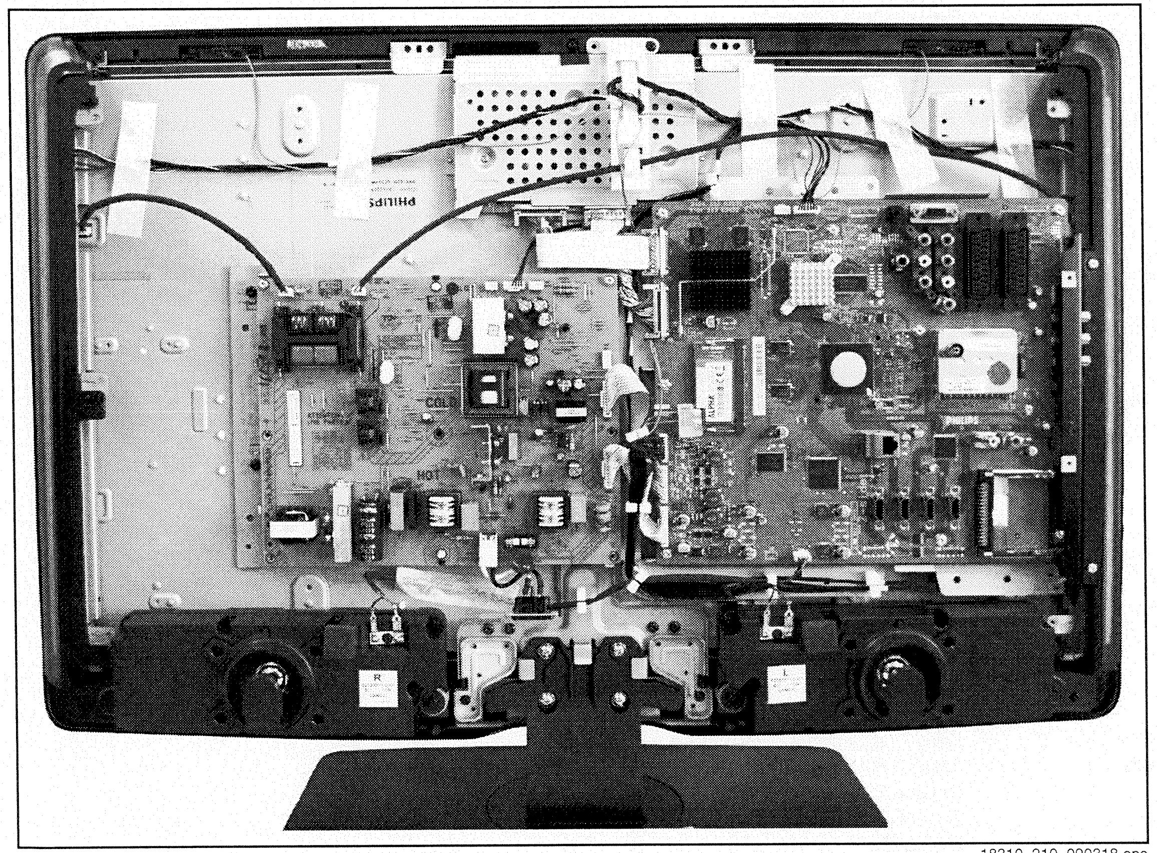

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Figure 4-1 Cable dressing 32"

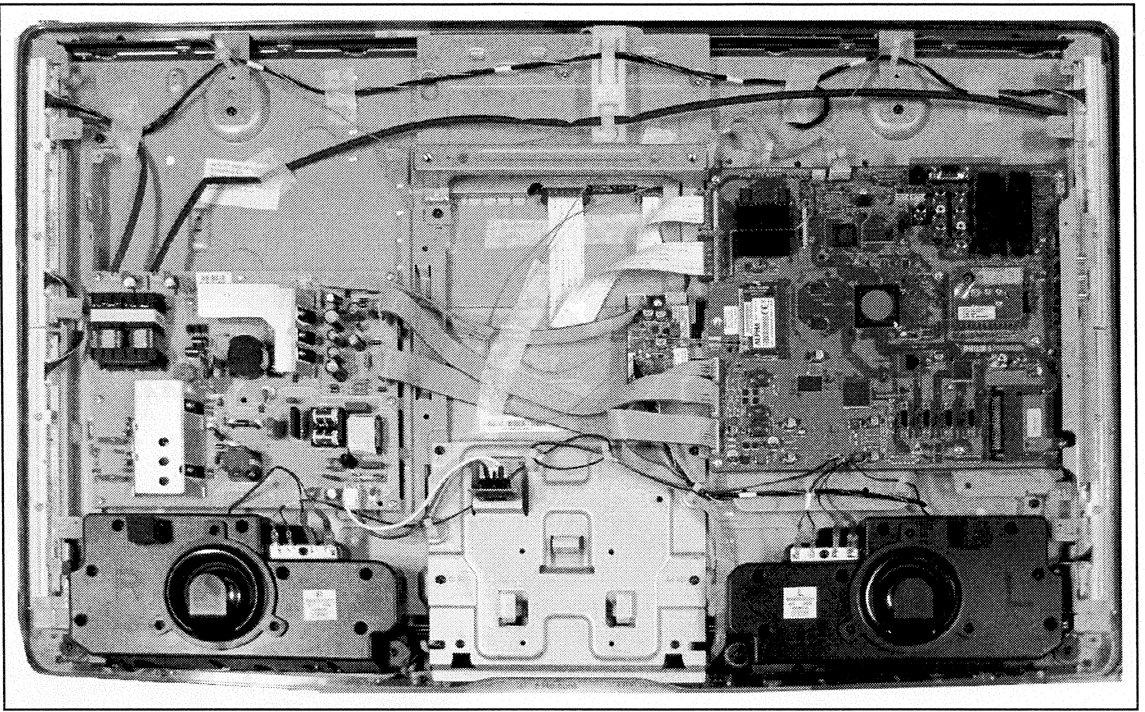

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Figure 4-2 Cable dressing 37"

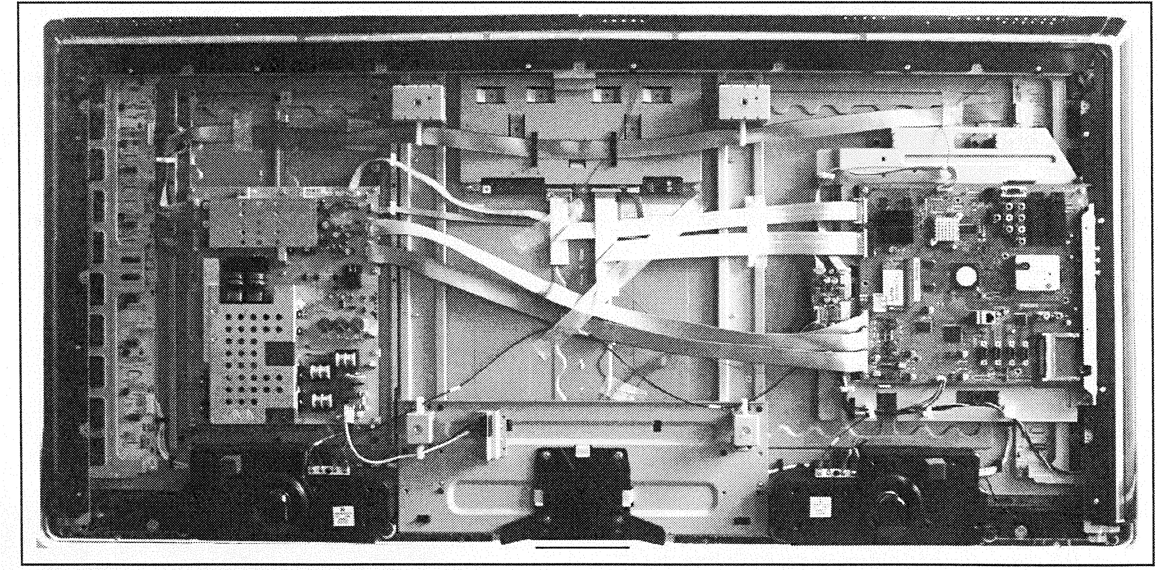

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Figure 4-3 Cable dressing 56" (21:9)

4.2 Service Positions

For easy servicing of this set, there are a few possibilities created:

- The buffers from the packaging.
- Foam bars (created for Service).

4.2.1 Foam Bars

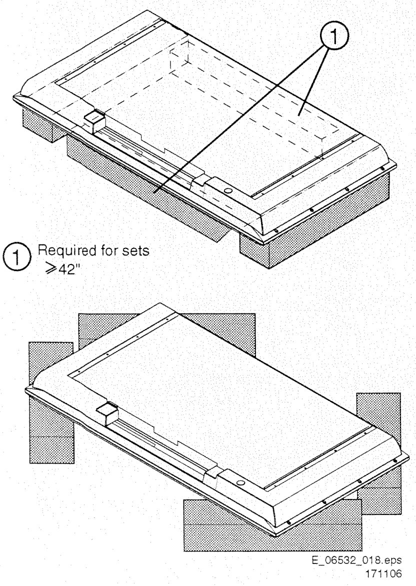

Figure 4-4 Foam bars

The foam bars (order code 3122 785 90580 for two pieces) can be used for all types and sizes of Flat TVs.
See Figure 4-4 for details. Sets with a display of 42" and larger, require **four** foam bars [1]. Ensure that the foam bars are always supporting the cabinet and **never** only the display.
Caution: Failure to follow these guidelines can seriously damage the display!
By laying the TV face down on the (ESD protective) foam bars, a stable situation is created to perform measurements and alignments. By placing a mirror under the TV, you can monitor the screen.

4.3 Assy/Panel Removal

4.3.1 Rear Cover

Warning: Disconnect the mains power cord before you remove the rear cover.
Note: it is **not** necessary to remove the stand while removing the rear cover.

Removing the Piezo Touch Control Panel PWB requires special attention. Refer to *Piezo Touch Control Panel* ***for details.***

1. Remove all screws of the rear cover.
2. Lift the rear cover from the TV. Make sure that wires and flat coils are not damaged while lifting the rear cover from the set.

4.3.2 Speakers

Each speaker unit is mounted with two screws. A sticker on the the unit indicates if it is the right ("R") or left ("L") box, seen from the front side of the set.
When defective, replace the whole unit.

4.3.3 Ambi Light

Each Ambi Light unit is mounted on a subframe. Refer to Figure 4-5 for details.

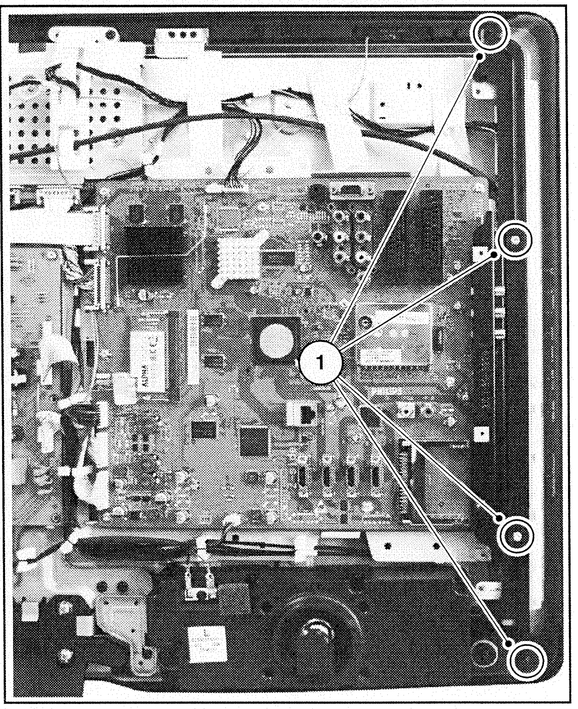

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Figure 4-5 Ambi Light unit

1. Remove the Ambi Light cover [1].
2. Unplug the connector(s).
3. The PWB can now be taken from the subframe.

When defective, replace the whole unit.
Note: the screws that secure the AmbiLight units are longer than the other screws.

4.3.4 Main Supply Panel

1. Unplug all connectors.
2. Remove the fixation screws.
3. Take the board out.

When defective, replace the whole unit.

4.3.5 IR & LED Board

Refer to Figure 4-6 for details.

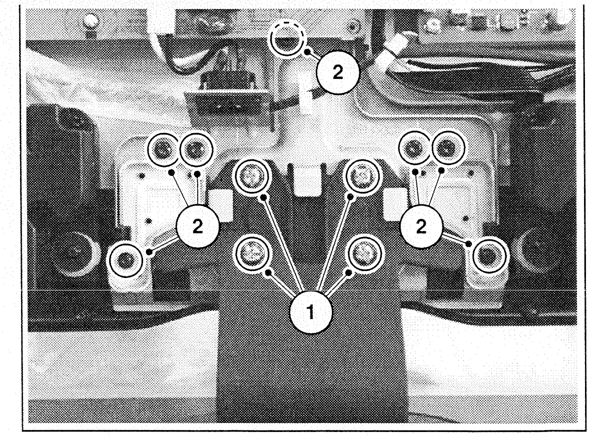

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Figure 4-6 IR & LED Board

1. Remove the Main Supply Panel as earlier described.
2. Remove the stand [1] and its subframe [2].
3. Now you gain access the IR & LED board.

When defective, replace the whole unit.

4.3.6 Piezo Touch Control Panel

The flexfoil between Piezo Flexfoil Assy (mounted on the plastic rim of the set), and the PWB as described below, is extremely vulnerable. Do not pull hard at the PWB or flexfoil.
Once the flexfoil has been damaged, the entire plastic rim of the set (with the touch-control pads) has to be swapped!

The Piezo Touch Control Panel PWB contains ESD sensitive components, implying that necessary industrial ESD precautions must be taken during removing or remounting. Refer to Figure 4-7, Figure 4-8 and Figure 4-9 for details.

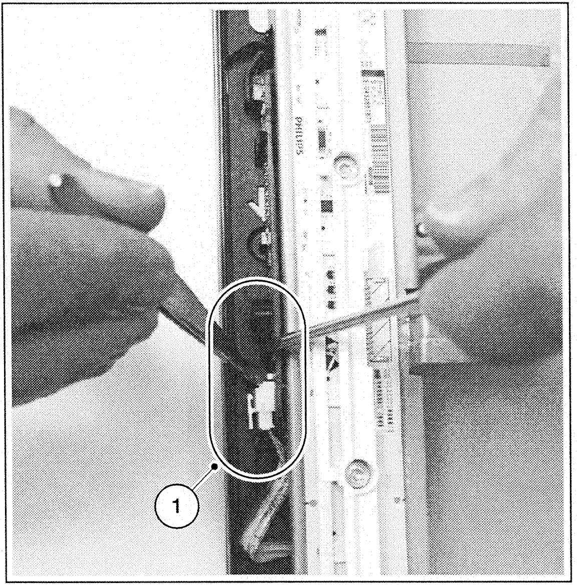

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Figure 4-7 Piezo Touch Control Panel -1-

1. Gently pull the bottom side of the PWB out of the cabinet until you can unplug the connector [1].

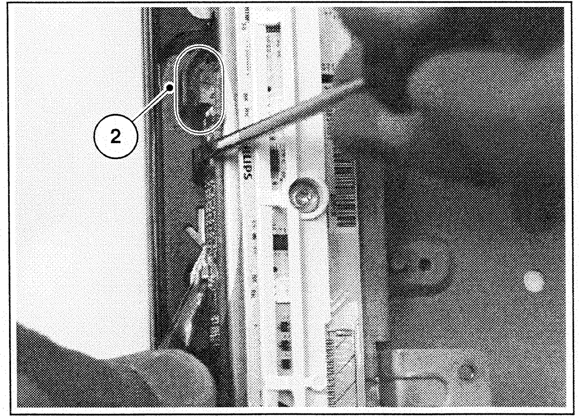

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Figure 4-8 Piezo Touch Control Panel -2-

1. Now gently pull the top side of the PWB out of the cabinet **without damaging the flexfoil** until you can unplug the connector [2].

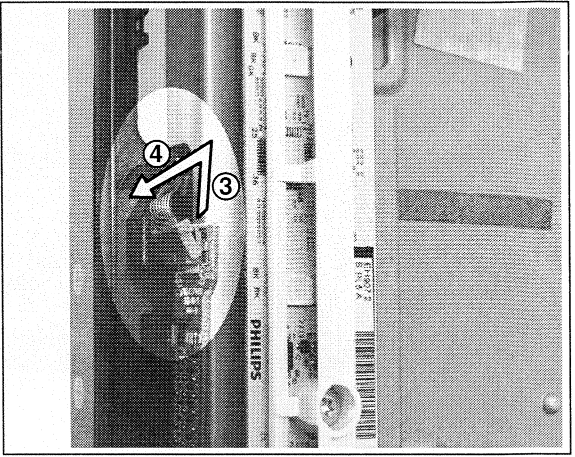

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Figure 4-9 Piezo Touch Control Panel -3-

1. To unplug the flexfoil connector, first the outer part of the connector has to be moved upwards [3], before this part can be turned sidewards [4] as shown in the picture. Now the flexfoil can be removed from the connector and the PWB can be taken out of the set.

When defective, replace the whole unit.

4.3.7 Small Signal Board (SSB)

Caution: It is mandatory to remount screws at their original position during re-assembly. Failure to do so may result in damaging the SSB.

1. Remove the Wi-Fi module that is mounted on the SSB.
2. Unplug all connectors.
3. Remove the screws that secure the board.
4. The SSB can now be taken out of the set.

4.3.8 LCD Panel

Refer to Figure 4-10 and Figure 4-11 for details.

1. Remove the Piezo Touch Control Panel PWB as earlier described.
2. Remove the AL covers as earlier described.
3. Remove both Main Supply Panel and SSB as earlier described.
4. Remove the subframes of Main Power Supply and SSB [1].
5. Remove both AL subframes (with the AL unit still mounted on it) by unplugging the connector [2] and removing the screws [3].
6. Remove all remaining adhesive tapes and remove all cables from their clamps.
7. Carefully remove the conducting tape [4], it must be re-used during re-assembly!
8. Remove the remaining screws (indicated with an arrow) that hold the plastic rim and remove the rim.
9. Now the LCD Panel can be lifted from the front cabinet. **The panel has to be slided downwards** once it has been lifted, because the brackets on the top cannot be removed from the cabinet. You will see a conducting foam between metal front and panel, near the location of the Piezo Touch Control Panel.

When mounting a new LCD Panel:

1. Check if this conducting foam between panel and metal front is in place !
2. Re-attach the conducting tape between LCD Panel and metal rim [4] !

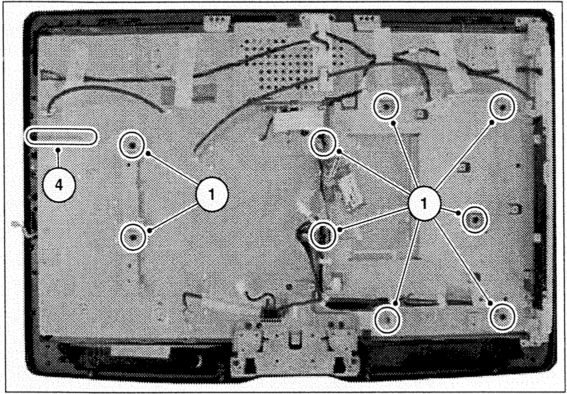

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Figure 4-10 LCD Panel -1-

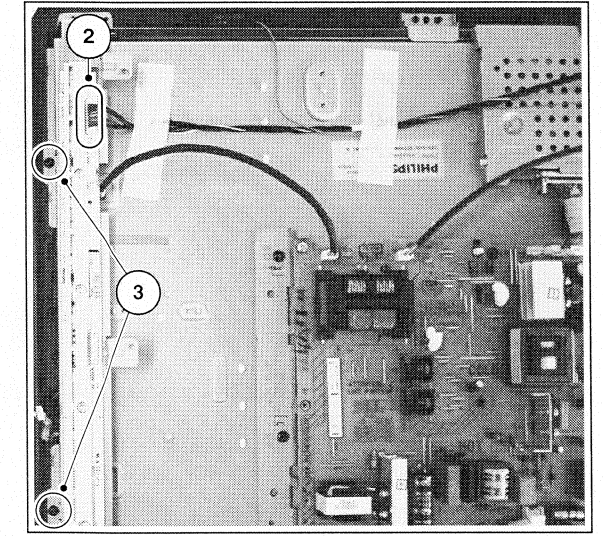

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Figure 4-11 LCD Panel -2-

4.3.9 Wi-Fi antenna

Follow the instructions for LCD Panel until “remove plastic rim”. After removal of this rim, you gain access to the Wi-Fi antennas.

4.4 Set Re-assembly

To re-assemble the whole set, execute all processes in reverse order.

Notes:

- While re-assembling, make sure that all cables are placed and connected in their original position.
- Pay special attention not to damage the EMC foams in the set. Ensure that EMC foams are mounted correctly.

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

5.1 Test Points
5.2 Service Modes
5.3 Stepwise Start-up
5.4 Service Tools
5.5 Error Codes
5.6 The Blinking LED Procedure
5.7 Protections
5.8 Fault Finding and Repair Tips
5.9 Software Upgrading

5.1 Test Points

As most signals are digital, it will be difficult to measure waveforms with a standard oscilloscope. However, several key ICs are capable of generating test patterns, which can be controlled via ComPair. In this way it is possible to determine which part is defective.

Perform measurements under the following conditions:
- Service Default Mode.
- Video: Colour bar signal.
- Audio: 3 kHz left, 1 kHz right.

5.2 Service Modes

Service Default mode (SDM) and Service Alignment Mode (SAM) offers several features for the service technician, while the Customer Service Mode (CSM) is used for communication between the call centre and the customer.

This chassis also offers the option of using ComPair, a hardware interface between a computer and the TV chassis. It offers the abilities of structured troubleshooting, error code reading, and software version read-out for all chassis. (see also section "5.4.1 ComPair").

Note: For the new model range, a new remote control (RC) is used with some renamed buttons. This has an impact on the activation of the Service modes. For instance the old "MENU" button is now called "HOME" (or is indicated by a "house" icon).

5.2.1 Service Default Mode (SDM)

Purpose
- To create a pre-defined setting, to get the same measurement results as given in this manual.
- To override SW protections detected by stand-by processor and make the TV start up to the step just before protection (a sort of automatic stepwise start-up). See section "5.3 Stepwise Start-up".
- To start the blinking LED procedure where only LAYER 2 errors are displayed. (see also section "5.5 Error Codes").

Specifications

Table 5-1 SDM default settings

Region	Freq. (MHz)	Default system
Europe, AP(PAL/Multi)	475.25	PAL B/G
Europe, AP DVB-T	546.00 PID Video: 0B 06 PID PCR: 0B 06 PID Audio: 0B 07	DVB-T

- All picture settings at 50% (brightness, colour, contrast).
- All sound settings at 50%, except volume at 25%.
- All service-unfriendly modes (if present) are disabled, like:
  - (Sleep) timer.
  - Child/parental lock.
  - Picture mute (blue mute or black mute).
  - Automatic volume levelling (AVL).
  - Skip/blank of non-favourite pre-sets.

How to Activate SDM

For this chassis there are two kinds of SDM: an **analog SDM** and a **digital SDM**. Tuning will happen according Table 5-1.
- **Analog SDM**: use the standard RC-transmitter and key in the code "062596", directly followed by the "MENU" (or HOME) button.
  Note: It is possible that, together with the SDM, the main menu will appear. To switch it "off", push the "MENU"(or HOME) button again.
- **Digital SDM**: use the standard RC-transmitter and key in the code "062593", directly followed by the "MENU" (or HOME) button.
  Note: It is possible that, together with the SDM, the main menu will appear. To switch it "off", push the "MENU" (or HOME) button again.
- **Analog SDM** can also be activated by grounding for a moment the solder pad on the SSB, with the indication "SDM" (see Service mode pad).

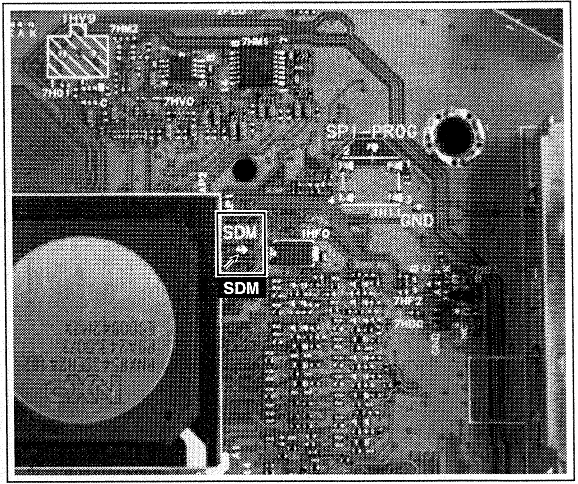

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Figure 5-1 Service mode pad

After activating this mode, "SDM" will appear in the upper right corner of the screen (when a picture is available).

How to Navigate
When the "MENU" (or HOME) button is pressed on the RC transmitter, the TV set will toggle between the SDM and the normal user menu.

How to Exit SDM
Use one of the following methods:
- Switch the set to STAND-BY via the RC-transmitter.
- Via a standard customer RC-transmitter: key in "00"-sequence.

5.2.2 Service Alignment Mode (SAM)

Purpose
- To perform (software) alignments.
- To change option settings.
- To easily identify the used software version.

- To view operation hours.
- To display (or clear) the error code buffer.

How to Activate SAM

Via a standard RC transmitter: Key in the code "062596" directly followed by the "INFO" button. After activating SAM with this method a service warning will appear on the screen, continue by pressing the "OK" button on the RC.

Contents of SAM (see also Table 6-4)

- **Hardware Info.**
  - **A. SW Version.** Displays the software version of the main software (**example:** Q5492-1.2.3.4 = AAAAB_X.Y.W.Z).
    - **AAAA**= the chassis name.
    - **B**= the SW branch version. This is a sequential number (this is no longer the region indication, as the software is now multi-region).
    - **X.Y.W.Z**= the software version, where X is the main version number (different numbers are not compatible with one another) and Y.W.Z is the sub version number (a higher number is always compatible with a lower number).
  - **B. STBY PROC Version.** Displays the software version of the stand-by processor.
  - **C. Production Code.** Displays the production code of the TV, this is the serial number as printed on the back of the TV set. Note that if an NVM is replaced or is initialized after corruption, this production code has to be re-written to NVM. ComPair will foresee in a possibility to do this.
- **Operation Hours.** Displays the accumulated total of operation hours (not the stand-by hours). Every time the TV is switched "on/off", 0.5 hours is added to this number.
- **Errors** (followed by maximum 10 errors). The most recent error is displayed at the upper left (for an error explanation see section "5.5 Error Codes").
- **Reset Error Buffer.** When "cursor right" (or the "OK button) is pressed and then the "OK" button is pressed, the error buffer is reset.
- **Alignments.** This will activate the "ALIGNMENTS" sub-menu. See Chapter 6. Alignments.
- **Dealer Options.** Extra features for the dealers.
- **Options.** Extra features for Service. For more info regarding option codes, 6. Alignments.
  Note that if the option code numbers are changed, these have to be confirmed with pressing the "OK" button before the options are stored. Otherwise changes will be lost.
- **Initialize NVM.** The moment the processor recognizes a corrupted NVM, the "initialize NVM" line will be highlighted. Now, two things can be done (dependent of the service instructions at that moment):
  - Save the content of the NVM via ComPair for development analysis, **before** initializing. This will give the Service department an extra possibility for diagnosis (e.g. when Development asks for this).
  - Initialize the NVM.

Note: When the NVM is corrupted, or replaced, there is a high possibility that no picture appears because the display code is not correct. So, before initializing the NVM via the SAM, a picture is necessary and therefore the correct display option has to be entered. Refer to Chapter 6. Alignments for details. To adapt this option, it's advised to use ComPair (the correct HEX values for the options can be found in Chapter 6. Alignments) or a method via a standard RC (described below).

Changing the display option via a standard RC: Key in the code "062598" directly followed by the "MENU" (or HOME) button and "XXX" (where XXX is the 3 digit decimal display code as mentioned in Table 6-3). Make sure to key in all three digits, also the leading zero's. If the above action is successful, the front LED will go out as an indication that the RC sequence was correct. After the display option is changed in the NVM, the TV will go to the Stand-by mode. If the NVM was corrupted or empty before this action, it will be initialized first (loaded with default values). This initializing can take up to 20 seconds.

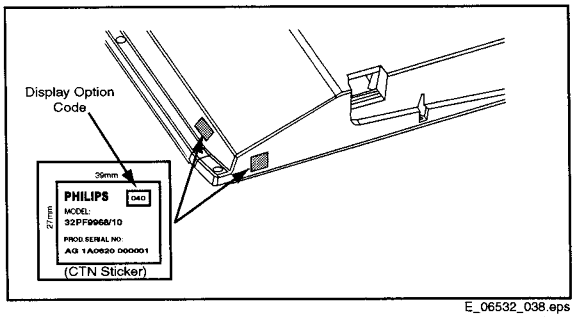

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Figure 5-2 Location of Display Option Code sticker

- **Store - go right.** All options and alignments are stored when pressing "cursor right" (or the "OK" button) and then the "OK"-button.
- **SW Maintenance.**
  - **SW Events.** Not useful for Service purposes. In case of specific software problems, the development department can ask for this info.
  - **HW Events.** Not useful for Service purposes. In case of specific software problems, the development department can ask for this info.
- **Operation hours display.** Displays the accumulated total of display operation hours. So, this one keeps up the lifetime of the display itself, mainly to compensate the degeneration behaviour.
- **Test settings.** For development purposes only.
- **Development file versions.** Not useful for Service purposes, this information is only used by the development department.
- **Upload to USB.** To upload several settings from the TV to an USB stick, which is connected to the SSB. The items are "Channel list", "Personal settings", "Option codes", "Display-related alignments" and "History list". **First a directory "repair\" has to be created in the root of the USB stick.** To upload the settings select each item separately, press "cursor right" (or the "OK" button), confirm with "OK" and wait until "Done" appears. In case the download to the USB stick was not successful "Failure" will appear. In this case, check if the USB stick is connected properly and if the directory "repair" is present in the root of the USB stick. Now the settings are stored onto the USB stick and can be used to download onto another TV or other SSB. Uploading is of course only possible if the software is running and if a picture is available. This method is created to be able to save the customer's TV settings and to store them into another SSB.
- **Download to USB.** To download several settings from the USB stick to the TV, same way of working needs to be followed as with uploading. To make sure that the download of the channel list from USB to the TV is executed properly, it is necessary to restart the TV and tune to a valid preset if necessary.
  Note: The "History list item" can not be downloaded from USB to the TV. This is a "read-only" item. In case of specific problems, the development department can ask for this info.

How to Navigate

- In SAM, the menu items can be selected with the "CURSOR UP/DOWN" key on the RC-transmitter. The selected item will be highlighted. When not all menu items fit on the screen, move the "CURSOR UP/DOWN" key to display the next/previous menu items.
- With the "CURSOR LEFT/RIGHT" keys, it is possible to:
  - (De) activate the selected menu item.
  - (De) activate the selected sub menu.

- With the “OK” key, it is possible to activate the selected action.

How to Exit SAM

Use one of the following methods:

- Switch the TV set to STAND-BY via the RC-transmitter.
- Via a standard RC-transmitter, key in “00” sequence, or select the “BACK” key.

5.2.3 Customer Service Mode (CSM)

Purpose

When a customer is having problems with his TV-set, he can call his dealer or the Customer Helpdesk. The service technician can then ask the customer to activate the CSM, in order to identify the status of the set. Now, the service technician can judge the severity of the complaint. In many cases, he can advise the customer how to solve the problem, or he can decide if it is necessary to visit the customer.
The CSM is a read only mode; therefore, modifications in this mode are not possible.
When in this chassis CSM is activated, a testpattern will be displayed during 5 seconds (1 second Blue, 1 second Green and 1 second Red, then again 1 second Blue and 1 second Green). This test pattern is generated by the PNX5100. So if this test pattern is shown, it could be determined that the back end video chain (PNX5100, LVDS, and display) of the SSB is working.
When CSM is activated and there is a USB stick connected to the TV, the software will dump the complete CSM content to the USB stick. The file (Csm.txt) will be saved in the root of the USB stick. This info can be handy if no information is displayed.

Also when CSM is activated, the LAYER 1 error is displayed via blinking LED. Only the latest error is displayed. (see also section 5.5 Error Codes).

How to Activate CSM

Key in the code “123654” via the standard RC transmitter.

Note: Activation of the CSM is only possible if there is no (user) menu on the screen!

How to Navigate

By means of the “CURSOR-DOWN/UP” knob on the RC-transmitter, can be navigated through the menus.

Contents of CSM

The contents are reduced to 3 pages: General, Software versions and Quality items. The group names itself are not shown anywhere in the CSM menu.

General

- **Set Type.** This information is very helpful for a helpdesk/ workshop as reference for further diagnosis. In this way, it is not necessary for the customer to look at the rear of the TV-set. Note that if an NVM is replaced or is initialized after corruption, this set type has to be re-written to NVM. ComPair will foresee in a possibility to do this.
- **Production Code.** Displays the production code (the serial number) of the TV. Note that if an NVM is replaced or is initialized after corruption, this production code has to be re-written to NVM. ComPair will foresee a in possibility to do this.
- **Installed date.** Indicates the date of the first installation of the TV. This date is acquired via time extraction.
- **Options 1.** Gives the option codes of option group 1 as set in SAM (Service Alignment Mode).
- **Options 2.** Gives the option codes of option group 2 as set in SAM (Service Alignment Mode).
- **12NC SSB.** Gives an identification of the SSB as stored in NVM. Note that if an NVM is replaced or is initialized after corruption, this identification number has to be re-written to NVM. ComPair will foresee in a possibility to do this. This identification number is the 12nc number of the SSB.
- **12NC display.** Shows the 12NC of the display.
- **12NC supply.** Shows the 12NC of the supply.
- **12NC “fan board”.** Shows the 12NC of the “fan board”-module (for sets with LED backlight)
- **12NC “LED Dimming Panel”.** Shows the 12NC of the LED dimming Panel (for sets with LED backlight).

Software versions

- **Current main SW.** Displays the built-in main software version. In case of field problems related to software, software can be upgraded. As this software is consumer upgradeable, it will also be published on the Internet. Example: Q5492_1.2.3.4
- **Standby SW.** Displays the built-in stand-by processor software version. Upgrading this software will be possible via ComPair or via USB (see section 5.9 Software Upgrading).
  Example: STDBY_88.68.1.2.
- **MOP ambient light SW.** Displays the MOP ambient light EPLD SW.
- **LED Dimming SW.** Displays the LED Dimming EPLD SW-version (for sets with LED backlight).
- **Local contrast SW.** Displays the MOP local contrast SW-version.

Quality items

- **Signal quality.** Poor / average /good
- **Child lock.** Not active / active. This is a combined item for locks. If any lock (Preset lock, child lock, lock after or parental lock) is active, the item shall show “active”.
- **HDMI HDCP key.** Indicates if the HDMI keys (or HDCP keys) are valid or not. In case these keys are not valid and the customer wants to make use of the HDMI functionality, the SSB has to be replaced.
- **Ethernet MAC address.** Displays the MAC address present in the SSB.
- **Wireless MAC address.** Displays the wireless MAC address to support the Wi-Fi functionality.
- **BDS key.** Indicates if the “BDS level 1” key is valid or not.
- **CI slot present.** If the common interface module is detected the result will be “YES” or “NO”.
- **HDMI input format.** The detected input format of the HDMI.
- **HDMI audio input stream.** The HDMI audio input stream is displayed: present / not present.
- **HDMI video input stream.** The HDMI video input stream is displayed: present / not present.

How to Exit CSM

Press “MENU” (or HOME) / “Back” key on the RC-transmitter.

5.3 Stepwise Start-up

When the TV is in a protection state due to an error detected by stand-by software (error blinking is displayed) **and** SDM is activated via shortcutting the pins on the SSB, the TV starts up until it reaches the situation just before protection. So, this is a kind of automatic stepwise start-up. In combination with the start-up diagrams below, you can see which supplies are present at a certain moment. Important to know is, that if e.g. the 3V3 detection fails and thus error layer 2 = 18 is blinking while the TV is restarted via SDM, the Stand-by Processor will enable the 3V3, but the TV set will not go to protection now. The TV will stay in this situation until it is reset (Mains/AC Power supply interrupted). **Caution:** in case the start-up in this mode with a faulty FET 7U08 is done, you can destroy all IC's supplied by the +3V3, due to overvoltage (12V on 3V3-line). It is recommended to measure first the FET 7U08 or others FET's on shortcircuit before activating SDM via the service pads.

The abbreviations "SP" and "MP" in the figures stand for:

- SP: protection or error detected by the **Stand-by Processor**.
- MP: protection or error detected by the MIPS **Main Processor**.

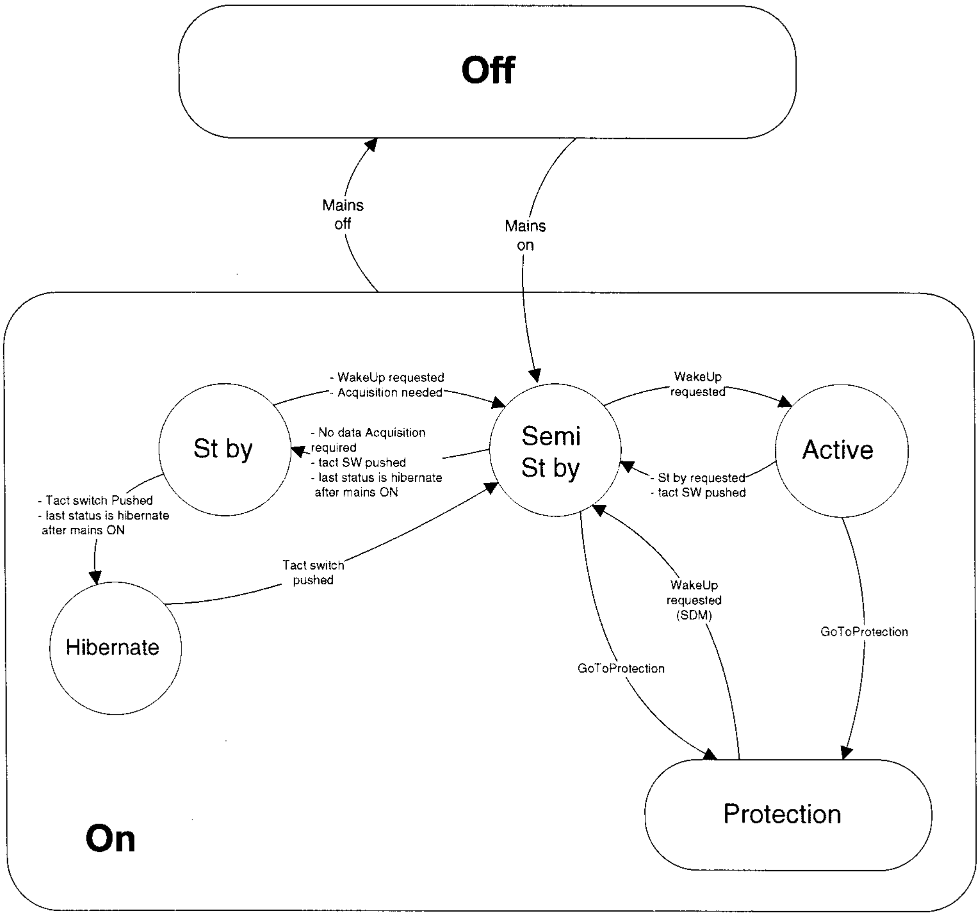

Off
Mains off
Mains on
St by
Semi St by
Active
Hibernate
Protection
On
- WakeUp requested
- Acquisition needed
- No data Acquisition required
- tact SW pushed
- last status is hibernate after mains ON
WakeUp requested
- St by requested
- tact SW pushed
- Tact switch Pushed
- last status is hibernate after mains ON
Tact switch pushed
WakeUp requested (SDM)
GoToProtection
GoToProtection
I_17660_124.eps
140308

Figure 5-3 Transition diagram

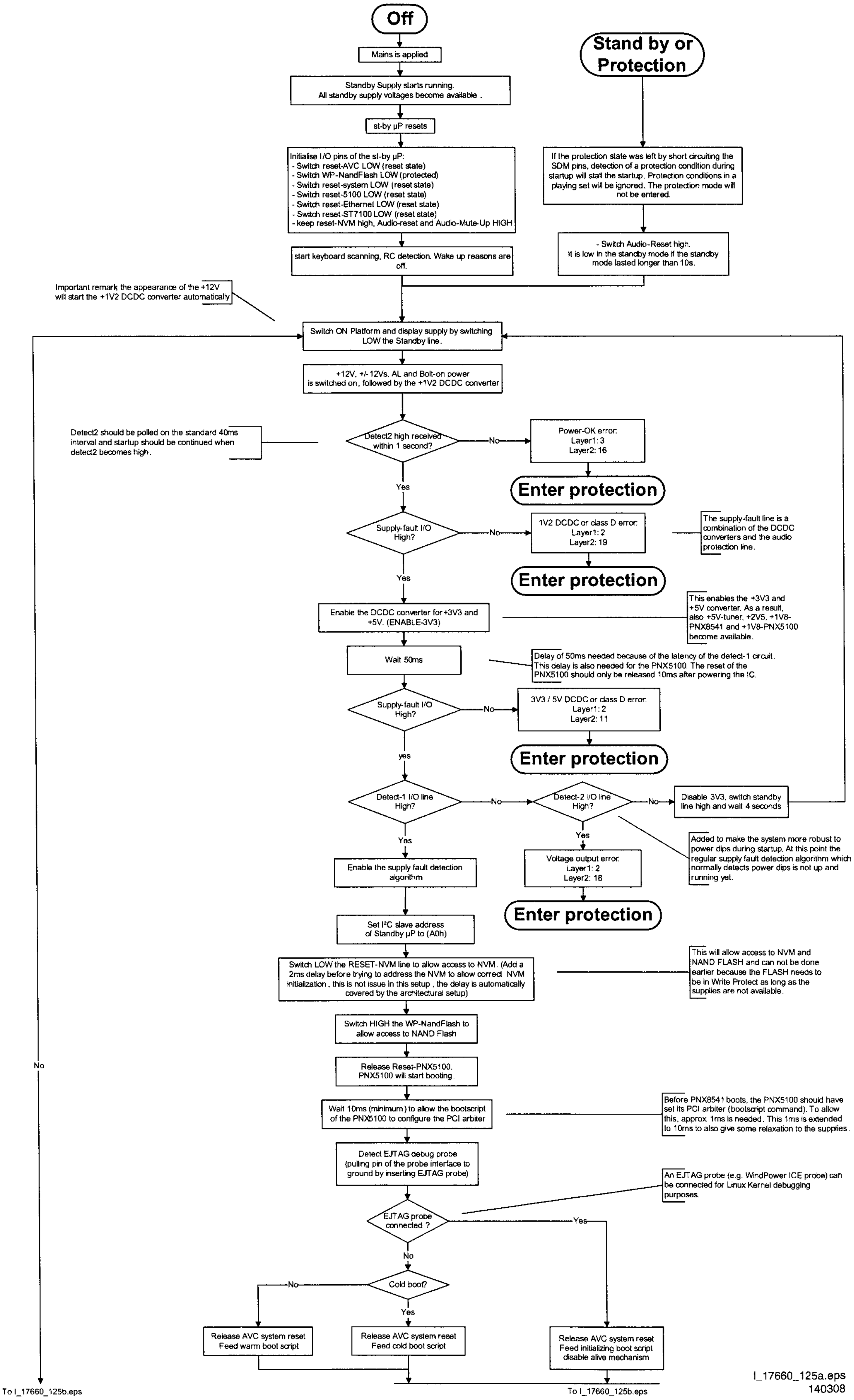
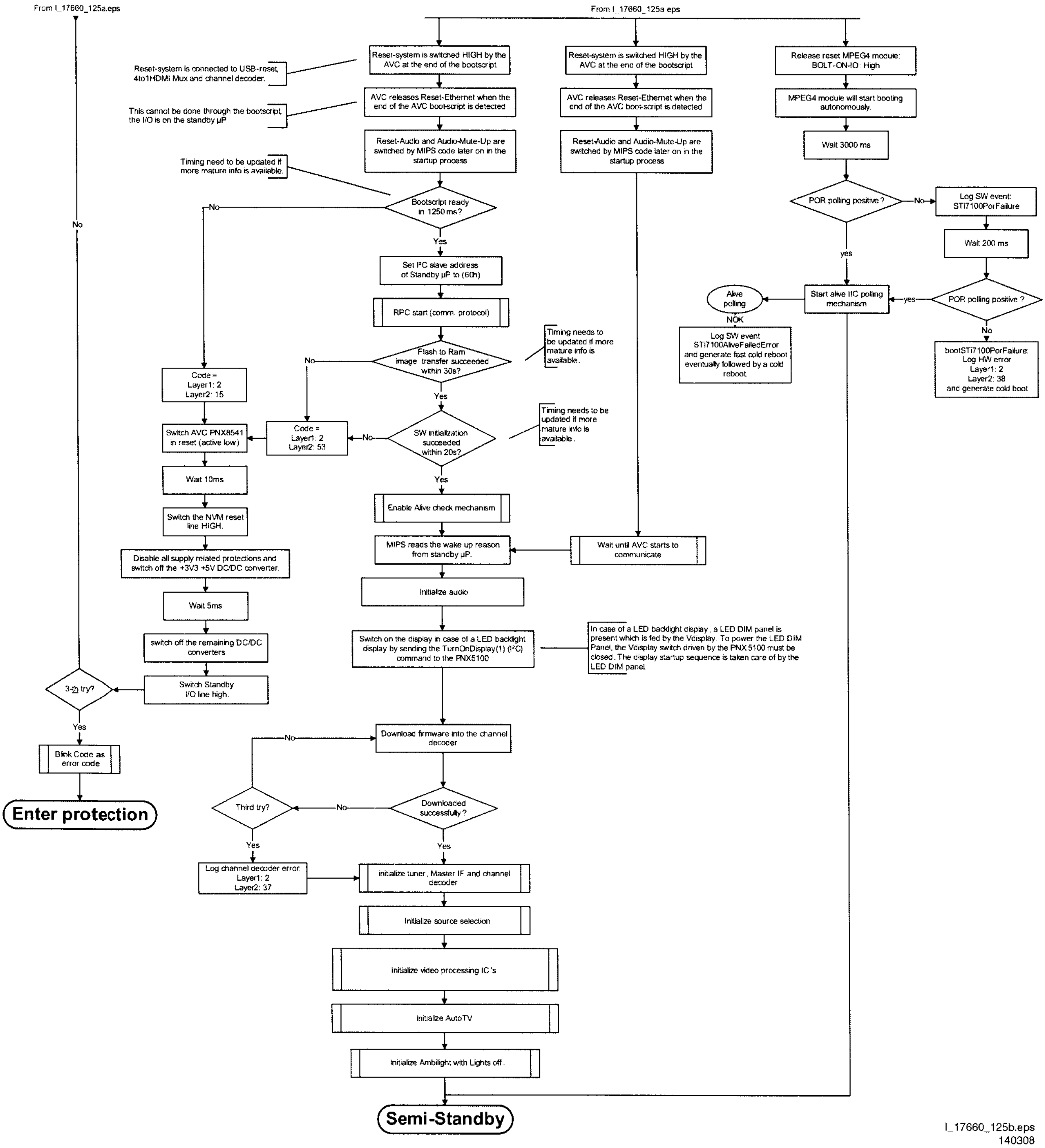

Off
Mains is applied
Standby Supply starts running.
All standby supply voltages become available .
st-by µP resets
Initialise I/O pins of the st-by µP:
- Switch reset-AVC LOW (reset state)
- Switch WP-NandFlash LOW (protected)
- Switch reset-system LOW (reset state)
- Switch reset-5100 LOW (reset state)
- Switch reset-Ethernet LOW (reset state)
- Switch reset-ST7100 LOW (reset state)
- keep reset-NVM high, Audio-reset and Audio-Mute-Up HIGH
start keyboard scanning, RC detection. Wake up reasons are off.
Stand by or Protection
If the protection state was left by short circuiting the SDM pins, detection of a protection condition during startup will stall the startup. Protection conditions in a playing set will be ignored. The protection mode will not be entered.
- Switch Audio-Reset high.
It is low in the standby mode if the standby mode lasted longer than 10s.
Important remark the appearance of the +12V will start the +1V2 DCDC converter automatically
Switch ON Platform and display supply by switching LOW the Standby line.
+12V, +/-12Vs, AL and Bolt-on power is switched on, followed by the +1V2 DCDC converter
Detect2 should be polled on the standard 40ms interval and startup should be continued when detect2 becomes high.
Detect2 high received within 1 second?
No
Power-OK error:
Layer1: 3
Layer2: 16
Enter protection
Yes
Supply-fault I/O High?
No
1V2 DCDC or class D error:
Layer1: 2
Layer2: 19
The supply-fault line is a combination of the DCDC converters and the audio protection line.
Enter protection
Yes
Enable the DCDC converter for +3V3 and +5V. (ENABLE-3V3)
This enables the +3V3 and +5V converter. As a result, also +5V-tuner, +2V5, +1V8-PNX8541 and +1V8-PNX5100 become available.
Wait 50ms
Delay of 50ms needed because of the latency of the detect-1 circuit. This delay is also needed for the PNX5100. The reset of the PNX5100 should only be released 10ms after powering the IC.
Supply-fault I/O High?
No
3V3 / 5V DCDC or class D error:
Layer1: 2
Layer2: 11
Enter protection
yes
Detect-1 I/O line High?
No
Detect-2 I/O line High?
No
Disable 3V3, switch standby line high and wait 4 seconds
Yes
Voltage output error:
Layer1: 2
Layer2: 18
Added to make the system more robust to power dips during startup. At this point the regular supply fault detection algorithm which normally detects power dips is not up and running yet.
Enter protection
Yes
Enable the supply fault detection algorithm
Set I²C slave address of Standby µP to (A0h)
Switch LOW the RESET-NVM line to allow access to NVM. (Add a 2ms delay before trying to address the NVM to allow correct NVM initialization , this is not issue in this setup , the delay is automatically covered by the architectural setup)
This will allow access to NVM and NAND FLASH and can not be done earlier because the FLASH needs to be in Write Protect as long as the supplies are not available.
Switch HIGH the WP-NandFlash to allow access to NAND Flash
No
Release Reset-PNX5100.
PNX5100 will start booting.
Wait 10ms (minimum) to allow the bootscript of the PNX5100 to configure the PCI arbiter
Before PNX8541 boots, the PNX5100 should have set its PCI arbiter (bootscript command). To allow this, approx 1ms is needed. This 1ms is extended to 10ms to also give some relaxation to the supplies.
Detect EJTAG debug probe
(pulling pin of the probe interface to ground by inserting EJTAG probe)
An EJTAG probe (e.g. WindPower ICE probe) can be connected for Linux Kernel debugging purposes.
EJTAG probe connected ?
Yes
No
Cold boot?
No
Yes
Release AVC system reset
Feed warm boot script
Release AVC system reset
Feed cold boot script
Release AVC system reset
Feed initializing boot script
disable alive mechanism
To I_17660_125b.eps
To I_17660_125b.eps
I_17660_125a.eps
140308

Figure 5-4 “Off” to “Semi Stand-by” flowchart (part 1)


From I_17660_125a.eps
From I_17660_125a.eps
Reset-system is connected to USB-reset, 4to1HDMI Mux and channel decoder.
This cannot be done through the bootscript, the I/O is on the standby µP
Timing need to be updated if more mature info is available.
Reset-system is switched HIGH by the AVC at the end of the bootscript
AVC releases Reset-Ethernet when the end of the AVC boot-script is detected
Reset-Audio and Audio-Mute-Up are switched by MIPS code later on in the startup process
Bootscript ready in 1250ms?
No
Yes
Set I²C slave address of Standby µP to (60h)
RPC start (comm. protocol)
Timing needs to be updated if more mature info is available.
Flash to Ram image transfer succeeded within 30s?
No
Yes
Timing needs to be updated if more mature info is available.
SW initialization succeeded within 20s?
No
Yes
Code = Layer1: 2 Layer2: 53
Code = Layer1: 2 Layer2: 15
Switch AVC PNX8541 in reset (active low)
Wait 10ms
Switch the NVM reset line HIGH.
Disable all supply related protections and switch off the +3V3 +5V DC/DC converter.
Wait 5ms
switch off the remaining DC/DC converters
Switch Standby I/O line high.
3-th try?
No
Yes
Blink Code as error code
Enter protection
Enable Alive check mechanism
MIPS reads the wake up reason from standby µP.
Initialize audio
Switch on the display in case of a LED backlight display by sending the TurnOnDisplay(1) (I²C) command to the PNX5100
In case of a LED backlight display, a LED DIM panel is present which is fed by the Vdisplay. To power the LED DIM Panel, the Vdisplay switch driven by the PNX5100 must be closed. The display startup sequence is taken care of by the LED DIM panel
Reset-system is switched HIGH by the AVC at the end of the bootscript
AVC releases Reset-Ethernet when the end of the AVC boot-script is detected
Reset-Audio and Audio-Mute-Up are switched by MIPS code later on in the startup process
Wait until AVC starts to communicate
Release reset MPEG4 module: BOLT-ON-IO: High
MPEG4 module will start booting autonomously.
Wait 3000 ms
POR polling positive ?
No
Log SW event: STi7100PorFailure
Wait 200 ms
POR polling positive ?
yes
yes
No
bootSTi7100PorFailure: Log HW error Layer1: 2 Layer2: 38 and generate cold boot
Start alive IIC polling mechanism
Alive polling
NOK
Log SW event STi7100AliveFailedError and generate fast cold reboot eventually followed by a cold reboot
Download firmware into the channel decoder
No
Downloaded successfully ?
No
Third try?
Yes
Yes
Log channel decoder error Layer1: 2 Layer2: 37
initialize tuner, Master IF and channel decoder
Initialize source selection
Initialize video processing IC's
initialize AutoTV
Initialize Ambilight with Lights off.
Semi-Standby

I_17660_125b.eps
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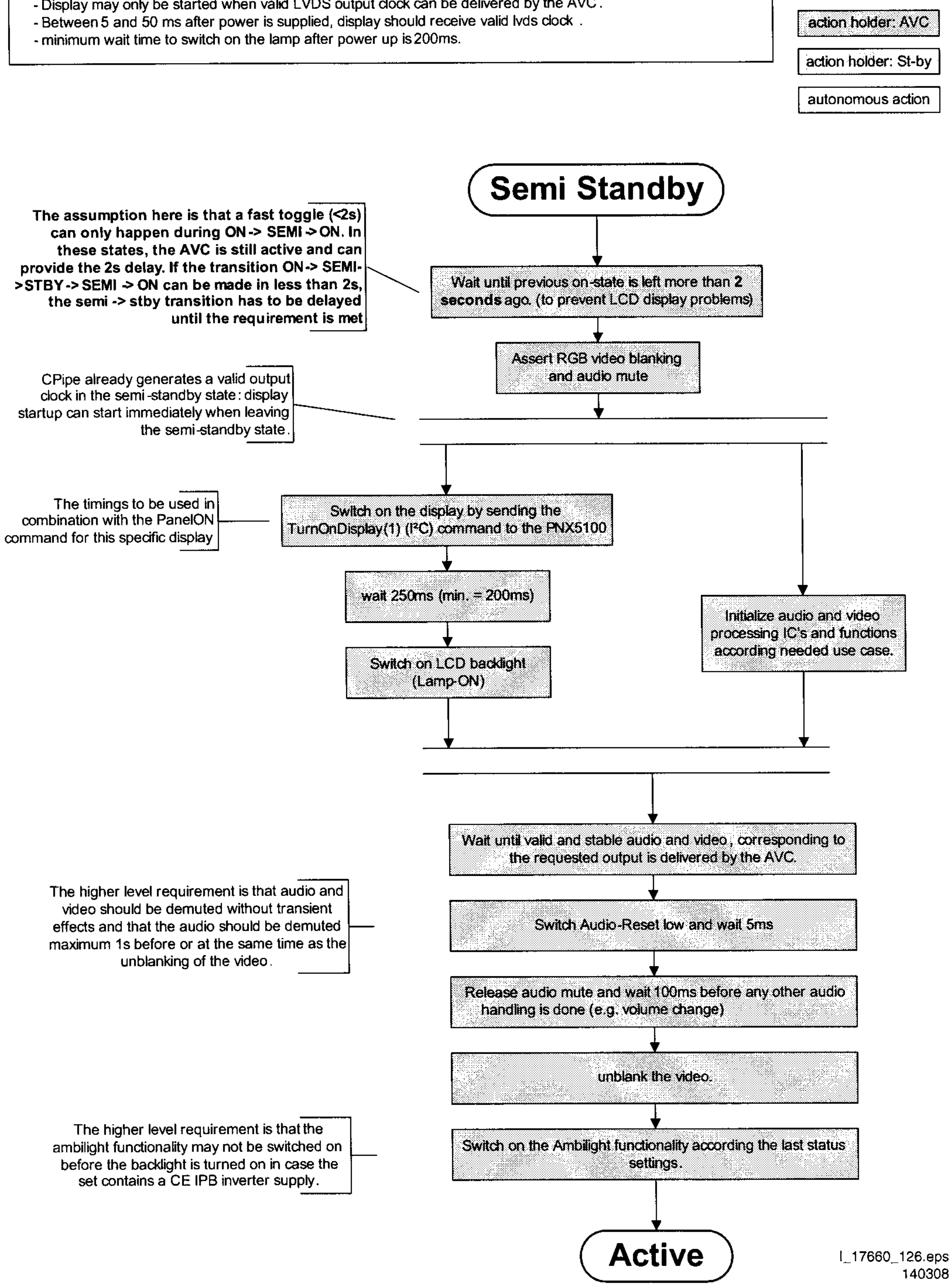
Figure 5-5 “Off” to “Semi Stand-by” flowchart (part 2)

Constraints taken into account:
- Display may only be started when valid LVDS output clock can be delivered by the AVC.
- Between 5 and 50 ms after power is supplied, display should receive valid lvds clock .
- minimum wait time to switch on the lamp after power up is 200ms.


action holder: AVC
action holder: St-by
autonomous action
Semi Standby
Wait until previous on-state is left more than 2 seconds ago. (to prevent LCD display problems)
Assert RGB video blanking and audio mute
Switch on the display by sending the TurnOnDisplay(1) (I²C) command to the PNX5100
wait 250ms (min. = 200ms)
Switch on LCD backlight (Lamp-ON)
Initialize audio and video processing IC's and functions according needed use case.
Wait until valid and stable audio and video, corresponding to the requested output is delivered by the AVC.
Switch Audio-Reset low and wait 5ms
Release audio mute and wait 100ms before any other audio handling is done (e.g. volume change)
unblank the video.
Switch on the Ambilight functionality according the last status settings.
Active

The assumption here is that a fast toggle (<2s) can only happen during ON-> SEMI -> ON. In these states, the AVC is still active and can provide the 2s delay. If the transition ON-> SEMI->STBY-> SEMI -> ON can be made in less than 2s, the semi -> stby transition has to be delayed until the requirement is met

CPipe already generates a valid output clock in the semi-standby state: display startup can start immediately when leaving the semi-standby state.

The timings to be used in combination with the PanelON command for this specific display

The higher level requirement is that audio and video should be demuted without transient effects and that the audio should be demuted maximum 1s before or at the same time as the unblanking of the video.

The higher level requirement is that the ambilight functionality may not be switched on before the backlight is turned on in case the set contains a CE IPB inverter supply.

I_17660_126.eps
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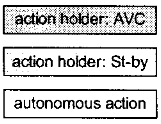
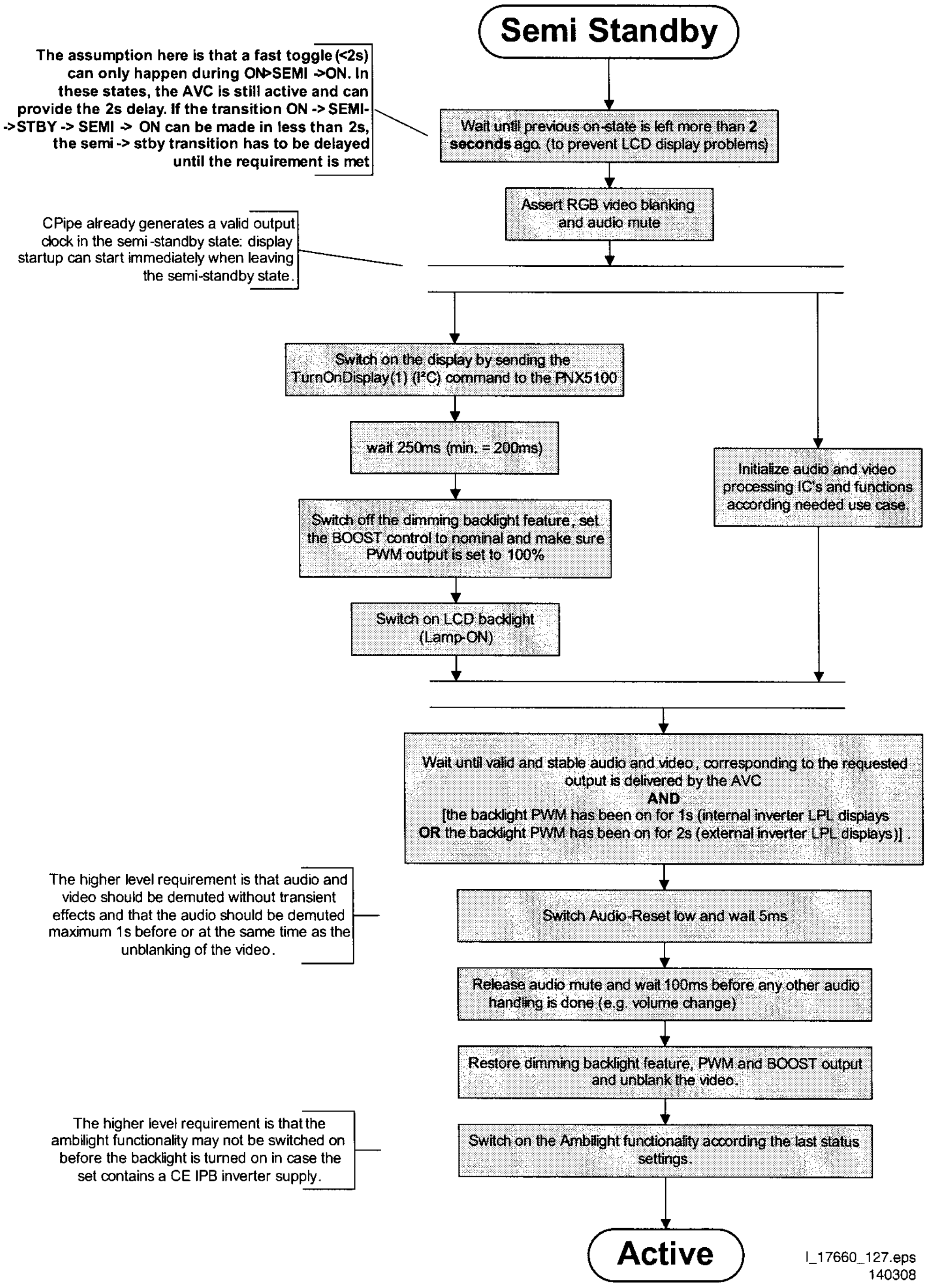
Figure 5-6 “Semi Stand-by” to “Active” flowchart

Constraints taken into account:

- Display may only be started when valid LVDS output clock can be delivered by the AVC.
- Between 5 and 50 ms after power is supplied, display should receive valid lvds clock .
- minimum wait time to switch on the lamp after power up is 200ms.
- To have a reliable operation of the backlight, the backlight should be driven with a PWM duty cycle of 100% during the first second. Only after this first one or two seconds, the PWM may be set to the required output level (Note that the PWM output should be present before the backlight is switched on). To minimize the artefacts, the picture should only be unblanked after these first seconds.


action holder: AVC
action holder: St-by
autonomous action


Semi Standby
Wait until previous on-state is left more than 2 seconds ago. (to prevent LCD display problems)
Assert RGB video blanking and audio mute
Switch on the display by sending the TurnOnDisplay(1) (I²C) command to the PNX5100
wait 250ms (min. = 200ms)
Switch off the dimming backlight feature, set the BOOST control to nominal and make sure PWM output is set to 100%
Switch on LCD backlight (Lamp-ON)
Initialize audio and video processing IC's and functions according needed use case.
Wait until valid and stable audio and video, corresponding to the requested output is delivered by the AVC
AND
[the backlight PWM has been on for 1s (internal inverter LPL displays
OR the backlight PWM has been on for 2s (external inverter LPL displays)] .
Switch Audio-Reset low and wait 5ms
Release audio mute and wait 100ms before any other audio handling is done (e.g. volume change)
Restore dimming backlight feature, PWM and BOOST output and unblank the video.
Switch on the Ambilight functionality according the last status settings.
Active

The assumption here is that a fast toggle (<2s) can only happen during ON>SEMI ->ON. In these states, the AVC is still active and can provide the 2s delay. If the transition ON -> SEMI- ->STBY -> SEMI -> ON can be made in less than 2s, the semi -> stby transition has to be delayed until the requirement is met

CPipe already generates a valid output clock in the semi-standby state: display startup can start immediately when leaving the semi-standby state.

The higher level requirement is that audio and video should be demuted without transient effects and that the audio should be demuted maximum 1s before or at the same time as the unblanking of the video.

The higher level requirement is that the ambilight functionality may not be switched on before the backlight is turned on in case the set contains a CE IPB inverter supply.

I_17660_127.eps
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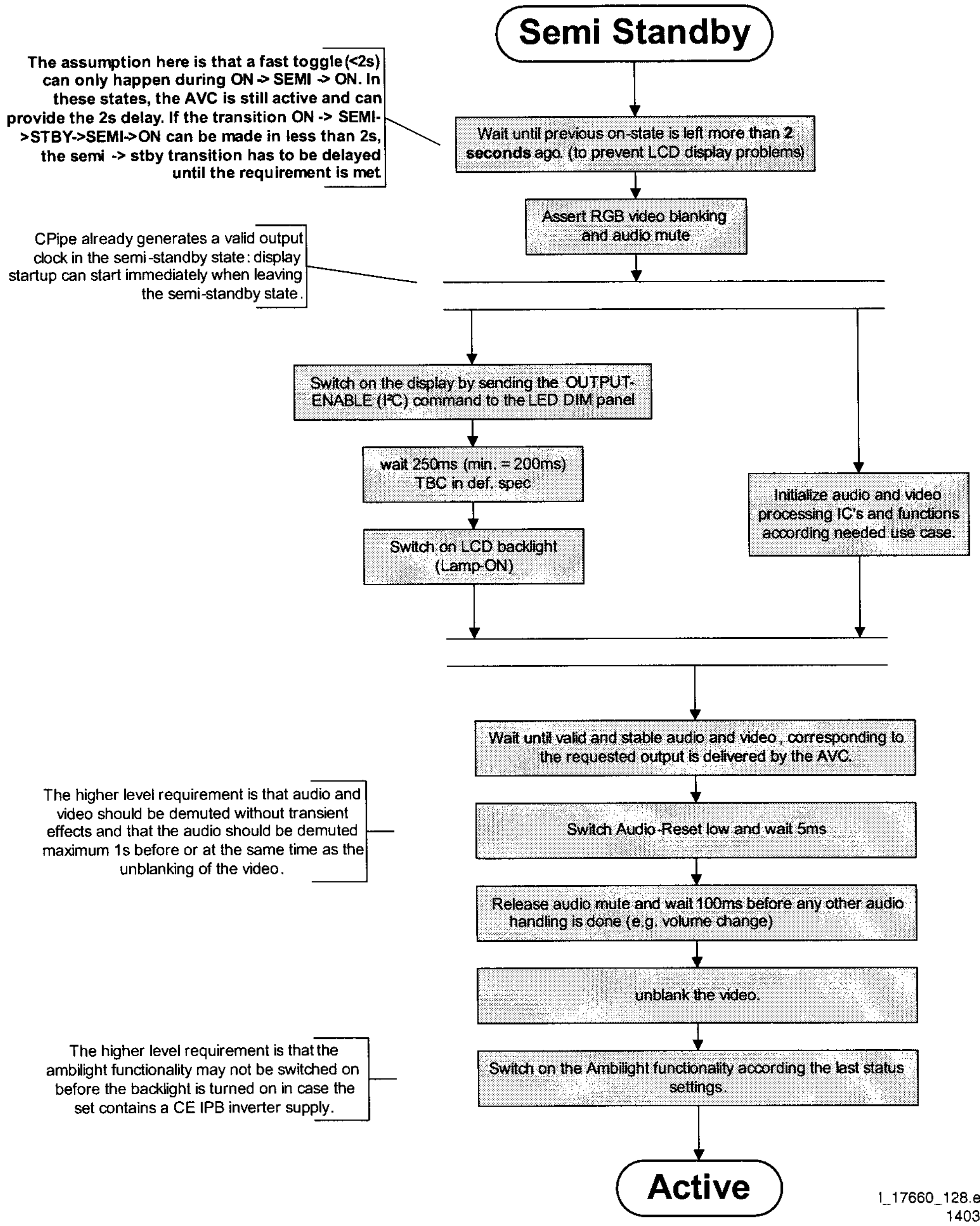
Figure 5-7 "Semi Stand-by" to "Active" flowchart LCD with preheat

Constraints taken into account:
- Display may only be started when valid LVDS output clock can be delivered by the AVC.
- Between 5 and 50 ms after power is supplied, display should receive valid lvds clock .
- minimum wait time to switch on the lamp after power up is 200ms.

action holder: AVC

action holder: St-by

autonomous action


Semi Standby
Wait until previous on-state is left more than 2 seconds ago. (to prevent LCD display problems)
Assert RGB video blanking and audio mute
Switch on the display by sending the OUTPUT-ENABLE (I²C) command to the LED DIM panel
wait 250ms (min. = 200ms) TBC in def. spec
Switch on LCD backlight (Lamp-ON)
Initialize audio and video processing IC's and functions according needed use case.
Wait until valid and stable audio and video, corresponding to the requested output is delivered by the AVC.
Switch Audio-Reset low and wait 5ms
Release audio mute and wait 100ms before any other audio handling is done (e.g. volume change)
unblank the video.
Switch on the Ambilight functionality according the last status settings.
Active

The assumption here is that a fast toggle (<2s) can only happen during ON -> SEMI -> ON. In these states, the AVC is still active and can provide the 2s delay. If the transition ON -> SEMI->STBY->SEMI->ON can be made in less than 2s, the semi -> stby transition has to be delayed until the requirement is met

CPipe already generates a valid output clock in the semi-standby state: display startup can start immediately when leaving the semi-standby state.

The higher level requirement is that audio and video should be demuted without transient effects and that the audio should be demuted maximum 1s before or at the same time as the unblanking of the video.

The higher level requirement is that the ambilight functionality may not be switched on before the backlight is turned on in case the set contains a CE IPB inverter supply.

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Figure 5-8 “Semi Stand-by” to “Active” flowchart (LED backlight)

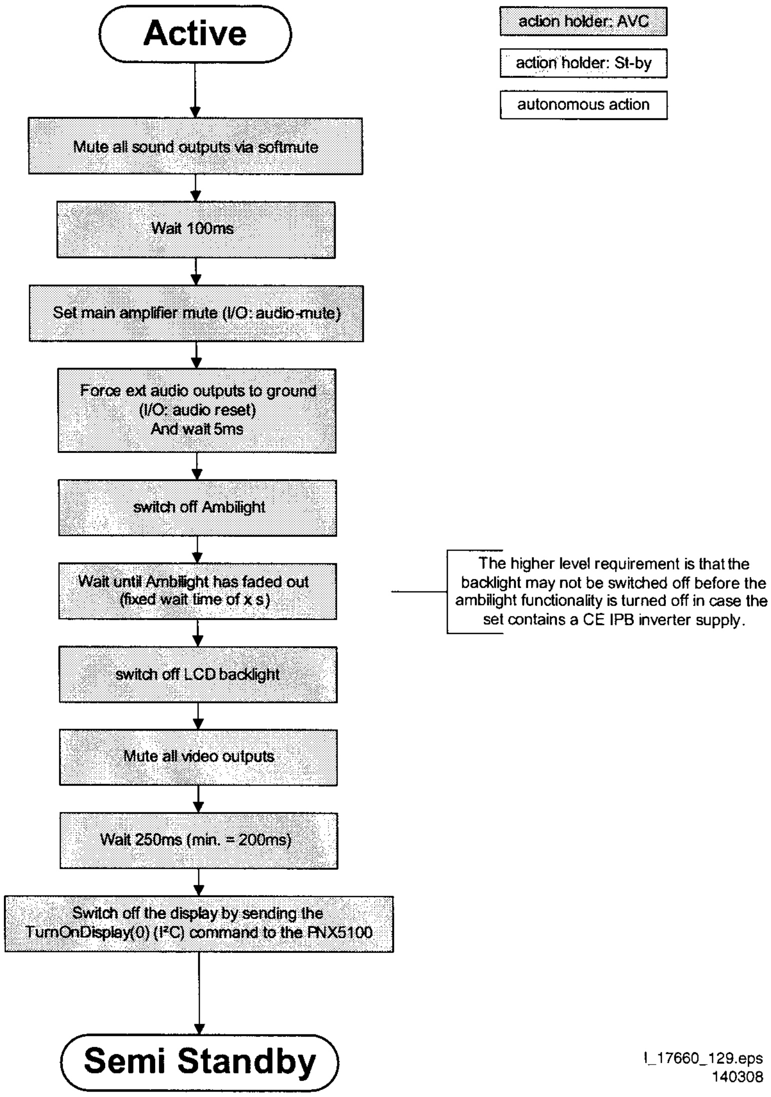
Active
action holder: AVC
action holder: St-by
autonomous action
Mute all sound outputs via softmute
Wait 100ms
Set main amplifier mute (I/O: audio-mute)
Force ext audio outputs to ground
(I/O: audio reset)
And wait 5ms
switch off Ambilight
Wait until Ambilight has faded out
(fixed wait time of x s)
The higher level requirement is that the backlight may not be switched off before the ambilight functionality is turned off in case the set contains a CE IPB inverter supply.
switch off LCD backlight
Mute all video outputs
Wait 250ms (min. = 200ms)
Switch off the display by sending the TurnOnDisplay(0) (I²C) command to the PNX5100
Semi Standby

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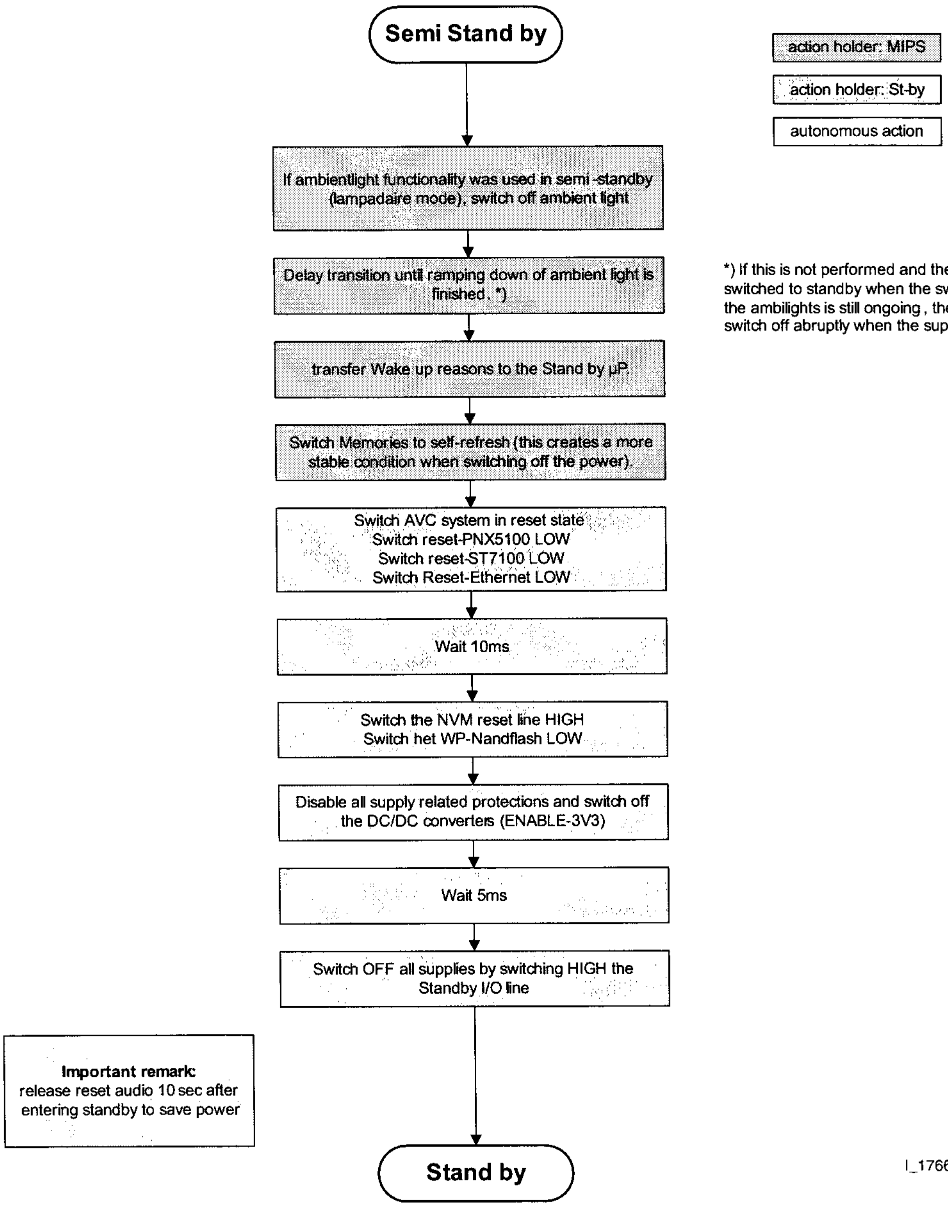
Figure 5-9 “Active” to “Semi Stand-by” flowchart (LCD non DFI)


Semi Stand by
action holder: MIPS
action holder: St-by
autonomous action
If ambientlight functionality was used in semi -standby (lampadaire mode), switch off ambient light
Delay transition until ramping down of ambient light is finished. *)
transfer Wake up reasons to the Stand by µP.
Switch Memories to self-refresh (this creates a more stable condition when switching off the power).
Switch AVC system in reset state
Switch reset-PNX5100 LOW
Switch reset-ST7100 LOW
Switch Reset-Ethernet LOW
Wait 10ms
Switch the NVM reset line HIGH
Switch het WP-Nandflash LOW
Disable all supply related protections and switch off the DC/DC converters (ENABLE-3V3)
Wait 5ms
Switch OFF all supplies by switching HIGH the Standby I/O line
Important remark:
release reset audio 10 sec after entering standby to save power
Stand by

*) If this is not performed and the set is switched to standby when the switch off of the ambilights is still ongoing, the lights will switch off abruptly when the supply is cut.

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Figure 5-10 “Semi Stand-by” to “Stand-by” flowchart

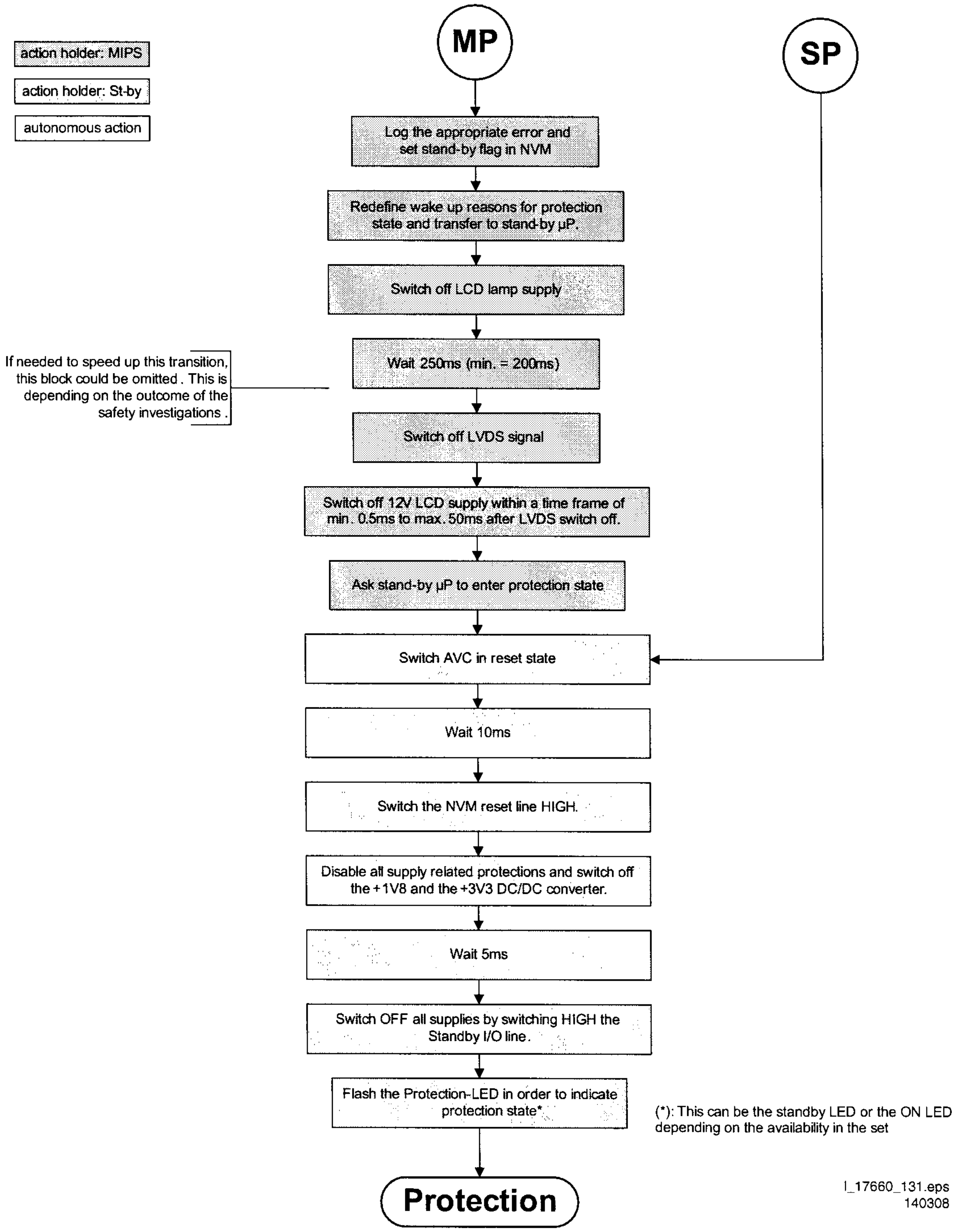
action holder: MIPS
action holder: St-by
autonomous action
MP
SP
Log the appropriate error and set stand-by flag in NVM
Redefine wake up reasons for protection state and transfer to stand-by µP.
Switch off LCD lamp supply
If needed to speed up this transition, this block could be omitted. This is depending on the outcome of the safety investigations.
Wait 250ms (min. = 200ms)
Switch off LVDS signal
Switch off 12V LCD supply within a time frame of min. 0.5ms to max. 50ms after LVDS switch off.
Ask stand-by µP to enter protection state
Switch AVC in reset state
Wait 10ms
Switch the NVM reset line HIGH.
Disable all supply related protections and switch off the +1V8 and the +3V3 DC/DC converter.
Wait 5ms
Switch OFF all supplies by switching HIGH the Standby I/O line.
Flash the Protection-LED in order to indicate protection state*
(*): This can be the standby LED or the ON LED depending on the availability in the set
Protection

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Figure 5-11 "To Protection State" flowchart

5.4 Service Tools

5.4.1 ComPair

Introduction

ComPair (Computer Aided Repair) is a Service tool for Philips Consumer Electronics products. and offers the following:

1. ComPair helps to quickly get an understanding on how to repair the chassis in a short and effective way.
2. ComPair allows very detailed diagnostics and is therefore capable of accurately indicating problem areas. No knowledge on I^2C or UART commands is necessary, because ComPair takes care of this.
3. ComPair speeds up the repair time since it can automatically communicate with the chassis (when the uP is working) and all repair information is directly available.
4. ComPair features TV software up possibilities.

Specifications

ComPair consists of a Windows based fault finding program and an interface box between PC and the (defective) product. The ComPair II interface box is connected **to the PC** via an USB cable. For the TV chassis, the ComPair interface box and the TV communicate via a bi-directional cable via the service connector(s).

The ComPair fault finding program is able to determine the problem of the defective television, by a combination of automatic diagnostics and an interactive question/answer procedure.

How to Connect

This is described in the chassis fault finding database in ComPair.

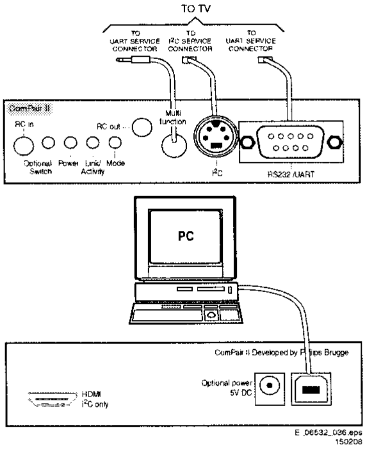


Figure 5-12 ComPair II interface connection

Caution: It is compulsory to connect the TV to the PC as shown in the picture above (with the ComPair interface in between), as the ComPair interface acts as a level shifter. If one connects the TV directly to the PC (via UART), ICs will be blown!

How to Order

ComPair II order codes:

- ComPair II interface: 3122 785 91020.
- Software is available via the Philips Service web portal.
- ComPair UART interface cable for Q54x.x.
  (using 3.5 mm Mini Jack connector): 3138 188 75051.

Note: While encounting problems, contact the local support desk.

5.4.2 Memory and Audio Test

With this tool you can test the memory of the PNX8543, as well if the PNX5100 is enabled and audio-testing.

What is needed?

- An USB-stick
- "TESTSCRIPT Q549". Downloadable from the Philips Service website from the section "Software for Service only"
- A ComPair/service cable (3138 188 75051).

Procedure

Create a directory "JETTFILES" under the root of the USB-stick

- Place "MemTestTV543.bin" and "autojett.bin" (available in "TESTSCRIPT Q549") under the directory "JETTFILES"
- Install the computer program "BOARDTESTLOGGER" (available in "TESTSCRIPT Q549") on the PC
- Connect a "ComPair/service"-cable from the service-connector in the set, into the "multi function" jack at the front of the ComPair II box :
  Required settings in ComPair :
  - start up the ComPair application.
  - Select the correct database (open file "Q549.2E LA", this will set the ComPair interface in the appropriate mode).
  - Close ComPair
- Start up the program "BOARDTESTLOGGER" and select "COMx"
- Put the USB stick into the TV and start up the TV while pressing the "i+"-button on a Philips DVD RC6 remote control (it's also possible to use a TV remote in "DVD"-mode)
- On the PC the memory test is shown now. This is also visible on the TV screen.
- In "BOARDTESTLOGGER" an option "Send extra UART command" can be found where you can select "AUD1". This command generates hear test tones of 200, 400, 1000, 2000, 3000, 5000, 8000 and 12500Hz.

5.5 Error Codes

5.5.1 Introduction

The error code buffer contains all detected errors since the last time the buffer was erased. The buffer is written from left to right, new errors are logged at the left side, and all other errors shift one position to the right.

When an error occurs, it is added to the list of errors, provided the list is not full. When an error occurs and the error buffer is full, then the new error is not added, and the error buffer stays intact (history is maintained).

To prevent that an occasional error stays in the list forever, the error is removed from the list after more than 50 hrs. of operation.

When multiple errors occur (errors occurred within a short time span), there is a high probability that there is some relation between them.

New in this chassis is the way errors can be displayed:

- There is a simple blinking LED procedure for board level repair (home repair) so called LAYER 1 errors next to the existing errors which are LAYER 2 errors (see Table 5-2).
  - LAYER 1 errors are one digit errors.
  - LAYER 2 errors are 2 digit errors.
- In protection mode.
  - From consumer mode: **LAYER 1.**
  - From SDM mode: **LAYER 2.**
- **Fatal errors, if I2C bus is blocked and the set reboots, CSM and SAM are not selectable.**
  - From consumer mode: **LAYER 1.**
  - From SDM mode: **LAYER 2.**
    Important remark:

  For all errors detected by MIPS which are fatal => rebooting of the TV set (reboot starts after LAYER 1 error blinking), one should short the solder paths (SDM) at start-up from the power OFF state by mains interruption and not via the power button to trigger the SDM via the hardware pins.
- In CSM mode
  - When entering CSM: error **LAYER 1** will be displayed by blinking LED. Only the latest error is shown.
- In SDM mode
  - When SDM is entered via Remote Control code or the hardware pins, **LAYER 2** is displayed via blinking LED.
- In the ON state
  - In "Display error mode", set with the RC commands "mute_06250X _OK" **LAYER 2** errors are displayed via blinking LED.
- Error display on screen.
  - In CSM no error codes are displayed on screen.
  - In SAM the complete error list is shown.

Basically there are three kinds of errors:
- **Errors detected by the Stand-by software which lead to protection.** These errors will always lead to protection and an automatic start of the blinking LED LAYER 1 error. (see section "5.6 The Blinking LED Procedure").
- **Errors detected by the Stand-by software which not lead to protection.** In this case the front LED should blink the involved error. See also section "5.5 Error Codes, 5.5.4 Error Buffer, Extra Info". Note that it can take up several minutes before the TV starts blinking the error (e.g. LAYER 1 error = 2, LAYER 2 error = 15 or 53).
- **Errors detected by main software (MIPS).** In this case the error will be logged into the error buffer and can be read out via ComPair, via blinking LED method LAYER 1-2 error, or in case picture is visible, via SAM.

5.5.2 How to Read the Error Buffer

Use one of the following methods:
- On screen via the SAM (only when a picture is visible). E.g.:
  - **00 00 00 00 00**: No errors detected
  - **23 00 00 00 00**: Error code 23 is the last and only detected error.
  - **37 23 00 00 00**: Error code 23 was first detected and error code 37 is the last detected error.
  - Note that no protection errors can be logged in the error buffer.
- Via the blinking LED procedure. See section 5.5.3 How to Clear the Error Buffer.
- Via ComPair.

5.5.3 How to Clear the Error Buffer

Use one of the following methods:
- By activation of the "RESET ERROR BUFFER" command in the SAM menu.
- With a normal RC, key in sequence "MUTE" followed by "062599" and "OK".
- If the content of the error buffer has not changed for 50+ hours, it resets automatically.

5.5.4 Error Buffer

In case of non-intermittent faults, clear the error buffer before starting to repair (**before** clearing the buffer, write down the content, as this history can give significant information). This to ensure that old error codes are no longer present.
If possible, check the entire contents of the error buffer. In some situations, an error code is only the result of another error code and not the actual cause (e.g. a fault in the protection detection circuitry can also lead to a protection).
There are several mechanisms of error detection:
- Via error bits in the status registers of ICs.
- Via polling on I/O pins going to the stand-by processor.
- Via sensing of analog values on the stand-by processor or the PNX8543.
- Via a "not acknowledge" of an I^2C communication.

Take notice that some errors need several minutes before they start blinking or before they will be logged. So in case of problems wait 2 minutes from start-up onwards, and then check if the front LED is blinking or if an error is logged.

Table 5-2 Error code overview

Description	Layer 1	Layer 2	Monitored by	Error/ Prot	Error Buffer/ Blinking LED	Device	Defective Board
I^2C3	2	13	MIPS	E	BL / EB	SSB	SSB
I^2C2	2	14	MIPS	E	BL / EB	SSB/Display	SSB/display
PNX doesn't boot (HW cause) PNX 5100 doesn't boot	2	15	Stby µP	P	BL	PNX8543/PNX51XX I^2C blocked	SSB
12V	3	16	Stby µP	P	BL	/	Supply
Inverter or display supply	3	17	MIPS	E	EB	/	
1V2, 3V3, 5V to low	2	18	Stby µP	P	BL	/	SSB
Temp protection	3	12	MIPS	E	EB	/	Display
PNX 5100	2	21	MIPS	E	EB	PNX5100	SSB
HDMI mux	2	23	MIPS	E	EB	TDA9996	SSB
I^2C switch	2	24	MIPS	E	EB	PCA9540	SSB
Boot-NVM PNX5100	2	25	MIPS	E	EB	STM24C08	SSB
Multi Standard demodulator (Micronas IF)	2	27	MIPS	E	EB	DRX3616K DRX3626K	SSB
ARM (ambilight)	8	28	MIPS	E	EB	NXP LPC2103	AL module or DC/DC
FPGA (Local contrast)	2	29	MIPS	E	EB	Altera	SSB
Tuner	2	34	MIPS	E	EB	UV1783S/HD1816	SSB
Fan I2C expander	7	41	MIPS	E	EB	PCA9533	FAN module
T° sensor	7	42	MIPS	E	EB	LM 75	T° sensor
FAN 1	7	43	MIPS	E	EB		FAN
FAN 2	7	44	MIPS	E	EB		FAN
Main NVM	2	/	MIPS	E	X	STM24C128	SSB
PNX doesn't boot (SW cause)	2	53	Stby µP	E	BL	PNX8543	SSB
Display (only 56PFL9954H)	5	64	MIPS	E	BL / EB	Altera	Display

Extra Info

- **Rebooting.** When a TV is constantly rebooting due to internal problems, most of the time no errors will be logged or blinked. This rebooting can be recognized via a ComPair interface and Hyperterminal (for Hyperterminal settings, see section "5.8 Fault Finding and Repair Tips, 5.8.6 Logging). It's shown that the loggings which are generated by the main software keep continuing. In this case diagnose has to be done via ComPair.
- **Error 13 (I^2C bus 3 blocked).** At the time of release of this manual, this error was not working as expected. Current situation: when this error occurs, the TV will constantly reboot due to the blocked bus. The best way for further diagnosis here, is to use ComPair.
- **Error 15 (PNX8543,PNX5100 doesn't boot).** Indicates that the main processor/PNX5100 was not able to read his bootscript. This error will point to a hardware problem around the PNX8543 (supplies not OK, PNX 8543 completely dead, I^2C link between PNX and Stand-by Processor broken, etc...). When error 15 occurs it is also possible that I^2C1 bus is blocked (NVM). I^2C1 can be indicated in the schematics as follows: SCL-UP-MIPS, SDA-UP-MIPS, SCL-1, SDA-1, SCL-2 or SDA-2.
  Other root causes for this error can be due to hardware problems from the NVM PNX5100, DDR's and the bootscript reading from the PNX5100.
- **Error 16 (12V).** This voltage is made in the power supply and results in protection (LAYER 1 error = 3) in case of absence. When SDM is activated we see blinking LED LAYER 2 error = 16.
- **Error 17 (Invertor or Display Supply).** Here the status of the "Power OK" is checked by software, no protection will occur during failure of the invertor or display supply (no picture), only error logging. LED blinking of LAYER 1 error = 3 in CSM, in SDM this gives LAYER 2 error = 17.
- **Error 18 (1V2-3V3-5V too low).** All these supplies are generated by the DC/DC supply on the SSB. If one of these supplies is too low, protection occurs and blinking LED LAYER 1 error = 2 will be displayed automatically. In SDM this gives LAYER 2 error = 18.
- **Error 21 (PNX 5100).** When there is no I^2C communication towards the PNX5100, the TV set will start rebooting and display LAYER 1 error = 2. Disconnect the mains cord now and start up the TV set with the solder path (SDM) short to ground during start-up to activate the LAYER 2 error blinking. Error "21" will be logged and displayed via the blinking LED procedure after a few moments from start-up. Remark : the rebooting can be recognized via a ComPair interface and Hyperterminal (for Hyperterminal settings, see section "5.8 Fault Finding and Repair Tips, 5.8.6 Logging"). It is shown that the loggings which are generated by the main software keep continuing. Check in the logging for keywords like e.g. "Device error 21".
- **Error 23 (HDMI).** When there is no I^2C communication towards the HDMI mux after start-up, LAYER 2 error = 23 will be logged and displayed via the blinking LED procedure if SDM is switched on. It should be noted that in case a new spare EDID MUX device is used for repair, the initial default address must be changed from "C0" to "CE", to be done via ComPair.
- **Error 24 (I^2C switch).** When there is no I^2C communication towards the I^2C switch, LAYER 2 error = 24 will be logged and displayed via the blinking LED procedure when SDM is switched on. Remark : this only works for TV sets with an I^2C controlled screen included.
- **Error 25 (Boot-NVM PNX5100).** Same behaviour as described in "Error 21 (PNX5100)".
- **Error 27 (Micronas IF).** When there is no I^2C communication towards the multi standard demodulator, LAYER 2 error = 27 will be logged and displayed via the blinking LED procedure if SDM is switched on.
- **Error 28 (ARM ambilight).** When there is no I^2C communication towards the ARM processor, LAYER 2 error = 28 will be logged and displayed via the blinking LED procedure if SDM is switched on.
- **Error 29 (FPGA local contrast).** When there is no I^2C communication towards this FPGA, LAYER 2 error = 29 will be logged and displayed via the blinking LED procedure if SDM is activated.
- **Error 34 (Tuner).** When there is no I^2C communication towards the tuner after start-up, LAYER 2 error = 34 will be

logged and displayed via the blinking LED procedure when SDM is switched on.

- **Error 42 (Temp sensor)**. Only applicable for TV sets with an I^2C controlled screen.
- **Main NVM**. When there is no I^2C communication towards the main NVM, LAYER 1 error = 2 will be displayed via the blinking LED procedure. In SDM, LAYER 2 error will be blinked as "15". Errors here can not be logged due to inaccessibility of the NVM device.
- **Error 53**. This error will indicate that the PNX8543 has read his bootscript (when this would have failed, error 15 would blink) but initialization was never completed because of hardware problems (NAND flash, ...) or software initialization problems. Possible cause could be that there is no valid software loaded (try to upgrade to the latest main software version). Note that it can take a few minutes before the TV starts blinking LAYER 1 error = 2 or in SDM, LAYER 2 error = 53.
- **Error 64**. Only applicable for TV sets with an I^2C controlled screen .

5.6 The Blinking LED Procedure

5.6.1 Introduction

The blinking LED procedure can be split up into two situations:

- Blinking LED procedure LAYER 1 error. In this case the error is automatically blinked when the TV is put in CSM. This will be only one digit error, namely the one that is referring to the defective board (see table "5-2 Error code overview") which causes the failure of the TV. This approach will especially be used for home repair and call centres. The aim here is to have service diagnosis from a distance.
- Blinking LED procedure LAYER 2 error. Via this procedure, the contents of the error buffer can be made visible via the front LED. In this case the error contains 2 digits (see table "5-2 Error code overview") and will be displayed when SDM (hardware pins) is activated. This is especially useful for fault finding and gives more details regarding the failure of the defective board.

Important remark:
For all errors detected by MIPS which are fatal => rebooting of the TV set (reboot starts after LAYER 1 error blinking), one should short the solder paths at start-up from the power OFF state by mains interruption and not via the power button to trigger the SDM via the hardware pins.

When one of the blinking LED procedures is activated, the front LED will show (blink) the contents of the error buffer. Error codes greater then 10 are shown as follows:

1. "n" long blinks (where "n" = 1 to 9) indicating decimal digit
2. A pause of 1.5 s
3. "n" short blinks (where "n"= 1 to 9)
4. A pause of approximately 3 s,
5. When all the error codes are displayed, the sequence finishes with a LED blink of 3 s
6. The sequence starts again.

Example: Error 12 8 6 0 0.
After activation of the SDM, the front LED will show:

1. One long blink of 750 ms (which is an indication of the decimal digit) followed by a pause of 1.5 s
2. Two short blinks of 250 ms followed by a pause of 3 s
3. Eight short blinks followed by a pause of 3 s
4. Six short blinks followed by a pause of 3 s
5. One long blink of 3 s to finish the sequence
6. The sequence starts again.

5.6.2 How to Activate

Use one of the following methods:

- **Activate the CSM**. The blinking front LED will show only the latest layer 1 error, this works in "normal operation" mode or automatically when the error/protection is monitored by the standby processor.
  In case no picture is shown and there is no LED blinking, read the logging to detect whether "error devices" are mentioned. (see section "5.8 Fault Finding and Repair Tips, 5.8.6 Logging").
- **Activate the SDM**. The blinking front LED will show the entire content of the LAYER 2 error buffer, this works in "normal operation" mode or when SDM (via hardware pins) is activated when the tv set is in protection.
  Important remark:
  For all errors detected by MIPS which are fatal => rebooting of the TV set (reboot starts after LAYER 1 error blinking), one should short the solder paths at start-up from the power OFF state by mains interruption and not via the power button to trigger the SDM via the hardware pins.
- **Transmit the commands "MUTE" - "062500" - "OK" with a normal RC.** The complete error buffer is shown. Take notice that it takes some seconds before the blinking LED starts.
- **Transmit the commands "MUTE" - "06250x" - "OK" with a normal RC** (where "x" is a number between 1 and 5). When x = 1 the last detected error is shown, x = 2 the second last error, etc.... Take notice that it takes some seconds before the blinking LED starts.

5.7 Protections

5.7.1 Software Protections

Most of the protections and errors use either the stand-by microprocessor or the MIPS controller as detection device. Since in these cases, checking of observers, polling of ADCs, and filtering of input values are all heavily software based, these protections are referred to as software protections. There are several types of software related protections, solving a variety of fault conditions:

- **Protections related to supplies:** check of the 12V, +5V, +3V3 and 1V2.
- **Protections related to breakdown of the safety check mechanism.** E.g. since the protection detections are done by means of software, failing of the software will have to initiate a protection mode since safety cannot be guaranteed any more.

Remark on the Supply Errors
The detection of a supply dip or supply loss during the normal playing of the set does not lead to a protection, but to a cold reboot of the set. If the supply is still missing after the reboot, the TV will go to protection.

Protections during Start-up
During TV start-up, some voltages and IC observers are actively monitored to be able to optimise the start-up speed, and to assure good operation of all components. If these monitors do not respond in a defined way, this indicates a malfunction of the system and leads to a protection. As the observers are only used during start-up, they are described in the start-up flow in detail (see section "5.3 Stepwise Start-up").

5.7.2 Hardware Protections

The only real hardware protection in this chassis appears in case of an audio problem e.g. DC voltage on the speakers. This protection will only affect the Class D (7D10) and puts the amplifier in a continuous burst mode (cyclus approximately 2 seconds).

Repair Tip

- There will be still picture available but no sound. While the Class D amplifier tries to start-up again, the cone of the loudspeakers will move slowly in one or the other direction until the initial failure shuts the amplifier down, this cyclus starts over and over again.

5.7.3 Important remark regarding the blinking LED indication

As for the blinking LED indication, the blinking led of LAYER 1 error displaying can be switched off by pushing the power button on the keyboard.
This condition is not valid after the set was unpowered (via mains interruption). The blinking LED starts again and can only be switched off by unplugging the mains connection.
This can be explained by the fact that the MIPS can not load the keyboard functionality from software during the start-up and doesn't recognizes the keyboard commands at this time.

5.8 Fault Finding and Repair Tips

Read also section "5.5 Error Codes, 5.5.4 Error Buffer, Extra Info".

5.8.1 Ambilight

Due to degeneration process of the AmbiLights, there can be a difference in the colour and/or light output of the spare ambilight module in comparison with the originals ones contained in the TV set. Via ComPair the light output can be adjusted.

5.8.2 Audio Amplifier

The Class D-IC 7D10 has a powerpad for cooling. When the IC is replaced it must be ensured that the powerpad is very well pushed to the PWB while the solder is still liquid. This is needed to insure that the cooling is guaranteed, otherwise the Class D-IC could break down in short time.

5.8.3 CSM

When CSM is activated and there is a USB stick connected to the TV, the software will dump the complete CSM content to the USB stick. The file (Csm.txt) will be saved in the root of the USB stick. If this mechanism works it can be concluded that a large part of the operating system is already working (MIPS, USB...)

5.8.4 DC/DC Converter

Description

The onboard supply consists of 5 DC/DC converters and 4 linear stabilizers. All DC/DC converters have +12V input voltage and deliver :

- +1V2-PNX85XX supply voltage (1.24V nominal), stabilized close to PNX8543 chip.
- +1V2-PNX5120 supply voltage (1.26V nominal), stabilized close to PNX5120 chip.
- +3V3 (3.34V nominal, overall 3.3 V for onboard IC's).
- +5V (5.15V nominal) for USB and Conditional Access Interface and +5V5-TUN for +5V-TUN tuner stabilizer.
- +33VTUN (34V nominal) for analog-only tuners.

The linear stabilizers are providing:

- +1V2-STANDBY (out of +3V3-STANDBY), 1.24V nominal.
- +1V8-PNX85XX and +1V8PNX5100 (connected via CFH1), 1.84V nominal.
- +2V5 (WOW FPGA diversity only), 2.5V nominal.
- +5V-TUN (out of +5V5-TUN), 5V nominal.

+3V3-STANDY and +1V2-STANDBY are permanent voltages. Supply voltages +1V2-PNX85XX and +1V2-PNX5100 are started immediately when +12V incoming voltage is available (+12V is enabled by STANDBY signal, active low). Supply voltages +3V3, 2V5, +1V8-PNX5100, +1V8-PNX85XX, +5V and +5V-TUN are switched-on directly by signal ENABLE-3V3 (active low), provided that +12V (detected via 7U40 &7U41) is available. +12V is considered OK (=> DETECT -12V signal becomes high and 12V/3V3 and 12V/5V DC-DC converter can be started up) if it rises above 10V5 (typical) and doesn't drop below 10V (typical).

Debugging

The best way to find a failure in the DC/DC converters is to check their start-up sequence at power-on via the mains cord, presuming that the standby microprocessor and the external supply are operational. Take STANDBY signal high-to-low transition as time reference.
When +12V becomes available (maximum 1 second after STANDBY signal goes low) then +1V2-PNX85XX and +1V2-PNX5100 are started immediately. Then, after ENABLE-3V3 goes low, all the other supply voltages should rise within 2ms.

Tips

- When an output supply voltage is short-circuited to GND the corresponding DC-DC converter is not making any audible noise, the converter switches-off immediately and will attempt a re-start only after +12V drops and rises again.
- Check the integrity (at least no short-circuit between drain and source) of power MOS-FETs, especially the high-side ones: 7U05, 7U08, 7U0D-1 and 7U0H-1 before starting the platform in SDM mode, otherwise it can be easily damaged.
- Switching frequency of DC-DC converters should be around 290KHz for 12V to 1V2 DC-DC converters and around 370KHz for 12V to 3V3 and 12V to 5V DC-DC converters.

5.8.5 Exit "Factory Mode"

When an "F" is displayed in the screen's right corner, this means the set is in "Factory" mode, and it normally happens after a new SSB is mounted. To exit this mode, push the "VOLUME minus" button on the TV's local keyboard for 10 seconds (this disables the continuous mode).
Then push the "SOURCE" button for 10 seconds until the "F" disappears from the screen.

5.8.6 Logging

When something is wrong with the TV set (f.i.the set is rebooting) you can check for more information via the logging in Hyperterminal. The Hyperterminal is available in every Windows application via Programs, Accessories, Communications, Hyperterminal. Connect a "ComPair UART"-cable (3138 188 75051) from the service connector in the TV to the "multi function" jack at the front of ComPair II box.
Required settings in ComPair before starting to log :
- Start up the ComPair application.
- Select the correct database (open file "Q549.2E LA", this will set the ComPair interface in the appropriate mode).
- Close ComPair
After start-up of the Hyperterminal, fill in a name (f.i. "logging") in the "Connection Description" box, then apply the following settings:

1. COMx
2. Bits per second = 115200
3. Data bits = 8
4. Parity = none
5. Stop bits = 1
6. Flow control = none

During the start-up of the TV set, the logging will be displayed. This is also the case during rebooting of the TV set (the same logging appears time after time). Also available in the logging is the "Display Option Code" (useful when there is no picture), look for item “DisplayRawNumber” in the beginning of the logging. Tip: when there is no picture available during rebooting you are able to check for “error devices” in the logging (LAYER 2 error) which can be very helpful to determine the failure cause of the reboot. For protection state, there is no logging.

5.8.7 Loudspeakers

Make sure that the volume is set to minimum during disconnecting the speakers in the ON-state of the TV. The audio amplifier can be damaged by disconnecting the speakers during ON-state of the set!

5.8.8 IPB

In case of no picture when CSM-test pattern from PNX5100 is activated and backlight doesn't light up, it's recommended first to check the inverter on the IPB + wiring (LAYER 2 error = 17 is displayed in SDM).

5.8.9 Tuner

Attention: In case the tuner is replaced, always check the tuner options!

5.8.10 PCI bus

The splash screen image is not distributed via the regular YUV signal path from the PNX8543 to the PNX51XX, but loaded one time via the PCI bus.Once the splash screen image is loaded into the PNX51XX, it will be continuously generated by the PNX51XX until the first incoming video disables the splash screen.So when teletext and/or general UI is available, but no splash screen (option “ON”) is visible during start-up, check the PCI bus as possible root cause.

5.8.11 Display option code

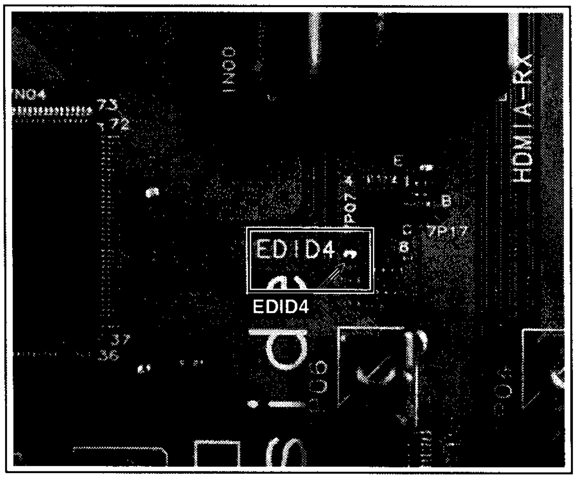
Attention: In case the SSB is replaced, always check the display option code in SAM, even when picture is available. Performance with the incorrect display option code can lead to unwanted side-effects for certain conditions.

5.8.12 Upgrade HDMI EDID NVM

The EDID MUX device (including all HDMI NVM except the 4th) is upgradeable via USB, see ComPair for further instructions. It should be noted that in case a new spare EDID MUX device is used for repair, the initial default address must be changed from “C0” to “CE”, to be done via ComPair.

5.8.13 Upgrade VGA/4th HDMI EDID NVM

The EDID for VGA connector or the 4th HDMI can only be upgraded via external I^2C. To upgrade the EDID for the VGA connector or 4th HDMI, pin 7 of the EDID NVM has to be short circuited to ground. Therefore a test point is foreseen (see Figure 5-13). For the VGA EDID NVM it's most suitable to connect pin 7 to ground on the NVM device itself. See ComPair for further instructions.



18310_220_090318.eps
090319

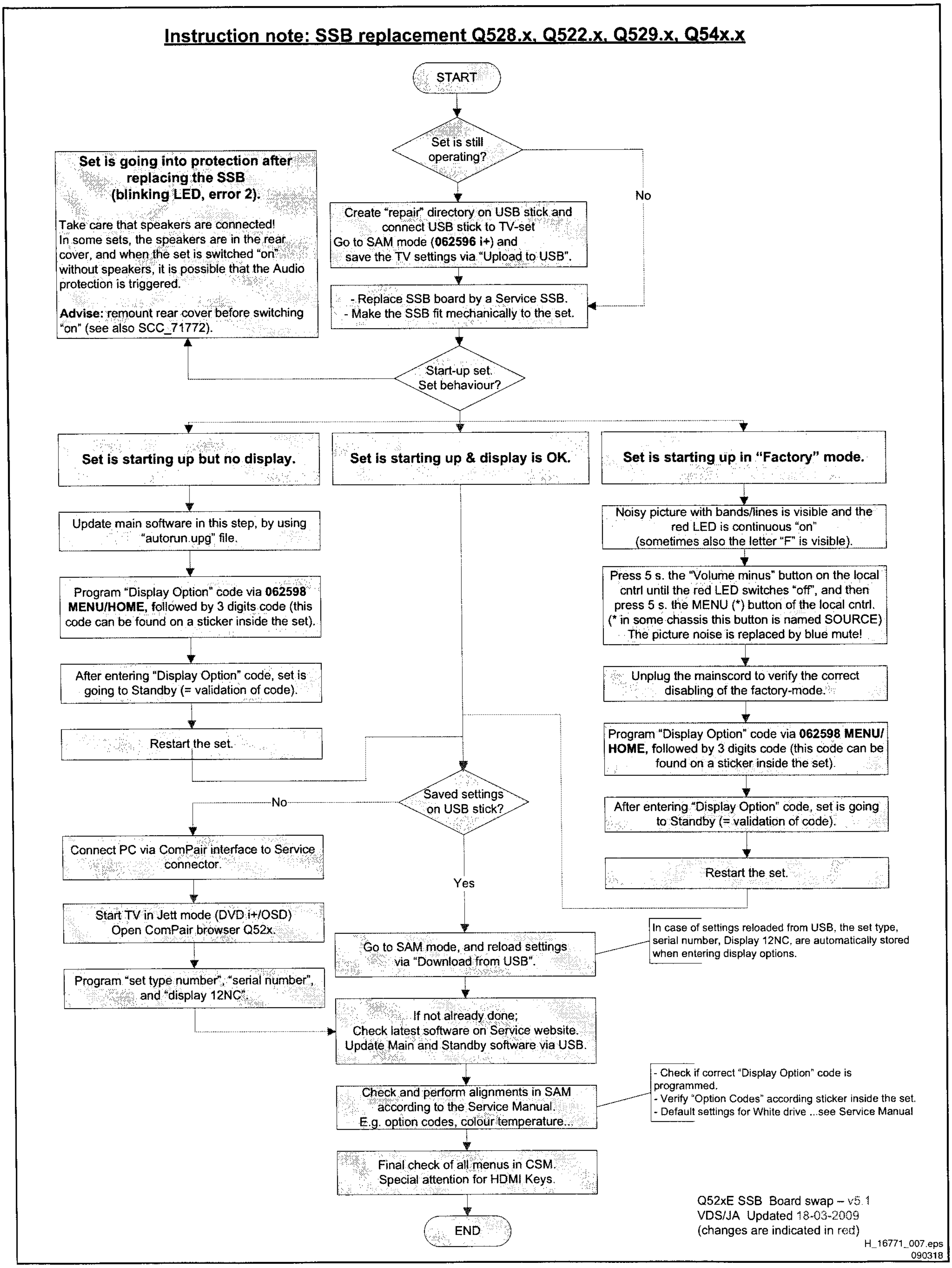
Figure 5-13 4th HDMI EDID NVM pin

5.8.14 Wi-Fi module

To prevent damage on the coax wires, especially the female core of the coax wires (can be bend over during dis- and reconnecting), this should be carried out by use of pliers.

5.8.15 SSB Replacement

Follow the instructions in the flowchart in case a SSB has to be exchanged. See figure "SSB replacement flowchart".



Instruction note: SSB replacement Q528.x, Q522.x, Q529.x, Q54x.x

Set is still operating?

Create "repair" directory on USB stick and connect USB stick to TV-set
Go to SAM mode (**062596 i+**) and save the TV settings via "Upload to USB".

- Replace SSB board by a Service SSB.
- Make the SSB fit mechanically to the set.

Start-up set. Set behaviour?

Set is going into protection after replacing the SSB (blinking LED, error 2).

Take care that speakers are connected!
In some sets, the speakers are in the rear cover, and when the set is switched "on" without speakers, it is possible that the Audio protection is triggered.

Advise: remount rear cover before switching "on" (see also SCC_71772).

Set is starting up but no display.

Update main software in this step, by using "autorun.upg" file.

Program "Display Option" code via **062598 MENU/HOME,** followed by 3 digits code (this code can be found on a sticker inside the set).

After entering "Display Option" code, set is going to Standby (= validation of code).

Restart the set.

Set is starting up & display is OK.

Set is starting up in "Factory" mode.

Noisy picture with bands/lines is visible and the red LED is continuous "on" (sometimes also the letter "F" is visible).

Press 5 s. the "Volume minus" button on the local cntrl until the red LED switches "off", and then press 5 s. the MENU (*) button of the local cntrl.
(* in some chassis this button is named SOURCE)
The picture noise is replaced by blue mute!

Unplug the mainscord to verify the correct disabling of the factory-mode.

Program "Display Option" code via **062598 MENU/HOME,** followed by 3 digits code (this code can be found on a sticker inside the set).

After entering "Display Option" code, set is going to Standby (= validation of code).

Restart the set.

Saved settings on USB stick?

Connect PC via ComPair interface to Service connector.

Start TV in Jett mode (DVD i+/OSD)
Open ComPair browser Q52x.

Program "set type number", "serial number", and "display 12NC".

Go to SAM mode, and reload settings via "Download from USB".

In case of settings reloaded from USB, the set type, serial number, Display 12NC, are automatically stored when entering display options.

If not already done;
Check latest software on Service website.
Update Main and Standby software via USB.

Check and perform alignments in SAM according to the Service Manual.
E.g. option codes, colour temperature...

- Check if correct "Display Option" code is programmed.
- Verify "Option Codes" according sticker inside the set.
- Default settings for White drive ...see Service Manual

Final check of all menus in CSM.
Special attention for HDMI Keys.

Q52xE SSB Board swap – v5.1
VDS/JA Updated 18-03-2009
(changes are indicated in red)

H_16771_007.eps
090318

Figure 5-14 SSB replacement flowchart

5.9 Software Upgrading

5.9.1 Introduction

The set software and security keys are stored in a NAND-Flash, which is connected to the PNX8543 via the PCI bus.

It is possible **for the user** to upgrade the **main** software via the USB port. This allows replacement of a software image in a stand alone set, without the need of an E-JTAG debugger. A description on how to upgrade the main software can be found in the DFU.

Important: When the NAND-Flash must be replaced, a new SSB must be ordered, due to the presence of the security keys! (copy protection keys, MAC address, ...).
Perform the following actions after SSB replacement:

1. Set the correct option codes (see sticker inside the TV).
2. Update the TV software => see the eUM (electronic User Manual) for instructions.
3. Perform the alignments as described in chapter 6 (section 6.5 Reset of Repaired SSB).
4. Check in CSM if the HDMI key, MAC address.. are valid.

For the correct order number of a new SSB, always refer to the Spare Parts list!

5.9.2 Main Software Upgrade

- The "UpgradeAll.upg" file is only used in the factory.
- The "FlashUtils.upg" file is only used by service centra which are allowed to do component level repair on the SSB.

Automatic Software Upgrade
In "normal" conditions, so when there is no major problem with the TV, the main software and the default software upgrade application can be upgraded with the "AUTORUN.UPG" (FUS part of the one-zip file: e.g. 3104 337 05661 _FUS _Q5492_ 1.26.15.0_commercial.zip). This can also be done by the consumers themselves, but they will have to get their software from the commercial Philips website or via the Software Update Assistant in the user menu (see eUM). The "autorun.upg" file must be placed in the root of the USB stick.
How to upgrade:

1. Copy "AUTORUN.UPG" to the root of the USB stick.
2. Insert USB stick in the set while the set is in ON MODE. The set will restart and the upgrading will start automatically. As soon as the programming is finished, a message is shown to remove the USB stick and restart the set.

Manual Software Upgrade
In case that the software upgrade application does not start automatically, it can also be started manually.
How to start the software upgrade application manually:

1. Disconnect the TV from the Mains/AC Power.
2. Press the "OK" button on a Philips TV remote control or a Philips DVD RC-6 remote control (it is also possible to use a TV remote in "DVD" mode). Keep the "OK" button pressed while reconnecting the TV to the Mains/AC Power.
3. The software upgrade application will start.

Attention!
In case the download application has been started **manually**, the "autorun.upg" will maybe not be recognized.
What to do in this case:

1. Create a directory "UPGRADES" on the USB stick.
2. Rename the "autorun.upg" to something else, e.g. to "software.upg". Do not use long or complicated names, keep it simple. Make sure that "AUTORUN.UPG" is no longer present in the root of the USB stick.
3. Copy the renamed "upg" file into this directory.
4. Insert USB stick into the TV.
5. The renamed "upg" file will be visible and selectable in the upgrade application.

Back-up Software Upgrade Application
If the default software upgrade application does not start (could be due to a corrupted boot 2 sector) via the above described method, try activating the "back-up software upgrade application".
How to start the "back-up software upgrade application" manually:

1. Disconnect the TV from the Mains/AC Power.
2. Press the "INFO"-button on a Philips remote control or "CURSOR DOWN" button on a Philips DVD RC-6 remote control (it is also possible to use a TV remote in "DVD" mode). Keep the "INFO"-button (or "cursor down" button) pressed while reconnecting the TV to the Mains/AC Power.
3. The software upgrade application will start.

5.9.3 Stand-by Software Upgrade via USB

In this chassis it is possible to upgrade the Stand-by software via a USB stick. The method is similar to upgrading the main software via USB.
Use the following steps:

1. Create a directory "UPGRADES" on the USB stick.
2. Copy the Stand-by software (part of the one-zip file, e.g. StandbySW_CFT72_88.0.0.0.upg) into this directory.
3. Insert the USB stick into the TV.
4. Start the download application manually (see section "_ Manual Software Upgrade".
5. Select the appropriate file and press the "OK" button to upgrade.

5.9.4 Content and Usage of the One-Zip Software File

Below the content of the One-Zip file is explained, and instructions on how and when to use it.

- **BootProm_PNX5120_Q5492_x.x.x.x.zip.** A programmed device can be ordered via the regional Service organization.
- **Ceisp2padll_P2PAD_x.x.x.x.zip.** Not to be used by Service technicians. For ComPair development only.
- **DDC_Q5492_x.x.x.x.zip.** Contains the content of the VGA NVM. See ComPair for further instruction.
- **EDID_Q5492_x.x.x.x.zip.** Contains the EDID content of the different EDID NVM's. See ComPair for further instructions.
- **EJTAGDownload_Q5492_x.x.x.x.zip.** Only used by service centra which are allowed to do component level repair.
- **FUS_Q5492_x.x.x.x_commercial.zip.** Contains the "autorun.upg" which is needed to upgrade the TV main software and the software download application.
- **Factory_Q5492_x.x.x.x_commercial.zip.** Only for production purposes, not to be used by Service technicians.
- **FlashUtils_Q5492_x.x.x.x_commercial.zip.** Not to be used by Service technicians.
- **MOP_RAC3_x.x.x.x.zip.** Contains the MOP local contrast software and is upgradeable via USB (UPG). This SW is not part of the FUS autorun.upg!
- **OAD_Q5492_x.x.x.x.zip.** Not to be used by Service Technicians.
- **OpenSourceFile_Q5492_x.x.x.x.zip.** Not to be used by Service technicians.
- **PQPrivate_Q5492_x.x.x.x.zip.** Not to be used by Service technicians.
- **StandbySW_CFTxx_x.x.x.x_commercial.zip.** Contains the Stand-by software in "upg" and "hex" format.
  - The "StandbySW_xxxxx_prod.upg" file can be used to upgrade the Stand-by software via USB.
  - The "StandbySW_xxxxx.hex" file can be used to upgrade the Stand-by software via ComPair.

  - The files “StandbySW_xxxxx_exhex.hex” and “StandbySW_xxxxx_dev.upg” may not be used by Service technicians (only for development purposes).
- **UpgradeAll_Q5492_x.x.x.x_commercial.zip.** Only for production purposes, not to be used by Service technicians.
  Caution: Never try to use this file, because it will overwrite the HDCP keys ! ! !
- **UpgradeExe_Q5492X_x.x.x.x.zip.** Not to be used by Service Technicians.
- **Ambilight_Q5492_x.x.x.x.zip.** Not to be used by Service technicians.
- **Cabinet_Q5492_x.x.x.x.zip.** Not to be used by Service technicians.
- **Display_Q5492_x.x.x.x.zip.** Not to be used by Service technicians.
- **LightGuide_TV522_x.x.x.x_.zip.** Not to be used by Service Technicians.
- **ProcessNVM_Q5492_x.x.x.x.zip.** Default NVM content. Must be programmed via ComPair or can be loaded via USB, be aware that all alignments stored in NVM are overwritten here.

5.9.5 Content of the MOP Ambilight ARM SW File

- MOP_AMBILIGHT_V1-2_UPG_jettsigned.zip. Contains the MOP ambientlight software (ARM processor on the DC-DC AL interface board) and is upgradeable via USB (UPG). This SW is not part of the FUS autorun.upg! and is not available in the One-Zip software file but provided separately via the commercial Philips website (software for servicers only). Instructions for upgrading are included in the zip file.

5.9.6 UART logging 2K9 (see section “5.8 Fault Finding and Repair Tips, 5.8.6 Logging)

6. Alignments

Index of this chapter:

6.1 General Alignment Conditions
6.2 Hardware Alignments
6.3 Software Alignments
6.4 Option Settings
6.5 Reset of Repaired SSB
6.7 Total Overview SAM modes

6.1 General Alignment Conditions

Perform all electrical adjustments under the following conditions:

- Power supply voltage (depends on region):
  - **AP-NTSC:** 120 VAC or 230 V_{AC} / 50 Hz (± 10%).
  - **AP-PAL-multi:** 120 - 230 V_{AC} / 50 Hz (± 10%).
  - **EU:** 230 V_{AC} / 50 Hz (± 10%).
  - **LATAM-NTSC:** 120 - 230 V_{AC} / 50 Hz (± 10%).
  - **US:** 120 V_{AC} / 60 Hz (± 10%).
- Connect the set to the mains via an isolation transformer with low internal resistance.
- Allow the set to warm up for approximately 15 minutes.
- Measure voltages and waveforms in relation to correct ground (e.g. measure audio signals in relation to AUDIO_GND).
  Caution: It is not allowed to use heat sinks as ground.
- Test probe: Ri > 10 MΩ, Ci < 20 pF.
- Use an isolated trimmer/screwdriver to perform alignments.

6.1.1 Alignment Sequence

- First, set the correct options:
  - In SAM, select "Options", and then "Option numbers".
  - Fill in the option settings for "Group 1" and "Group 2" according to the set sticker (see also paragraph 6.4 Option Settings).
  - Press OK on the remote control before the cursor is moved to the left.
  - In submenu "Option numbers" select "Store" and press OK on the RC.
- OR:
  - In main menu, select "Store" again and press OK on the RC.
  - Switch the set to Stand-by.
- Warming up (>15 minutes).

6.2 Hardware Alignments

Not applicable.

6.3 Software Alignments

Put the set in SAM mode (see Chapter 5. Service Modes, Error Codes, and Fault Finding). The SAM menu will now appear on the screen. Select ALIGNMENTS and go to one of the sub menus. The alignments are explained below.
The following items can be aligned:

- Tuner AGC.
- White point.

To store the data:

- Press OK on the RC **before the cursor is moved to the left.**
- In main menu select "Store" and press OK on the RC.
- Press MENU on the RC to switch back to the main menu.
- Switch the set to stand-by mode.

For the next alignments, supply the following test signals via a video generator to the RF input:

- **EU/AP-PAL models:** a PAL B/G TV-signal with a signal strength of at least 1 mV and a frequency of 475.25 MHz
- **US/AP-NTSC models:** an NTSC M/N TV-signal with a signal strength of at least 1 mV and a frequency of 61.25 MHz (channel 3).
- **LATAM models:** an NTSC M TV-signal with a signal strength of at least 1 mV and a frequency of 61.25 MHz (channel 3).

6.3.1 Tuner AGC (RF AGC Take Over Point Adjustment)

Purpose: To keep the tuner output signal constant as the input signal amplitude varies.
No alignment is necessary, for the AGC alignment you can use the default value : "80".
Store settings and exit SAM.

6.3.2 White Point

- Set "Active control" to "Off".
- Choose "TV menu", "TV Settings" and then "Picture" and set picture settings as follows:

Picture Setting	
Dynamic backlight	Off
Dynamic Contrast	Off
Colour Enhancement	Off
Picture Format	Unscaled
Light Sensor	Off
Brightness	50
Colour	0
Contrast	100

- Go to the SAM and select "Alignments"-> "White point".

White point alignment LCD screens:

- Use a 100% white screen as input signal and set the following values:
  - "Colour temperature": "Normal".
  - All "White point" values to: "127".
  - "Red BL offset" values to "8".
  - "Green BL offset" values to "8".

In case you have a colour analyser:

- Measure with a calibrated contactless colour analyser in the centre of the screen. Consequently, the measurement needs to be done in a dark environment.
- Adjust the correct x,y coordinates (while holding one of the White point registers R, G or B on 127) by means of decreasing the value of one or two other white points to the correct x,y coordinates (see Table 6-1 White D alignment values). Tolerance: dx: ± 0.004, dy: ± 0.004.
- Repeat this step for the other colour temperatures that need to be aligned.
- When finished press OK on the RC and then press STORE (in the SAM root menu) to store the aligned values to the NVM.
- Restore the initial picture settings after the alignments.

Table 6-1 White D alignment values

Value	Cool (11000K)	Normal (9000K)	Warm (6500K)
x	0.270	0.279	0.309
y	0.279	0.287	0.328

If you do not have a colour analyser, you can use the default values. This is the next best solution. The default values are average values coming from production.

- Select a COLOUR TEMPERATURE (e.g. COOL, NORMAL, or WARM).

- Set the RED, GREEN and BLUE default values according to the values in Table 6-2.
- When finished press OK on the RC, then press STORE (in the SAM root menu) to store the aligned values to the NVM.
- Restore the initial picture settings after the alignments.

Table 6-2 White tone default setting

White Tone	32"			37"			Black level offset	
Colour Temp	**R**	**G**	**B**	**R**	**G**	**B**	**R**	**G**
Normal	127	95	97	127	121	106	8	8
Cool	127	100	112	124	127	119	8	8
Warm	127	89	52	127	111	64	8	8

White Tone	56"			Black level offset	
Colour Temp	**R**	**G**	**B**	**R**	**G**
Normal	127	117	111	8	8
Cool	124	124	125	8	8
Warm	127	95	65	8	8

6.4 Option Settings

6.4.1 Introduction

The microprocessor communicates with a large number of I2C ICs in the set. To ensure good communication and to make digital diagnosis possible, the microprocessor has to know which ICs to address. The presence / absence of these PNX5100 ICs (back-end advanced video picture improvement IC which offers motion estimation and compensation features (commercially called HDNM) plus integrated Ambilight control) is made known by the option codes.

Notes:

- After changing the option(s), save them by pressing the OK button on the RC before the cursor is moved to the left, select STORE in the SAM root menu and press OK on the RC.
- The new option setting is only active after the TV is switched "off" / "stand-by" and "on" again with the mains switch (the NVM is then read again).

6.4.2 Dealer Options

For dealer options, in SAM select "Dealer options".
See Table 6-4 SAM mode overview.

6.4.3 (Service) Options

Select the sub menu's to set the initialisation codes (options) of the model number via text menus.
See Table 6-4 SAM mode overview.

6.4.4 Opt. No. (Option numbers)

Select this sub menu to set all options at once (expressed in two long strings of numbers).
An option number (or "option byte") represents a number of different options. When you change these numbers directly, you can set all options very quickly. All options are controlled via eight option numbers.
When the NVM is replaced, all options will require resetting. To be certain that the factory settings are reproduced exactly, you must set both option number lines. You can find the correct option numbers on a sticker inside the TV set and in Table 6-3 Option and display code overview.
Example: The options sticker gives the following option numbers:

- 08192 00133 01387 45160
- 12232 04256 00164 00000

The first line (group 1) indicates hardware options 1 to 4, the second line (group 2) indicate software options 5 to 8.
Every 5-digit number represents 16 bits (so the maximum value will be 65536 if all options are set).
When all the correct options are set, the sum of the decimal values of each Option Byte (OB) will give the option number.
See Table 6-3 Option and display code overview for the options.

Diversity
Not all sets with the same Commercial Type Number (CTN) necessarily have the same option code!
Use of Alternative BOM => an alternative BOM number usually indicates the use of an alternative display or power supply. This results in another display code thus in another Option code. For the power supply there is no difference. Refer to Chapter 2. Technical Specifications and, Connections.

6.4.5 Option Code Overview

Table 6-3 Option and display code overview

CTN	Options Group 1	Options Group 2	Disp. code
32PFL9604H/12	08211 35971 18431 45288	30645 47282 00184 00000	181
32PFL9604H/60	08211 35971 18431 45288	30645 47282 00184 00000	181
37PFL9604H/12	08227 35972 18431 45288	30625 47282 00176 00000	161
37PFL9604H/60	08227 35972 18431 45288	30625 47282 00176 00000	161
56PFL9954H/12	08275 33925 18431 45288	30644 47282 00161 00000	180

Important: after having edited the option numbers as described above, you **must press OK** on the remote control **before the cursor is moved to the left**!

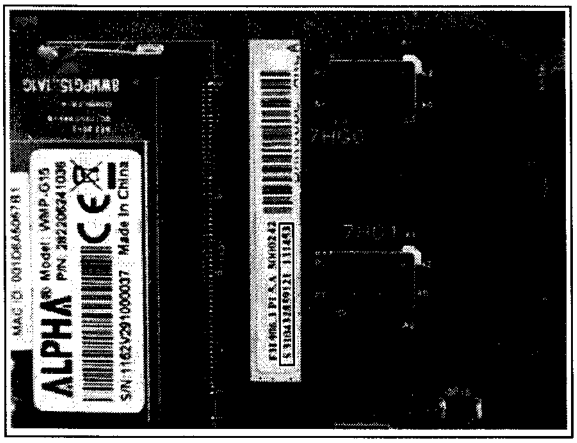
6.5 Reset of Repaired SSB

A very important issue towards a repaired SSB from a service repair shop implies the reset of the NVM on the SSB.
A repaired SSB in service should get the service Set type "00PF0000000000" and Production code "00000000000000".
Also the virgin bit is to be set. To set all this, you can use the ComPair tool.
In case of a display replacement, reset the "Operation hours display" to "0", or to the operation hours of the replacement display.

New here in this chassis is the "Net TV" functionality. Therefore the CTN ("set type" item in CSM1) must be filled into the spare SSB to ensure access to the Net TV portals.
The loading of the CTN can be done via ComPair (Model number programming).
The reset item (Clear NET TV memory) can be selected via MENU (or HOME) => Setup => Installation => Clear NET TV memory (customer preferences stored at provider side will be reset now).

6.5.1 SSB identification

Whenever ordering a new SSB, it should be noted that the correct ordering number (12nc) of a SSB is located on a sticker on the SSB. The format is <12nc SSB><serial number>. The ordering number of a “Service” SSB is the same as the ordering number of an initial “factory” SSB.



18310_221_090318.eps
090319

Figure 6-1 SSB identification

6.6 Service SSB delivered without main software loaded

Due to a changed manufacturing process, new **Service SSB’s can be delivered** to the warehouse **without main TV software** loaded. Below you find the steps to follow when such an SSB is received.

6.6.1 When a picture is available

1. Mount the Service SSB into the TV set. After start-up, normally the download application will appear on the screen.
2. Download the latest main software (FUS) from the www.p4c.philips.com website.
3. Create a folder "upgrades" in the root of a USB stick (size > 50 MB) and save the "autorun.upg" file in this "upgrades" folder. **Note:** it is possible to rename this file, e.g. "Q549_SW_version.upg", this in case there are more than one "autorun.upg" files on your USB stick
4. Plug the prepared USB stick into the TV set, and select the "autorun" file in the displayed browser on the screen
5. Now the main TV software will be loaded automatically, supported by a progress bar
6. Set the correct "display code" via "062598-HOME-xxx", where "xxx" is the 3-digit display panel code (see sticker on the side/bottom of the cabinet).

6.6.2 When no picture is available

Due to a possible wrong display option code in the received Service SSB (NVM), no picture can be available at start-up and thus no download application will be visible. Here you can proceed and finalize step by step to load the main TV software via the UART logging on the PC (for visual feedback).

1. Start-up the TV set, equipped with the Service SSB, and enable the UART logging on the PC (see for settings 5.8 Fault Finding and Repair Tips 5.8.6 Logging)
2. The TV set will start-up automatically in the download application if main TV software is not loaded
3. Plug the prepared USB stick into the TV set, press cursor "Right" to enter the list, and navigate to the "autorun" file in the UART logging printout via the cursor keys on the remote control. When the correct file is selected, press "OK"
4. Press cursor "Down" and "OK" to start the flashing of the main TV software. Printouts like: "L: 1-100% , V: 1-100% and P: 1-100%" should be visible now in the UART logging
5. Wait until the message "Operation successful!" is displayed and remove all inserted media. Restart the TV set
6. Set the correct "display code" via "062598-HOME-xxx", where "xxx" is the 3-digit display panel code (see sticker on the side/bottom of the cabinet).

6.6.3 Use of repaired SSBs instead of new

Repaired SSBs on stock will obviously already contain main TV software. This implies that only a main software upgrade is required if you use a “repaired” SSB for board swap instead of a “new” SSB.

6.7 Total Overview SAM modes

Table 6-4 SAM mode overview

Main Menu	Sub-menu 1	Sub-menu 2	Sub-menu 3	Description
Hardware Info	A. SW VERSION	e.g. “Q5492_1.26.15.0”		Display TV & Standby SW version and CTN serial number.
	B. Standby processor version	e.g. “STDBY_88.68.0.0”		
	C. Production code	e.g. “See type plate”		
Operation hours				Displays the accumulated total of operation hours.TV switched “on/off” & every 0.5 hours is increase one
Error				Displayed the most recent errors.
Reset error buffer				Clears all content in the error buffer.
Alignment	Tuner AGC			RF-AGC Take over point adjustment (AGC default value is 80)
	Whitepoint	Colour temperature	Normal	3 different modes of colour temperature can be selected
			Warm	
			Cool	
		White point red		LCD White Point Alignment. For values, see Table 6-1 White D alignment values.
		White point green		
		White point blue		
		Red black level offset		
		Green black level offset		

Main Menu	Sub-menu 1	Sub-menu 2	Sub-menu 3	Description
Dealer options	Picture mute	Off/On		Select Picture mute On/Off. Picture is muted / not muted in case no input signal is detected at input connectors.
	Virgin mode	Off/On		Select Virgin mode On/Off. TV starts up / does not start up (once) with a language selection menu after the mains switch is turned "on" for the first time (virgin mode)
	E-sticker	Off/On		Select E-sticker On/Off (USP's on-screen)
	Auto store mode	None		
		PDC/VPS		
		TXT page		
		PDC/VPS/TXT		
Options	Digital broadcast	DVB	Off/On	Select DVB On/Off
		DVB - T installation	Off/On or Country dependent	Select DVB T installation On/Off or by country
		DVB - T light	Off/On	Select DVB T light On/Off
		DVB - C	Off/On	Select DVB C On/Off
		DVB - C installation	Off/On or Country dependent	Select DVB C installation On/Off or by country
		Over the air download	Off/On or Country dependent	Select Over the air download On/Off or by country
		8 days EPG	Off/On	Select 8 day EPG On/Off
	Digital features	USB	Off/On	Select USB On/Off
		Ethernet	Off/On	Select Ethernet On/Off
		Wi-Fi	Off/On	Select Wi-Fi On/Off
		DLNA	Off/On	Select DLNA On/Off
		Online service	Off	Online service is Off
		PTP (Picture Transfer Protocol)	Off/On	Select PTP On/Off
		Update assistant	Off/On	Select Update assistant On/Off
		Internet software update	Off	Internet software update is Off
	Display	Screen	180 / LCD Sharp Z3LA13 56"	Displayed the panel code & type model.
		LightGuide	Off/On	Select LightGuide On/Off
		Display fans	Not present/Present	Select Display fans Present/Not present.
		Temperature sensor	Sensor present in display (only for 21:9)	N.A.
		Temperature LUT	0	N.A
		E-box & monitor	Off/On	Select E-box & monitor On/Off
	Video reproduction	Picture processing	None/PNX5100	Select Picture processing None/PNX5100 (Q549.xE chassis).
		MOP local contrast	Off/On	Select MOP local contrast On/Off
		Light sensor	Off/On	Select Light sensor On/Off
		Light sensor type	0/1/2/3	Select Light sensor type form 0 to 3 (for difference styling).
		Pixel Plus type	Pixel Plus HD	Select type of picture improvement.
			Perfect Pixel HD	
			Pixel Precise HD	
		Ambilight	None,	Select type of Ambilight modules use.
			2 sided 2/2	For 8400 series only
			2 sided 4/4	
			3 sided 2/3/2	
			3 sided 4/3/4	
			3 sided 4/5/4	
			4 sided 4/3/4/3	
		Ambilight technology	LED/Future use	Ambilight technology LED is in use.
		MOP ambilight	Off/On	Select MOP ambilight On/Off

Main Menu	Sub-menu 1	Sub-menu 2	Sub-menu 3	Description
	Audio reproduction	Acoustic system		Cabinet design used for setting dynamic audio parameters.
	Source selection	EXT1/AV1 type	SCART CVBS RGB LR	Select input source when connected with external equipment.
			CVBS Y/C YPbPr LR	
			CVBS Y/C YPbPr HV LR	
			(CVBS) YPbPr LR	
		EXT2/AV2 type	SCART CVBS RGB LR	Select input source when connected with external equipment.
			CVBS Y/C LR	
			(CVBS) YPbPr LR	
			CVBS Y/C LR	
		EXT3/AV3 type	None	Select input source when connected with external equipment.
			CVBS	
			CVBS LR	
			YPbPr	
			YPbPr LR	
			YPbPr HV LR	
		VGA	Off/On	Select VGA On/Off
		SIDE I/O	Off/On	Select SIDE I/O On/Off
		HDMI 1	Off/On	Select HDMI 1 On/Off
		HDMI 2	Off/On	Select HDMI 2 On/Off
		HDMI 3	Off/On	Select HDMI 3 On/Off
		HDMI 4	Off/On	Select HDMI 4 On/Off
		HDMI side	Off/On	Select HDMI side On/Off
		HDMI CEC	Off/On	Select HDMI CEC On/Off
		HDMI CEC RC passthrough	Off/On	Select HDMI CEC RC passthrough On/Off
		HDMI CEC Pixel Plus link	Off/On	Select Pixel Plus link On/Off
	Miscellaneous	Region	Europe/AP-PAL-MULTI/Australia	Select Region/country.
		Tuner type	HD1816-MK1/TD1716-MK4/ TD1716-MK3/HD1816-MK2	Select type of Tuner used.
		System RC support	Off/On	Select System RC support On/Off.
		Embedded user manual	Off/On	Select Embedded user manual On/Off.
		Start-up screen	Off/On	Select Start-up screen On/Off.
		Wallpaper	Off/On	Select Wallpaper On/Off.
		Hotel mode	Off	Hotel mode is Off.
Option number	Group 1	e.g. "08192.02181.01387.45160"		The first line (group 1) indicates hardware options 1 to 4.
	Group 2	e.g. "10185.12448.00164.00000"		The second line (group 2) indicates software options 5 to 8.
	Store			Store after changing.
Initialise NVM				N.A
Store				Select Store in the SAM root menu after making **any** changes.
Software maintenance	Software events	Display		Display information is for development purposes.
		Clear		
		Test reboot		
	Hardware events	Display		Display information is for development purposes.
		Clear		
Operation hours display		0003		In case the display must be swapped for repair, you can reset the ""Display operation hours"" to ""0"". So, this one does keeps up the lifetime of the display itself (mainly to compensate the degeneration behaviour).
Test setting	Digital info	QAM modulation: 64-QAM		Display information is for development purposes.
		Symbol rate: 23:29		
		Original network ID: 12817		
		Network ID:12817		
		Transportstream ID: 2		
		Service ID: 3		
		Hierarchical modulation: 0		
		Selected video PID: 35		
		Selected main audio PID: 99		
		Selected 2nd audio PID: -1		
	Install start frequency	000		Install start frequency from "0" MHz
	Install end frequency	999		Install end frequency as 999 MHz
	Default install frequency			
	Installation	Digital only		Select Digital only or Digital + Analogue before installation.
		Digital + Analogue		

Main Menu	Sub-menu 1	Sub-menu 2	Sub-menu 3	Description
Development file versions	Development 1 file version	Display parameters DISPT 3.26.8.7		Display information is for development purposes.
		Acoustics parameters ACSTS 3.6.6.5		
		PQ - PRFPP 1.26.10.4		
		Ambilight parameters PRFAM 2.6.1.3		
	Development 2 file version	12NC one zip software		Display information is for development purposes.
		Initial main software		
		NVM version Q5492_0.4.0.0		
		Flash units SW Q5492_0.26.15.0		
Upload to USB	Channel list			To upload several settings from the TV to an USB stick
	Personal settings			
	Option codes			
	Display-related alignment			
	History list			
Download from USB	Channel list			To download several settings from the USB stick to the TV.
	Personal settings			
	Option codes			
	Display-related alignment			

7. Circuit Descriptions

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7.1 Introduction
7.2 Power Architecture
7.3 Front-End
7.4 HDMI
7.5 Video and Audio Processing - PNX8543
7.6 Common Interface CI+
7.7 Net TV
7.8 Ambi Light

Notes:

- Only **new** circuits (circuits that are not published recently) are described.
- Figures can deviate slightly from the actual situation, due to different set executions.
- For a good understanding of the following circuit descriptions, please use the wiring, block (see chapter 9. Block Diagrams) and circuit diagrams (see chapter 10. Circuit Diagrams and PWB Layouts).Where necessary, you will find a separate drawing for clarification.

7.1 Introduction

The Q549.2E LA chassis (platform name TV543/92) is the successor of the Q529.1E LA chassis (platform TV522/92).

Main difference with the previous platform is the introduction of “Net TV” and “CI+”.

7.1.1 Implementation

Key components of this chassis are:

- PNX8543 Digital Colour Decoder
- EP3C25F324C7N FPGA (“Local Contrast”)
- HD1816AF Hybrid Tuner
- DRX3926K Demodulator
- TDA9996 HDMI Switch
- TPA3123D2PWP Class D Power Amplifier
- DP83816AVNG PCI ethernet media access controller and physical layer (MacPhyter-II).

7.1.2 TV543 Architecture Overview

- For details about the chassis block diagrams refer to chapter 9. Block Diagrams. An overview of the TV543 architecture can be found in Figure 7-1.

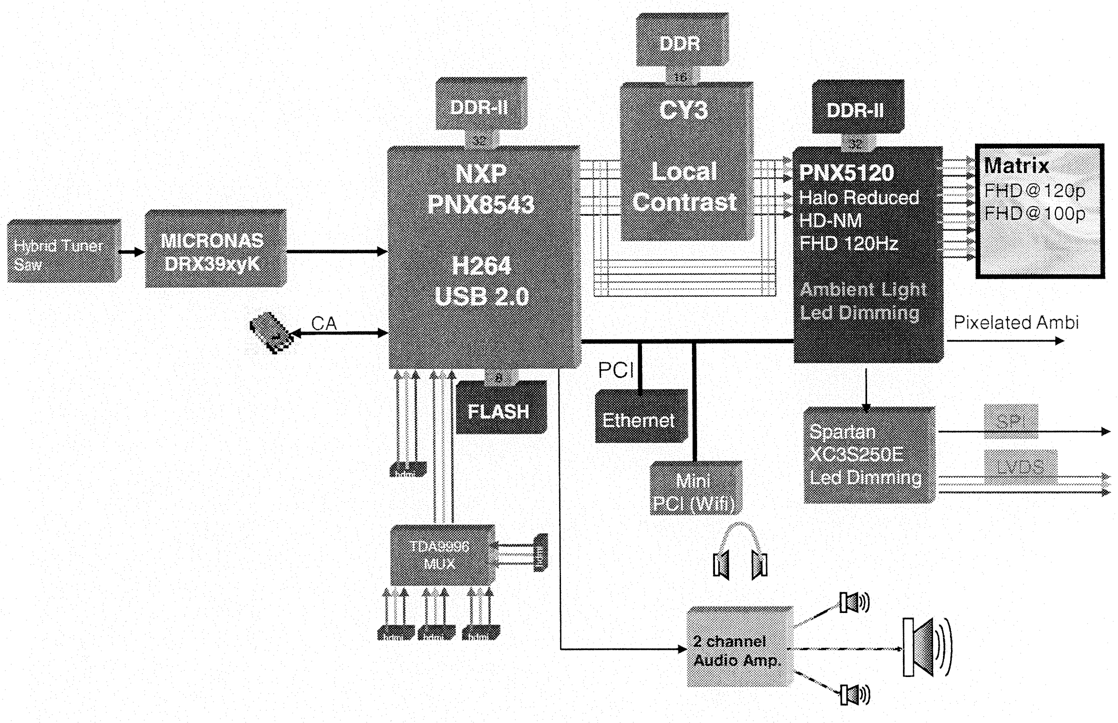
DDR
16
DDR-II
32
CY3
Local Contrast
DDR-II
32
NXP PNX8543
H264
USB 2.0
PNX5120
Halo Reduced
HD-NM
FHD 120Hz
Ambient Light
Led Dimming
Matrix
FHD@120p
FHD@100p
Hybrid Tuner
Saw
MICRONAS
DRX39xyK
CA
Pixelated Ambi
PCI
8
FLASH
Ethernet
hdmi
Mini
PCI (Wifi)
Spartan
XC3S250E
Led Dimming
SPI
LVDS
TDA9996
MUX
hdmi
hdmi
hdmi
hdmi
2 channel
Audio Amp.

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Figure 7-1 Architecture of TV543/92 Elite Core platform

7.1.3 SSB Cell Layout

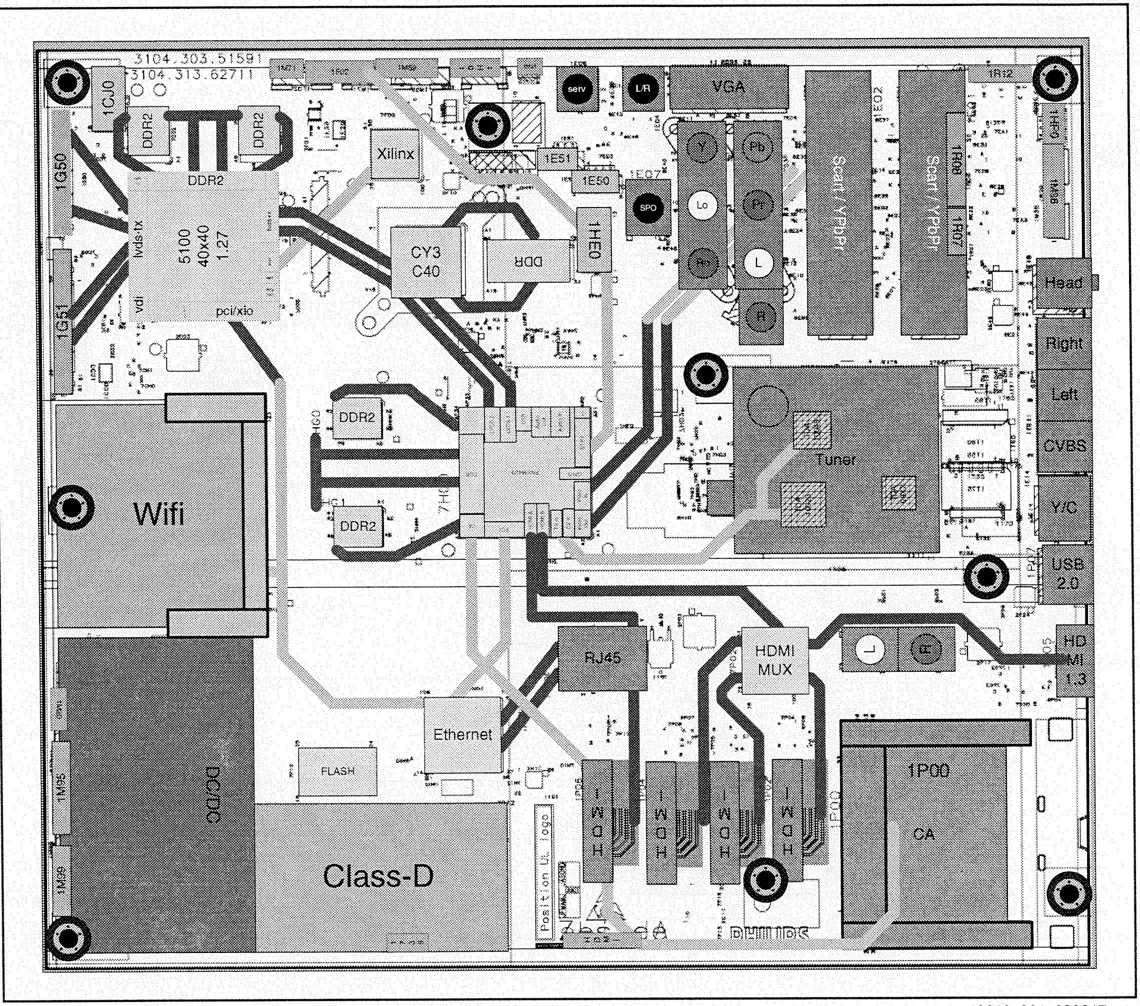
3104.303.51591
3104.313.62711
1CJ0
DDR2
DDR2
1G50
1G51
DDR2
lvds-tx
5100
40x40
1.27
vdi
pci/xio
Xilinx
1E51
1E50
CY3
C40
DDR
1HE0
serv
L/R
VGA
Y
Pb
Pr
Lo
L
Ro
R
SPD
Scart / YPbPr
Scart / YPbPr
1R08
1R07
1R12
1HF0
1M98
Head
Right
Left
CVBS
Y/C
USB
2.0
HD
MI
1.3
Tuner
DDR2
DDR2
7HC0
Wifi
RJ45
HDMI
MUX
L
R
Ethernet
FLASH
DC/DC
1M95
1M99
Class-D
Position UL logo
HDMI
HDMI
HDMI
HDMI
1P00
CA
PHILIPS

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Figure 7-2 SSB layout cells (top view)

7.2 Power Architecture

Refer to figure Figure 7-3 for the power architecture of this platform.

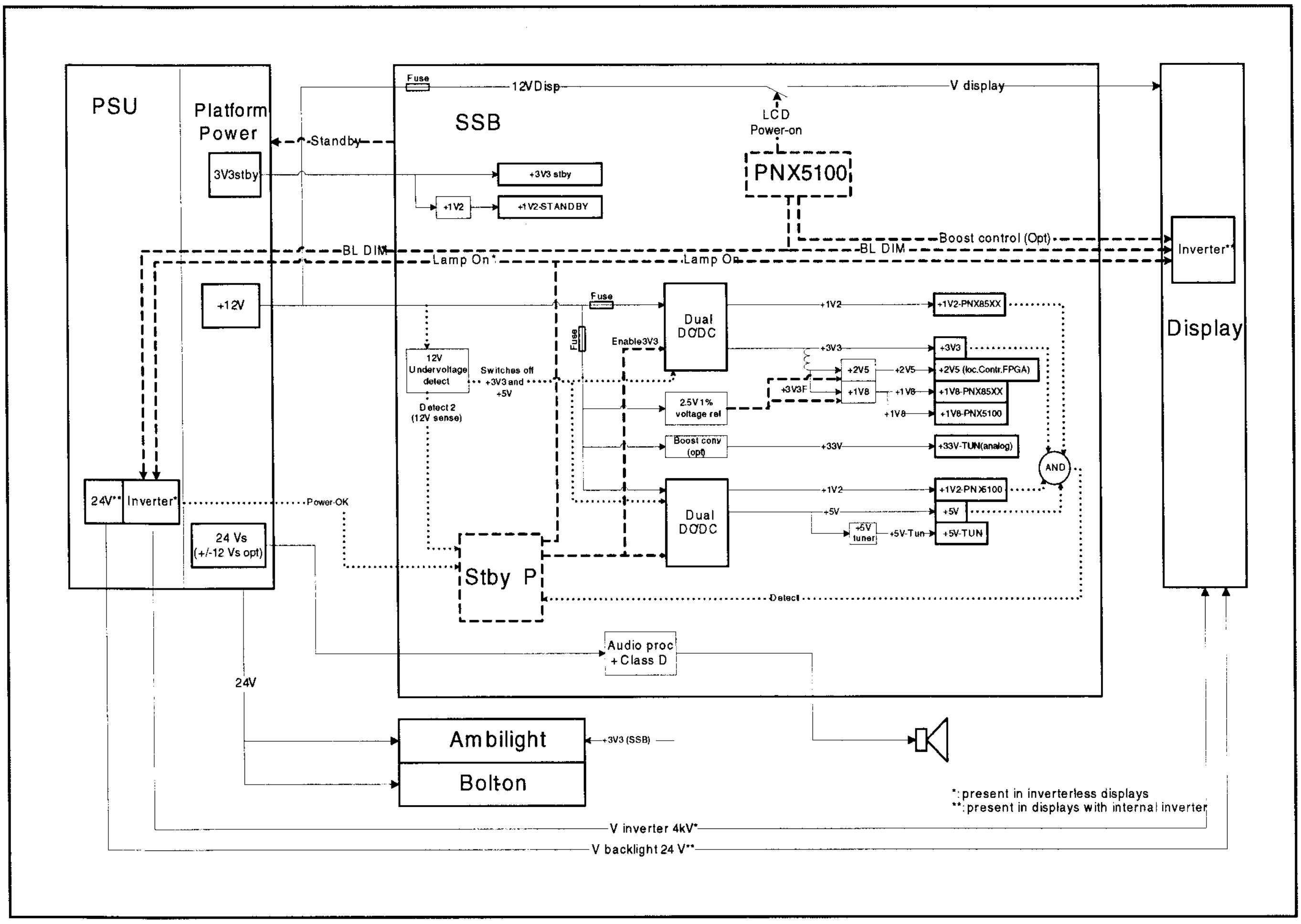
PSU
Platform Power
3V3stby
+12V
24V**
Inverter*
24 Vs (+/-12 Vs opt)
Standby
BL DIM
Lamp On*
Power-OK
SSB
Fuse
12VDisp
V display
LCD Power-on
PNX5100
+3V3 stby
+1V2
+1V2-STANDBY
Boost control (Opt)
BL DIM
Lamp On
Inverter**
Display
Fuse
Dual DC/DC
Fuse
Enable3V3
12V Undervoltage detect
Switches off +3V3 and +5V
Detect 2 (12V sense)
+1V2
+1V2-PNX85XX
+3V3
+3V3
+2V5
+2V5
+2V5 (loc.Contr.FPGA)
+3V3F
+1V8
+1V8
+1V8-PNX85XX
+1V8
+1V8-PNX5100
2.5V 1% voltage ref
Boost conv (opt)
+33V
+33V-TUN(analog)
AND
Dual DC/DC
+1V2
+1V2-PNX5100
+5V
+5V
+5V tuner
+5V-Tun
+5V-TUN
Stby P
Detect
Audio proc + Class D
24V
Ambilight
+3V3 (SSB)
Bolt-on
*: present in inverterless displays
**: present in displays with internal inverter
V inverter 4kV*
V backlight 24 V**

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Figure 7-3 Power Architecture TV543/92 platform

7.2.1 Power Supply Unit

All power supplies are a black box for Service. When defective, a new board must be ordered and the defective one must be returned, unless the main fuse of the board is broken. Always replace a defective fuse with one with the correct specifications! This part is available in the regular market. Consult the Service website for the order codes of the boards.

In the TV543 Elite Core platform, for sets up to and including 47", the Integrated Power Board (IPB) - incl. inverter is used. For sets of 52 " and 56", a conventional PSU (with additional inverters) is used.

In this manual, no detailed information is available because of design protection issues.

The output voltages to the chassis are:

- +3V3-STANDBY (standby-mode only)
- +12V (on-mode)
- +Vsnd (+24V) (audio power) (on-mode)
- +24V (bolt-on power) (on-mode)
- IPB: High voltage to the LCD panel (for sets up to and including 47").

7.2.2 Diversity

Below find an overview of the different PSUs that are used:

Table 7-1 Supply diversity

Supplier	PSU	Model	Input Voltage Range
LGIT	PLHL-T826A	32"	High Mains (198- 265 Vac)
Delta	DPS-298CP A	37"	High Mains (198- 265 Vac)
Delta	DPS-411AP-3 A	56"	High Mains (198- 265 Vac)

7.3 Front-End

The Front-End consist of the following key components:

- Tuner HD1816AF
- SAW filter 36M125
- IF demodulator DRX3926K
- AGC amplifier UPC3221GV.

Below find a block diagram of the front-end application.

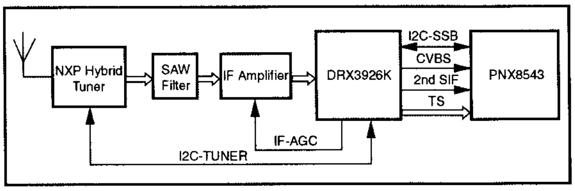
NXP Hybrid Tuner
SAW Filter
IF Amplifier
DRX3926K
I2C-SSB
CVBS
2nd SIF
TS
PNX8543
IF-AGC
I2C-TUNER

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Figure 7-4 Front-End block diagram

The DRX3926K is a multi-standard demodulator supporting DVB-C, DVB-T and analogue standards. The demodulated digital stream is fed into the parallel transport stream data ports of the PNX8543. The demodulated analogue signal in the form of CVBS is connected to the analogue video CVBS/Y input channel, while the SIF is connected via the SSIF2 positive input port.

7.4 HDMI

In this platform, the TDA9996 HDMI multiplexer is implemented. Only for one HDMI input, a separate EEPROM is implemented to store the EDID values. For the other HDMI inputs, the EDID contents are no longer stored in a separate EEPROM, but directly in the multiplexer. Each input has its own physical subaddress: the first 253 bytes are common, where the last 3 bytes define the specific input. The EDID contents are, at +5V power-up, downloaded to RAM. The following figures show the HDMI input configuration and EDID control.

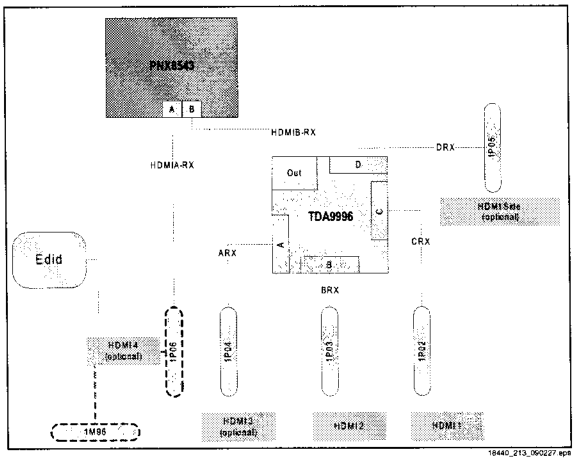
PNX8543
A
B
HDMIB-RX
HDMIA-RX
DRX
1P05
Out
D
TDA9996
C
A
B
HDMI Side (optional)
Edid
ARX
CRX
BRX
HDMI4 (optional)
1P06
1P04
1P03
1P02
1M96
HDMI3 (optional)
HDMI2
HDMI1

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Figure 7-5 HDMI input configuration

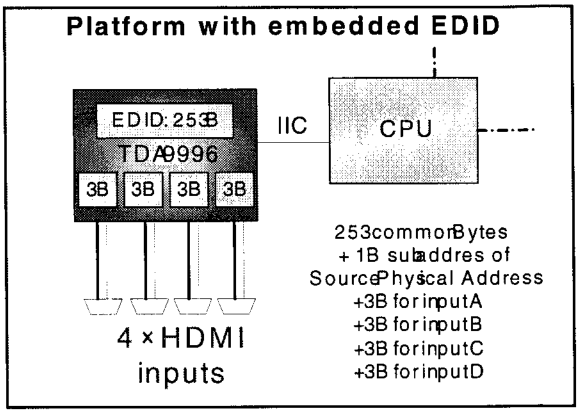
Platform with embedded EDID
EDID: 253B
TDA9996
3B
3B
3B
3B
IIC
CPU
253 common Bytes
+ 1B subaddres of
Source Physical Address
+3B for input A
+3B for input B
+3B for input C
+3B for input D
4 × HDMI
inputs

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Figure 7-6 EDID control (embedded EDID)

The delta's with respect to the use of the TDA9996 as HDMI multiplexer compared with earlier chassis/platforms are:

- +5V detection mechanism
- Stable clock detection mechanism
- Integrated EDID
- RT control
- HPD control
- TMDS output control
- CEC control
- New hotplug control for PNX8543 for 5th HDMI input
- New EDID structure: EDID stored in TDA9996, therefore there are no EDID pins on the SSB. Only in the event of a 5th HDMI input, an additional EEPROM is foreseen, as was implemented in previous platforms.

After replacement of the TDA9996 HDMI mux, the default I^2C address should be reprogrammed from C0 to CE, and the HDMI EDIDs should be reprogrammed as well. Both actions should be executed via ComPair.

7.5 Video and Audio Processing - PNX8543

The PNX8543 is the main audio and video processor (or System-on-Chip) for this platform. It is a member of the PNX85xx SoC family (described in earlier chassis) with the addition of the MPEG4 functionality; the separate STi710x MPEG4 decoder is no longer implemented in this platform.

Some more delta's compared to the previous PNX85xx are:

- 2 HDMI inputs (A & B)
- HDMI deep colour RGB/YCbCr 4:4:1 10/12 bit detection.

The PNX8543 handles the digital and analogue audio- and video decoding and processing. The processor is a MIPS32 general purpose CPU and a 8051-based TV controller for power management and user event handling.

- For a functional diagram of the PNX8543, refer to Figure 7-7.

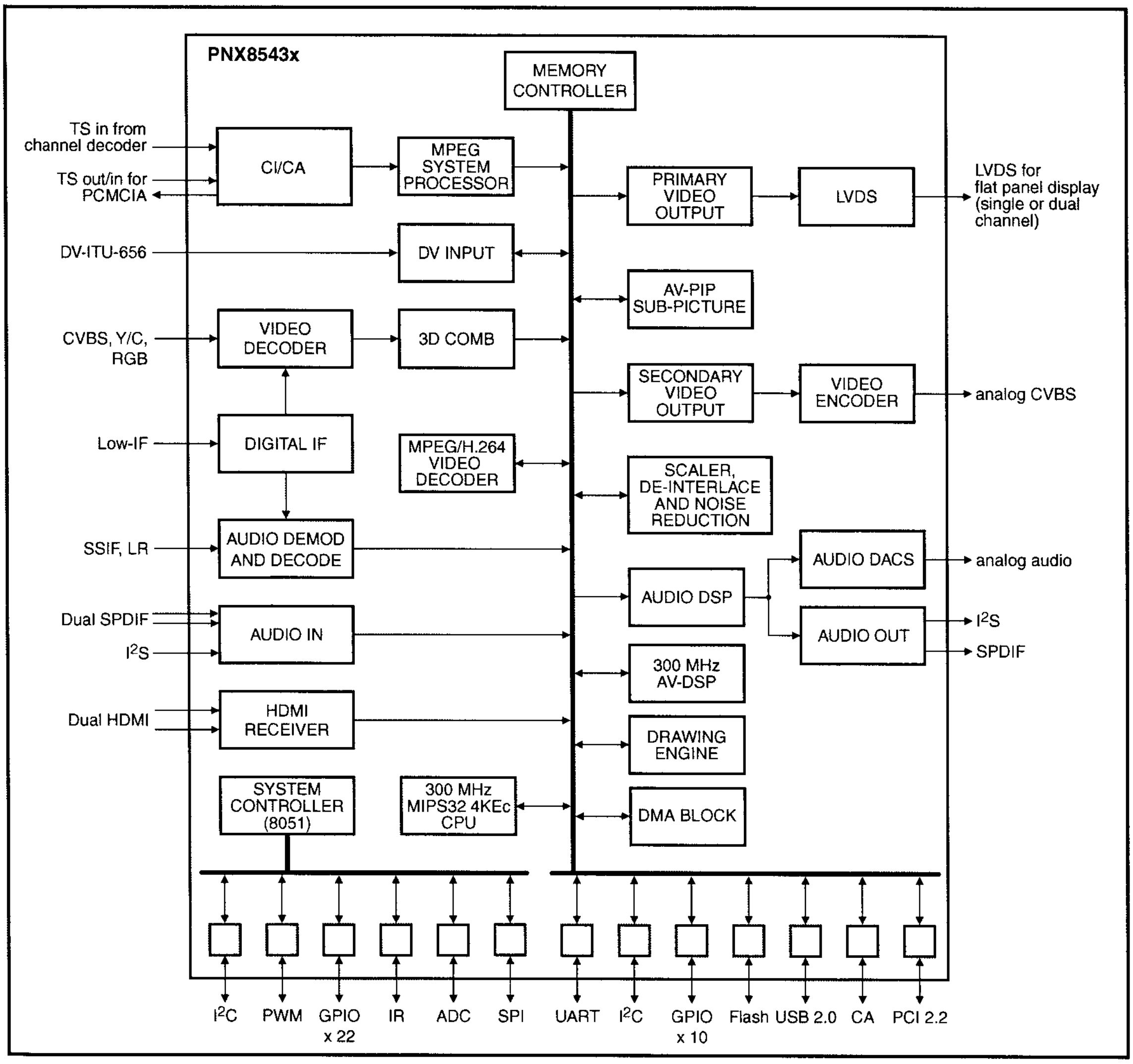
PNX8543x
MEMORY CONTROLLER
TS in from channel decoder
TS out/in for PCMCIA
CI/CA
MPEG SYSTEM PROCESSOR
PRIMARY VIDEO OUTPUT
LVDS
LVDS for flat panel display (single or dual channel)
DV-ITU-656
DV INPUT
AV-PIP SUB-PICTURE
CVBS, Y/C, RGB
VIDEO DECODER
3D COMB
SECONDARY VIDEO OUTPUT
VIDEO ENCODER
analog CVBS
Low-IF
DIGITAL IF
MPEG/H.264 VIDEO DECODER
SCALER, DE-INTERLACE AND NOISE REDUCTION
SSIF, LR
AUDIO DEMOD AND DECODE
AUDIO DACS
analog audio
AUDIO DSP
Dual SPDIF
I²S
AUDIO IN
AUDIO OUT
I²S
SPDIF
300 MHz AV-DSP
Dual HDMI
HDMI RECEIVER
DRAWING ENGINE
SYSTEM CONTROLLER (8051)
300 MHz MIPS32 4KEc CPU
DMA BLOCK
I²C
PWM
GPIO x 22
IR
ADC
SPI
UART
I²C
GPIO x 10
Flash
USB 2.0
CA
PCI 2.2

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Figure 7-7 PNX8543 functional diagram

7.5.1 Video Subsystem

Refer to Figure 7-8 for the main video interfaces for the PNX8543 and the video signal flow between blocks and memory.

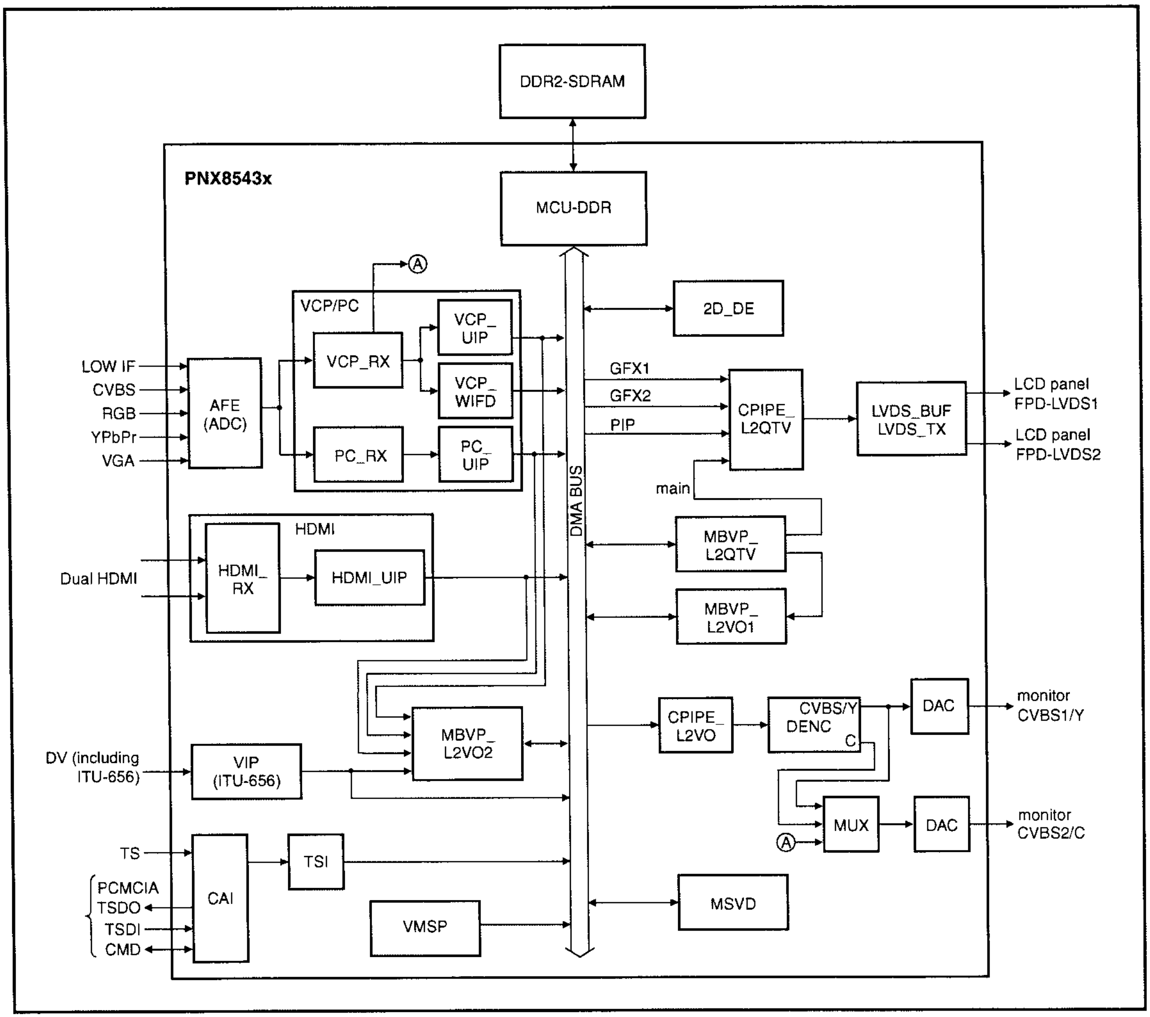
DDR2-SDRAM
PNX8543x
MCU-DDR
A
VCP/PC
VCP_UIP
VCP_RX
VCP_WIFD
PC_RX
PC_UIP
2D_DE
GFX1
GFX2
PIP
CPIPE_L2QTV
LVDS_BUF
LVDS_TX
LCD panel FPD-LVDS1
LCD panel FPD-LVDS2
main
DMA BUS
LOW IF
CVBS
RGB
YPbPr
VGA
AFE (ADC)
HDMI
HDMI_RX
HDMI_UIP
Dual HDMI
MBVP_L2QTV
MBVP_L2VO1
MBVP_L2VO2
CPIPE_L2VO
CVBS/Y DENC
C
DAC
monitor CVBS1/Y
MUX
DAC
monitor CVBS2/C
DV (including ITU-656)
VIP (ITU-656)
TS
PCMCIA
TSDO
TSDI
CMD
CAI
TSI
VMSP
MSVD

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Figure 7-8 PNX8543 video flow diagram

The Video Subsystem consist of the following blocks:

- Analogue Front-End (AFE) block
- Video and PC Capture (VPC/PC) pipe
- HDMI Receiver interface
- Memory-Based Video Processor MBVP)
- Video Composition Pipe (CPIPE)
- Memory Based Video Processor (MBVP) VO-1
- Memory Based Video Processor (MBVP) VO-2
- Video Composition Pipe (CPIPE)
- Dual Flat Panel Display-LVDS (FPD-LVDS)
- Digital Encoder (DENC)
- Digital Video VIP
- 2D graphics block.

7.5.2 Audio Subsystem

Refer to Figure 7-9 for the main audio interfaces for the PNX8543 and the audio signal flow between blocks and memory.

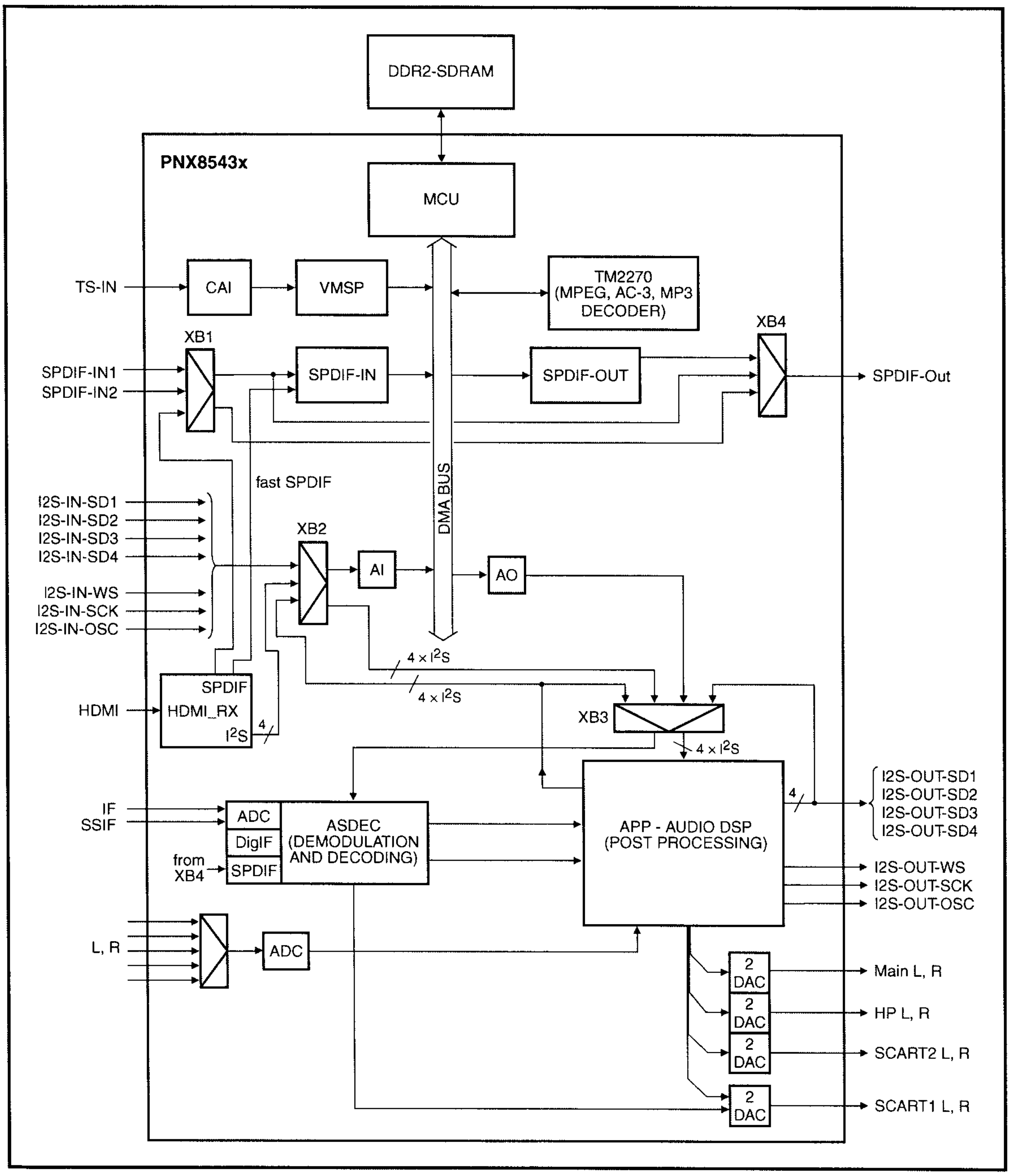
DDR2-SDRAM
PNX8543x
MCU
TS-IN
CAI
VMSP
TM2270 (MPEG, AC-3, MP3 DECODER)
XB1
XB4
SPDIF-IN1
SPDIF-IN2
SPDIF-IN
SPDIF-OUT
SPDIF-Out
fast SPDIF
DMA BUS
I2S-IN-SD1
I2S-IN-SD2
I2S-IN-SD3
I2S-IN-SD4
I2S-IN-WS
I2S-IN-SCK
I2S-IN-OSC
XB2
AI
AO
4 x I²S
4 x I²S
HDMI
SPDIF
HDMI_RX
I²S
4
XB3
4 x I²S
IF
SSIF
ADC
DigIF
SPDIF
from XB4
ASDEC (DEMODULATION AND DECODING)
APP - AUDIO DSP (POST PROCESSING)
4
I2S-OUT-SD1
I2S-OUT-SD2
I2S-OUT-SD3
I2S-OUT-SD4
I2S-OUT-WS
I2S-OUT-SCK
I2S-OUT-OSC
L, R
ADC
2 DAC
2 DAC
2 DAC
2 DAC
Main L, R
HP L, R
SCART2 L, R
SCART1 L, R

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Figure 7-9 PNX8543 audio flow diagram

The Audio Subsystem consist of the following blocks:

- Analogue Audio Front End (AAFE) used to capture Baseband Audio Inputs and to sample Secondary Sound IF (SSIF) directly or via Low-IF input
- HDMI Receiver interface block
- SPDIF input block
- Audio Input (AI) block
- Audio Output (AO) block
- Demodulation & Decoding (ASDEC) DSP for decoding all analogue terrestrial TV sound standards
- Audio Post-Processing (APP) block
- Digital Audio decoder.

7.5.3 Connectivity and Compute Subsystem

Refer to Figure 7-10 for the connectivity and compute subsystem.

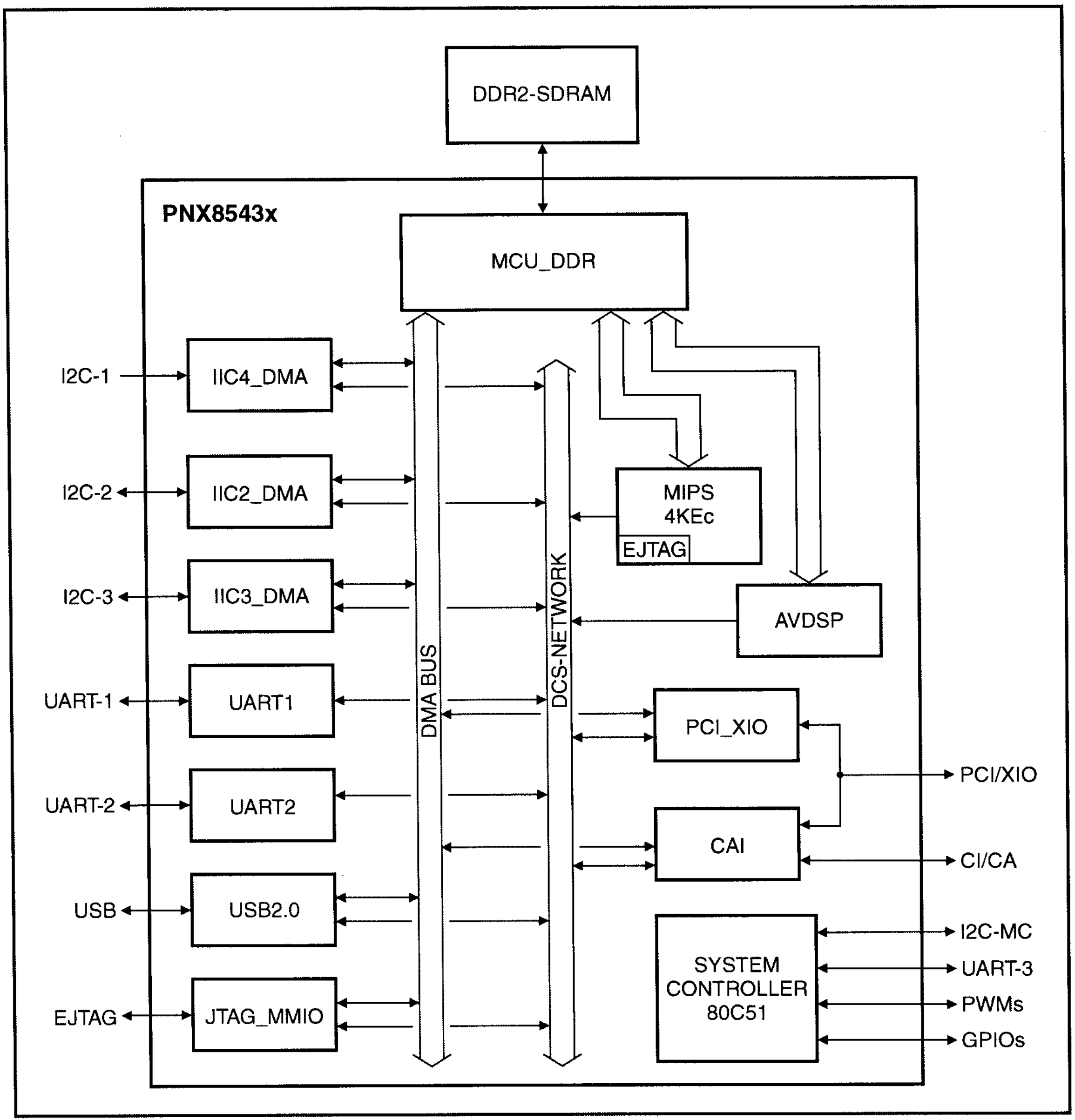
DDR2-SDRAM
PNX8543x
MCU_DDR
I2C-1
IIC4_DMA
I2C-2
IIC2_DMA
I2C-3
IIC3_DMA
UART-1
UART1
UART-2
UART2
USB
USB2.0
EJTAG
JTAG_MMIO
DMA BUS
DCS-NETWORK
MIPS
4KEc
EJTAG
AVDSP
PCI_XIO
CAI
SYSTEM
CONTROLLER
80C51
PCI/XIO
CI/CA
I2C-MC
UART-3
PWMs
GPIOs

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Figure 7-10 PNX8543 connectivity and compute subsystem

The Connectivity Subsystem consists of:
- PCI/XIO interface
- USB2.0 interface
- Three 2-wire UARTs
- Four Master/Slave I^2C interfaces
- Common Interface/Conditional Access Interface.

The Computing Subsystem consists of:
- 32-bit MIPS RISC core
- Enhanced JTAG (EJTAG) block inside the MIPS
- JTAG_MMIO blocks
- TV controller
- Audio/Video DSP (AV_DSP)
- Memory Control Unit (MCU).

7.5.4 Service Notice - FLASH RAM / PNX8543 exchange

The FLASH RAM (item 7P10) and/or PNX8543 (item 7H00) can only be exchanged by an authorised central workshop with dedicated programming tools. Due to the presence of (CI+) keys in the components, **unauthorised exchange of these components will always result in a defective board.**

7.6 Common Interface CI+

Together with this platform, an extention to the Common Interface (CI) Conditional Access system is added, called CI+.

CI+ or Common Interface Plus is a specification that extends the Common Interface (DVB-CI) as described in the digital broadcasting standard DVB.

The weakness of the conventional CI module as Conditional Access system was the absence of a Copy Protection mechanism, as decrypted content could be sent over the PCMCIA interface unscrambled. With the CI+ extension, a form of copy protection is established between the Conditional Access Module (CAM) and the Integrated Digital Television (IDTV). The security mechanisms in CI+ are derived/copied from POD (with the exception of Out Of Band (OOB) used in US CA systems). For more information about conventional CA systems using a CI module, refer to the BJ3.0E L/PA or BL2.xU Service Manual.

The CI+ standard is downwards compatible with the existing CI standard.

The following figure shows the implementation of the CI+ Conditional Access system in the TV543 platform.

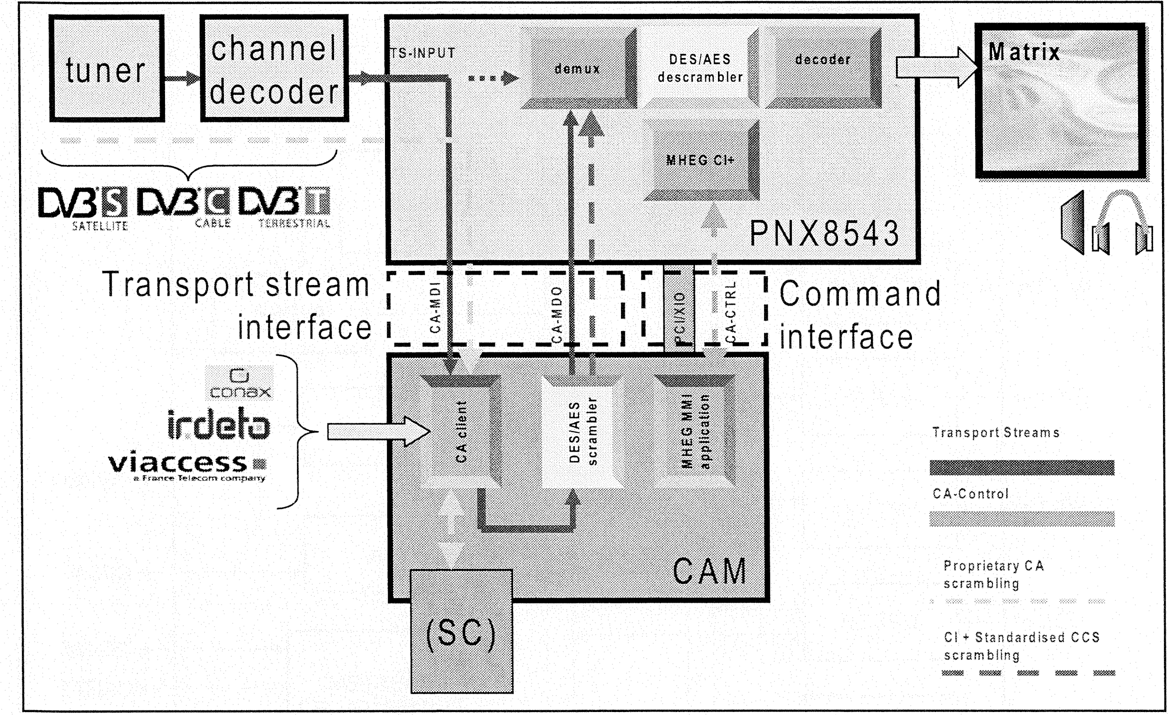
tuner
channel decoder
DVB S SATELLITE
DVB C CABLE
DVB T TERRESTRIAL
TS-INPUT
demux
DES/AES descrambler
decoder
MHEG CI+
PNX8543
Matrix
Transport stream interface
CA-MDI
CA-MDO
PCI/XIO
CA-CTRL
Command interface
conax
irdeto
viaccess
a France Telecom company
CA client
DES/AES scrambler
MHEG MMI application
CAM
(SC)
Transport Streams
CA-Control
Proprietary CA scrambling
CI + Standardised CCS scrambling

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Figure 7-11 CI+ Conditional Access implementation

7.7 Net TV

In this chassis, a feature that enables access to dedicated internet pages from a limited group of information suppliers, called “Net TV”, is introduced. A separate Wi-Fi module enables wireless communication with a local network.

7.8 Ambi Light

The Ambi Light architecture in this platform has been entirely renewed. The characteristics are:

- Additional DC/DC board generating 12/16/24 V (optional)
- ARM processor (on DC/DC panel or AL board)
- Low-power LEDs
- SPI interface from ARM to LED drivers
- I^2C upgradeable via USB
- Each AL module has a temperature sensor.

The use of the DC/DC board is optional. In case no DC/DC board is implemented, the ARM processor is located on one of the AL boards.

Refer to Figure 7-12 for the Ambi Light architecture.

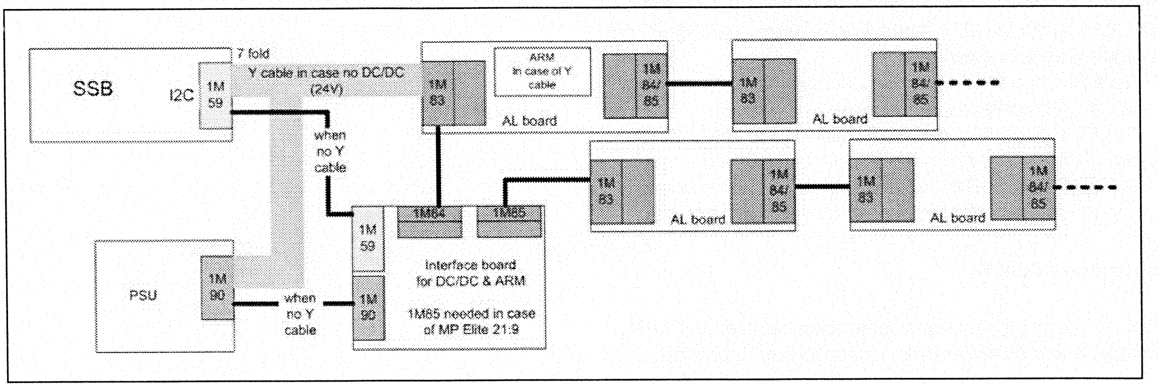
SSB
I2C
1M 59
7 fold
Y cable in case no DC/DC (24V)
when no Y cable
PSU
1M 90
when no Y cable
1M 59
1M 90
1M84
1M85
Interface board for DC/DC & ARM
1M85 needed in case of MP Elite 21:9
1M 83
ARM in case of Y cable
1M 84/ 85
AL board
1M 83
1M 84/ 85
AL board
1M 83
1M 84/ 85
AL board
1M 83
1M 84/ 85
AL board

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Figure 7-12 Interface between Ambi Light and SSB

7.8.1 ARM controller

Refer to Figure 7-13 below for signal interfacing to and from the ARM controller. The ARM controller is located on the DC/DC board (item no. 7302) or AL panel (item no. 7102).

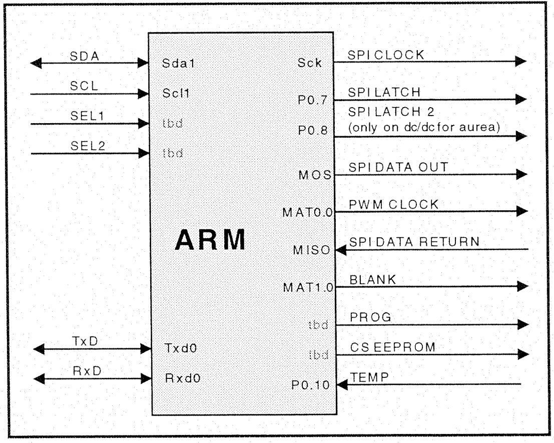
SDA
SCL
SEL1
SEL2
TxD
RxD
Sda1
Scl1
tbd
tbd
Txd0
Rxd0
ARM
Sck
P0.7
P0.8
MOS
MAT0.0
MISO
MAT1.0
tbd
tbd
P0.10
SPI CLOCK
SPI LATCH
SPI LATCH 2
(only on dc/dc for aurea)
SPI DATA OUT
PWM CLOCK
SPI DATA RETURN
BLANK
PROG
CS EEPROM
TEMP

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Figure 7-13 ARM controller interface

Data transfer between ARM processor and LED drivers is executed by a Serial Peripheral Interface (SPI) bus interface.

The SPI bus is a synchronous serial data link standard that operates in full duplex mode.

For debugging purposes, the working principle is given below:

- At startup the controller will read-out matrix data from the EEPROM devices (via SPI DATA RETURN)
- Before operation, the driver current is set via SPI, with driver in DC mode
- During normal operation the controller receives RGB-, configuration-, operation mode- and topology data via I^2C
- The controller converts the I^2C RGB data via the matrixes to SPI LED data
- Via data return the controller receives error data (if applicable).

Also PWM clock and BLANK signals are generated by the controller. The controller can be reprogrammed via I^2C (via USB). The controller can receive matrix values via I^2C, which will be stored in the EEPROM of each AL module via the SPI bus. The temperature sensor in each AL module controls the TEMP line; in case of a too high temperature the controller will reduce the overall brightness.

7.8.2 LED driver communication (via SPI bus)

Refer to Figure 7-14 below for signal interfacing between the ARM controller and the LED drivers on the AL boards, and the LED drivers and the EEPROMs on the AL boards.

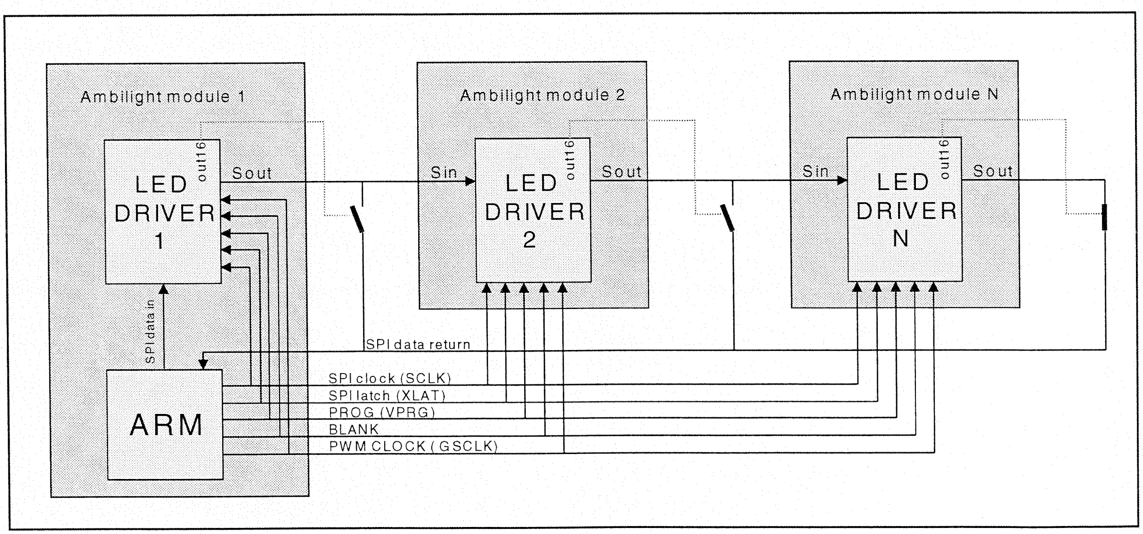
Ambilight module 1
LED DRIVER 1
out16
Sout
SPI data in
ARM
Ambilight module 2
Sin
LED DRIVER 2
out16
Sout
Ambilight module N
Sin
LED DRIVER N
out16
Sout
SPI data return
SPI clock (SCLK)
SPI latch (XLAT)
PROG (VPRG)
BLANK
PWM CLOCK (GSCLK)

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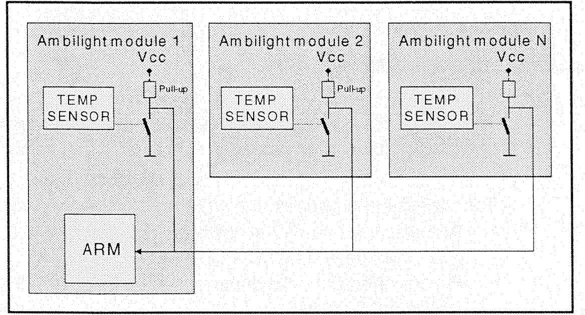
Figure 7-14 SPI communication between ARM controller and LED drivers

The ARM controller communicates with the LED drivers (on each AL module) via an SPI bus. For debugging purposes, the working principle is given below:

- Data from the ARM controller is linked through the drivers, which are connected in cascade
- SPI CLK, SPI LATCH, PROG, BLANK and PWM CLOCK are going directly from the controller to each driver
- SPI DATA RETURN is linked from the last driver to the controller: controller decides which driver returns data.

7.8.3 Temperature Control

Refer to Figure 7-15 for signal interfacing between the ARM controller and the temperature sensor on the AL boards.


Ambilight module 1
Vcc
Pull-up
TEMP SENSOR
ARM
Ambilight module 2
Vcc
Pull-up
TEMP SENSOR
Ambilight module N
Vcc
TEMP SENSOR

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090318

Figure 7-15 Communication between ARM controller and temperature sensor

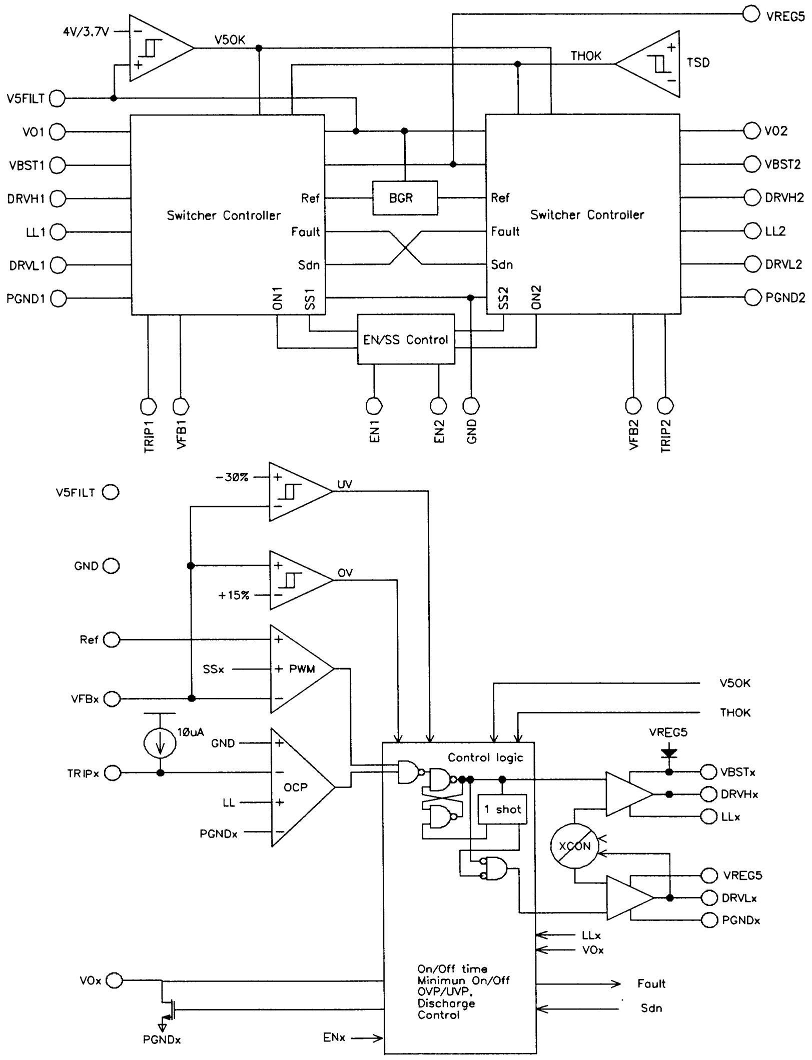
Each AL board is equipped with a temperature sensor. If one of the sensors detects a temperature over the threshold, the TEMP line is pulled LOW which results in brightness reduction.

8. IC Data Sheets

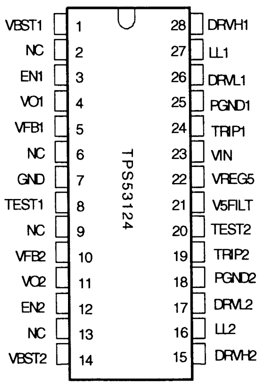
This chapter shows the internal block diagrams and pin configurations of ICs that are drawn as “black boxes” in the electrical diagrams (with the exception of “memory” and “logic” ICs).

8.1 Diagram SSB: DC/DC B01A, TPS53124PW (IC 7U03)

Block Diagram


4V/3.7V
V5OK
VREG5
THOK
TSD
V5FILT
VO1
VBST1
DRVH1
LL1
DRVL1
PGND1
Switcher Controller
Ref
Fault
Sdn
ON1
SS1
BGR
EN/SS Control
Switcher Controller
Ref
Fault
Sdn
SS2
ON2
VO2
VBST2
DRVH2
LL2
DRVL2
PGND2
TRIP1
VFB1
EN1
EN2
GND
VFB2
TRIP2
V5FILT
GND
Ref
VFBx
TRIPx
-30%
UV
+15%
OV
SSx
PWM
10uA
GND
OCP
LL
PGNDx
V5OK
THOK
VREG5
Control logic
1 shot
VBSTx
DRVHx
LLx
XCON
VREG5
DRVLx
PGNDx
LLx
VOx
On/Off time
Minimun On/Off
OVP/UVP,
Discharge
Control
Fault
Sdn
VOx
PGNDx
ENx

Pin Configuration

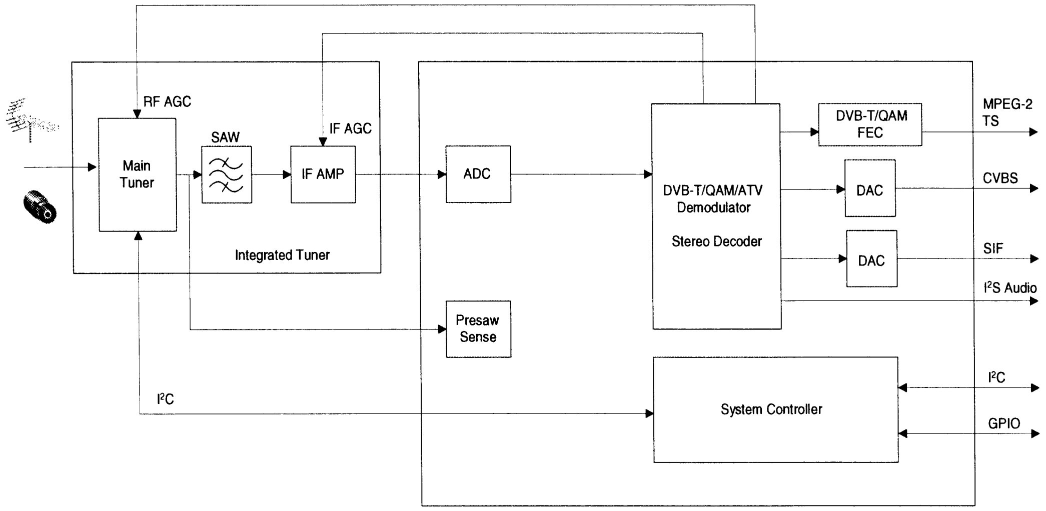

VBST1 1
NC 2
EN1 3
VO1 4
VFB1 5
NC 6
GND 7
TEST1 8
NC 9
VFB2 10
VO2 11
EN2 12
NC 13
VBST2 14
TPS53124
28 DRVH1
27 LL1
26 DRVL1
25 PGND1
24 TRIP1
23 VIN
22 VREG5
21 V5FILT
20 TEST2
19 TRIP2
18 PGND2
17 DRVL2
16 LL2
15 DRVH2

18250_300_090319.eps
090319

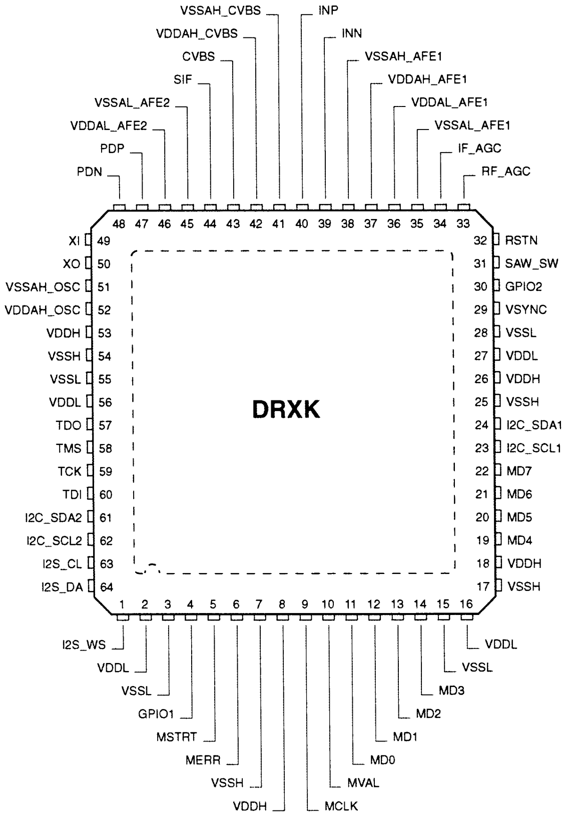
Figure 8-1 Internal block diagram and pin configuration

8.2 Diagram SSB: Front End B02B, DRX3926K (IC 7T50)

Block Diagram


RF AGC
IF AGC
SAW
Main Tuner
IF AMP
Integrated Tuner
ADC
Presaw Sense
DVB-T/QAM/ATV Demodulator
Stereo Decoder
DVB-T/QAM FEC
DAC
DAC
System Controller
MPEG-2 TS
CVBS
SIF
I²S Audio
I²C
GPIO
I²C

Pin Configuration

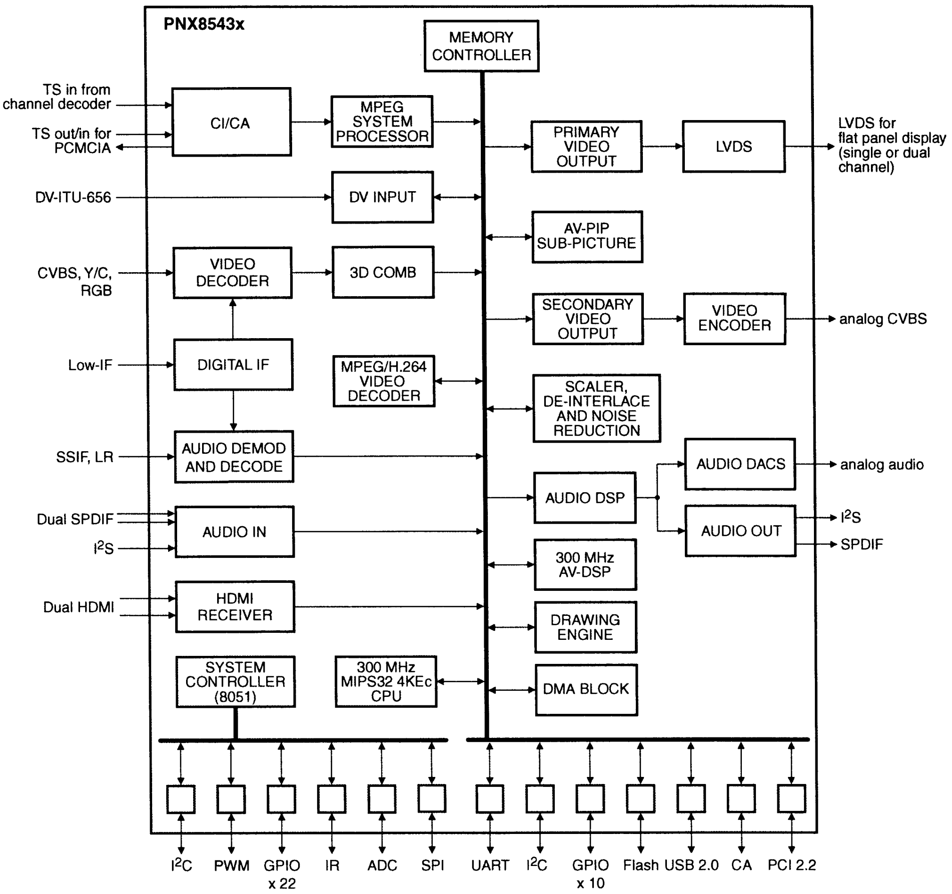

DRXK
1 I2S_WS
2 VDDL
3 VSSL
4 GPIO1
5 MSTRT
6 MERR
7 VSSH
8 VDDH
9 MCLK
10 MVAL
11 MD0
12 MD1
13 MD2
14 MD3
15 VSSL
16 VDDL
17 VSSH
18 VDDH
19 MD4
20 MD5
21 MD6
22 MD7
23 I2C_SCL1
24 I2C_SDA1
25 VSSH
26 VDDH
27 VDDL
28 VSSL
29 VSYNC
30 GPIO2
31 SAW_SW
32 RSTN
33 RF_AGC
34 IF_AGC
35 VSSAL_AFE1
36 VDDAL_AFE1
37 VDDAH_AFE1
38 VSSAH_AFE1
39 INN
40 INP
41 VSSAH_CVBS
42 VDDAH_CVBS
43 CVBS
44 SIF
45 VSSAL_AFE2
46 VDDAL_AFE2
47 PDP
48 PDN
49 XI
50 XO
51 VSSAH_OSC
52 VDDAH_OSC
53 VDDH
54 VSSH
55 VSSL
56 VDDL
57 TDO
58 TMS
59 TCK
60 TDI
61 I2C_SDA2
62 I2C_SCL2
63 I2S_CL
64 I2S_DA

18440_300_090303.eps
090303

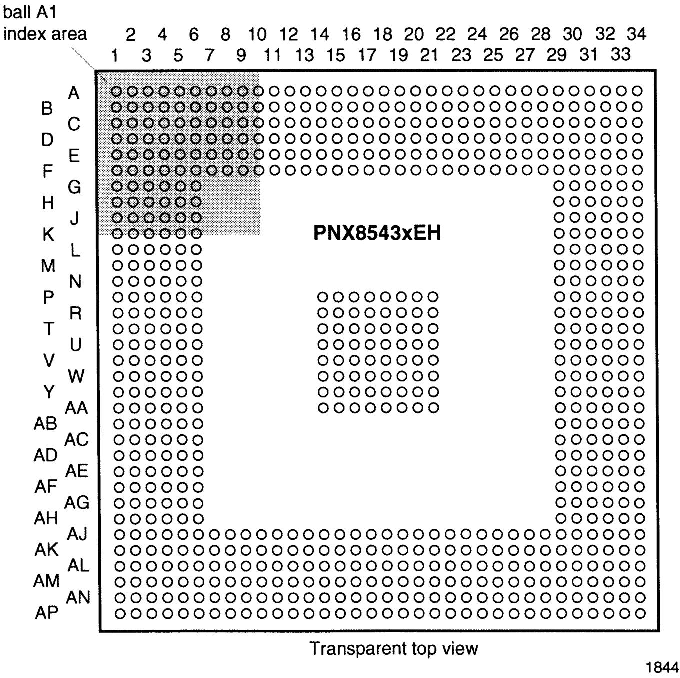
Figure 8-2 Pin configuration

8.3 Diagram SSB: PNX8543 - Stand-by Controller B04A, PNX8543 (IC7H00)

Block Diagram


PNX8543x
MEMORY CONTROLLER
TS in from channel decoder
TS out/in for PCMCIA
CI/CA
MPEG SYSTEM PROCESSOR
PRIMARY VIDEO OUTPUT
LVDS
LVDS for flat panel display (single or dual channel)
DV-ITU-656
DV INPUT
AV-PIP SUB-PICTURE
CVBS, Y/C, RGB
VIDEO DECODER
3D COMB
SECONDARY VIDEO OUTPUT
VIDEO ENCODER
analog CVBS
Low-IF
DIGITAL IF
MPEG/H.264 VIDEO DECODER
SCALER, DE-INTERLACE AND NOISE REDUCTION
SSIF, LR
AUDIO DEMOD AND DECODE
AUDIO DACS
analog audio
AUDIO DSP
Dual SPDIF
I^2S
AUDIO IN
AUDIO OUT
I^2S
SPDIF
300 MHz AV-DSP
Dual HDMI
HDMI RECEIVER
DRAWING ENGINE
SYSTEM CONTROLLER (8051)
300 MHz MIPS32 4KEc CPU
DMA BLOCK
I^2C
PWM
GPIO x 22
IR
ADC
SPI
UART
I^2C
GPIO x 10
Flash
USB 2.0
CA
PCI 2.2

Pin Configuration

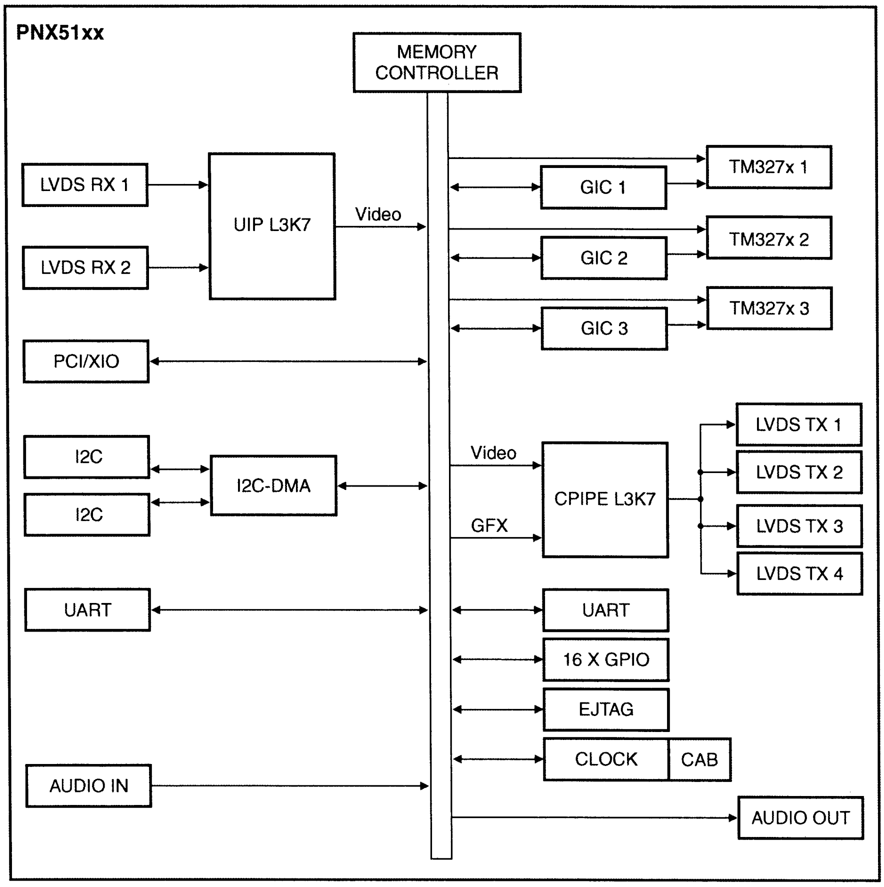

ball A1 index area
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33
A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
T
U
V
W
Y
AA
AB
AC
AD
AE
AF
AG
AH
AJ
AK
AL
AM
AN
AP
PNX8543xEH
Transparent top view

18440_301_090303.eps
090303

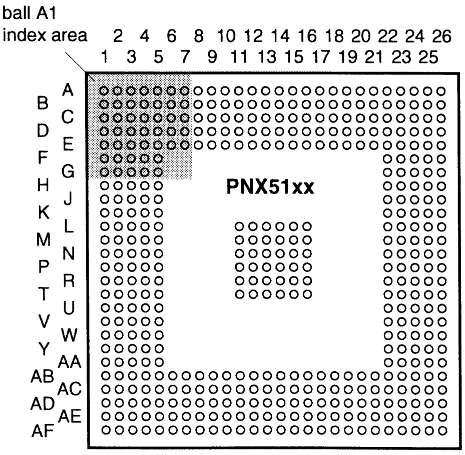
Figure 8-3 Internal block diagram and pin configuration

8.4 Diagram SSB: Ethernet B05A, PNX5120 (IC7C00)

Block Diagram


PNX51xx
MEMORY CONTROLLER
LVDS RX 1
LVDS RX 2
UIP L3K7
Video
TM327x 1
GIC 1
TM327x 2
GIC 2
TM327x 3
GIC 3
PCI/XIO
I2C
I2C
I2C-DMA
Video
GFX
CPIPE L3K7
LVDS TX 1
LVDS TX 2
LVDS TX 3
LVDS TX 4
UART
UART
16 X GPIO
EJTAG
CLOCK
CAB
AUDIO IN
AUDIO OUT

Pin Configuration

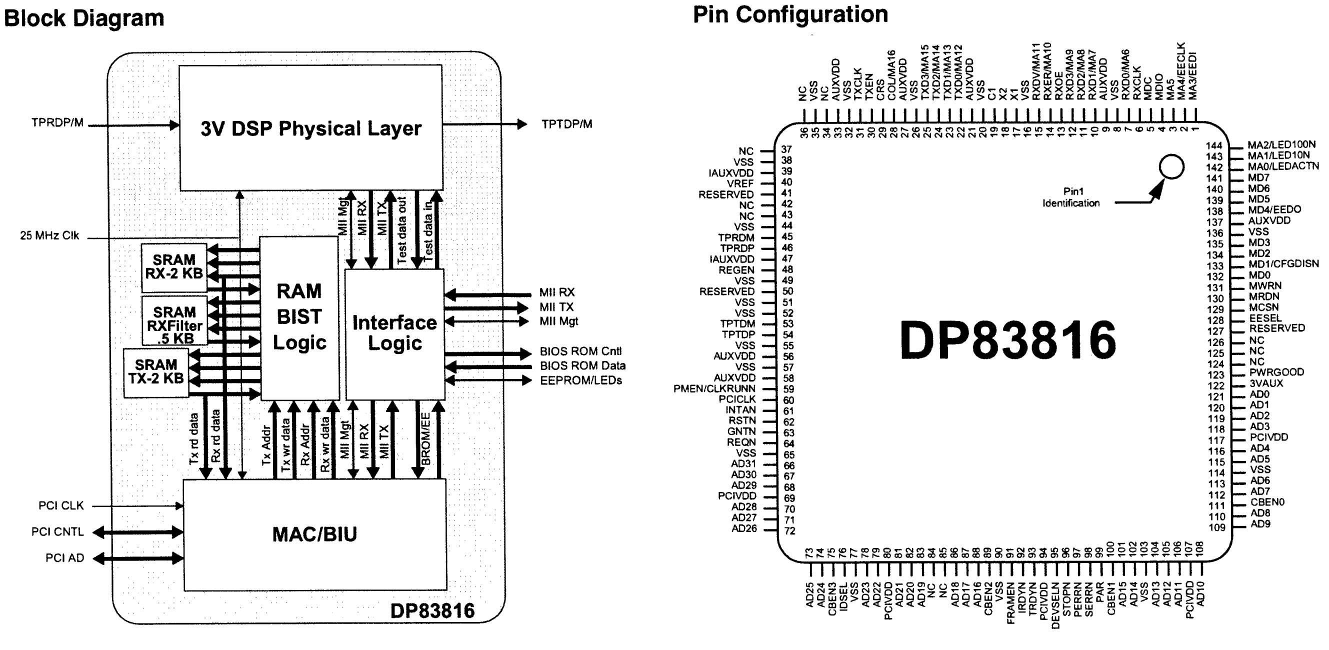

ball A1 index area
2 4 6 8 10 12 14 16 18 20 22 24 26
1 3 5 7 9 11 13 15 17 19 21 23 25
A B C D E F G H J K L M N P R T U V W Y AA AB AC AD AE AF
PNX51xx

Transparent top view

18560_300_090403.eps
090403

Figure 8-4 Internal block diagram and pin configuration

8.5 Diagram SSB: Ethernet B07G, DP83816 (IC7N04)



Block Diagram

Pin Configuration

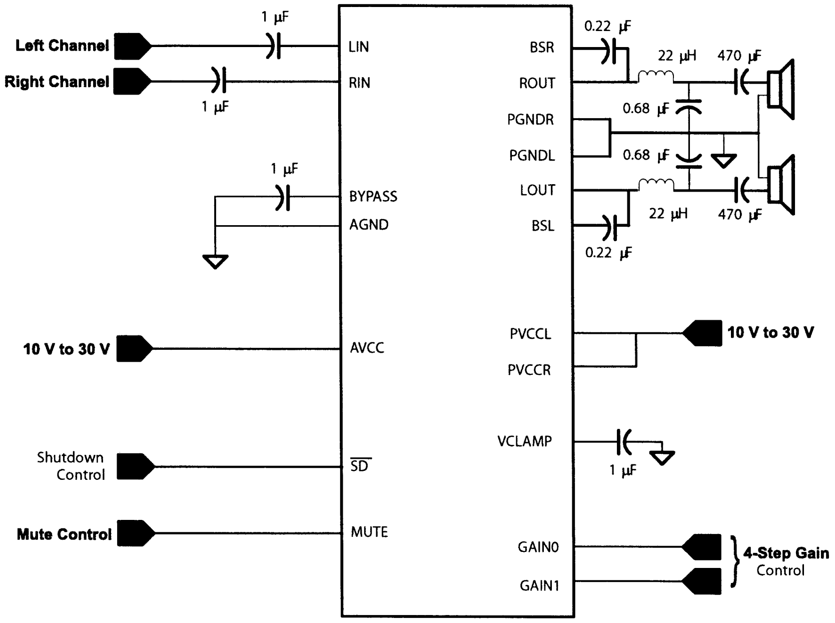
TPRDP/M
3V DSP Physical Layer
TPTDP/M
25 MHz Clk
SRAM RX-2 KB
SRAM RXFilter .5 KB
SRAM TX-2 KB
RAM BIST Logic
Interface Logic
MII Mgt
MII RX
MII TX
Test data out
Test data in
MII RX
MII TX
MII Mgt
BIOS ROM Cntl
BIOS ROM Data
EEPROM/LEDs
Tx rd data
Rx rd data
Tx Addr
Tx wr data
Rx Addr
Rx wr data
MII Mgt
MII RX
MII TX
BROM/EE
PCI CLK
PCI CNTL
PCI AD
MAC/BIU
DP83816
1 MA3/EEDI
2 MA4/EECLK
3 MA5
4 MDIO
5 MDC
6 RXCLK
7 RXD0/MA6
8 VSS
9 AUXVDD
10 RXD1/MA7
11 RXD2/MA8
12 RXD3/MA9
13 RXOE
14 RXER/MA10
15 RXDV/MA11
16 VSS
17 X1
18 X2
19 C1
20 VSS
21 AUXVDD
22 TXD0/MA12
23 TXD1/MA13
24 TXD2/MA14
25 TXD3/MA15
26 VSS
27 AUXVDD
28 COL/MA16
29 CRS
30 TXEN
31 TXCLK
32 VSS
33 AUXVDD
34 NC
35 VSS
36 NC
37 NC
38 VSS
39 IAUXVDD
40 VREF
41 RESERVED
42 NC
43 NC
44 VSS
45 TPRDM
46 TPRDP
47 IAUXVDD
48 REGEN
49 VSS
50 RESERVED
51 VSS
52 VSS
53 TPTDM
54 TPTDP
55 VSS
56 AUXVDD
57 VSS
58 AUXVDD
59 PMEN/CLKRUNN
60 PCICLK
61 INTAN
62 RSTN
63 GNTN
64 REQN
65 VSS
66 AD31
67 AD30
68 AD29
69 PCIVDD
70 AD28
71 AD27
72 AD26
73 AD25
74 AD24
75 CBEN3
76 IDSEL
77 VSS
78 AD23
79 AD22
80 PCIVDD
81 AD21
82 AD20
83 AD19
84 NC
85 NC
86 AD18
87 AD17
88 AD16
89 CBEN2
90 VSS
91 FRAMEN
92 IRDYN
93 TRDYN
94 PCIVDD
95 DEVSELN
96 STOPN
97 PERRN
98 SERRN
99 PAR
100 CBEN1
101 AD15
102 AD14
103 VSS
104 AD13
105 AD12
106 AD11
107 PCIVDD
108 AD10
109 AD9
110 AD8
111 CBEN0
112 AD7
113 AD6
114 VSS
115 AD5
116 AD4
117 PCIVDD
118 AD3
119 AD2
120 AD1
121 AD0
122 3VAUX
123 PWRGOOD
124 NC
125 NC
126 NC
127 RESERVED
128 EESEL
129 MCSN
130 MRDN
131 MWRN
132 MD0
133 MD1/CFGDISN
134 MD2
135 MD3
136 VSS
137 AUXVDD
138 MD4/EEDO
139 MD5
140 MD6
141 MD7
142 MA0/LEDACTN
143 MA1/LED10N
144 MA2/LED100N
Pin1 Identification
DP83816

F_15710_167.eps
230905

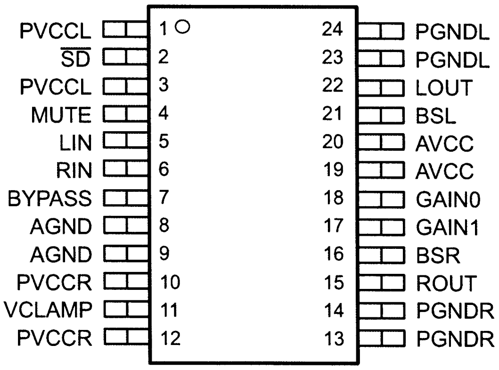
Figure 8-5 Internal block diagram and pin configuration

8.6 Diagram SSB: Audio B10A, TPA3123D (IC 7D10)

Block Diagram


Left Channel
Right Channel
1 µF
1 µF
1 µF
10 V to 30 V
Shutdown Control
Mute Control
LIN
RIN
BYPASS
AGND
AVCC
SD
MUTE
BSR
ROUT
PGNDR
PGNDL
LOUT
BSL
PVCCL
PVCCR
VCLAMP
GAIN0
GAIN1
0.22 µF
22 µH
470 µF
0.68 µF
0.68 µF
22 µH
470 µF
0.22 µF
10 V to 30 V
1 µF
4-Step Gain Control

Pin Configuration


PVCCL 1
SD 2
PVCCL 3
MUTE 4
LIN 5
RIN 6
BYPASS 7
AGND 8
AGND 9
PVCCR 10
VCLAMP 11
PVCCR 12
24 PGNDL
23 PGNDL
22 LOUT
21 BSL
20 AVCC
19 AVCC
18 GAIN0
17 GAIN1
16 BSR
15 ROUT
14 PGNDR
13 PGNDR

TERMINAL		I/O/P	DESCRIPTION
NAME	24-PIN (PWP)		
SD	2	I	Shutdown signal for IC (low = disabled, high = operational). TTL logic levels with compliance to AVCC
RIN	6	I	Audio input for right channel
LIN	5	I	Audio input for left channel
GAIN0	18	I	Gain select least-significant bit. TTL logic levels with compliance to AVCC
GAIN1	17	I	Gain select most-significant bit. TTL logic levels with compliance to AVCC
MUTE	4	I	Mute signal for quick disable/enable of outputs (high = outputs switch at 50% duty cycle, low = outputs enabled). TTL logic levels with compliance to AVCC
BSL	21	I/O	Bootstrap I/O for left channel
PVCCL	1, 3	P	Power supply for left-channel H-bridge, not internally connected to PVCCR or AVCC
LOUT	22	O	Class-D 1/2-H-bridge positive output for left channel
PGNDL	23, 24	P	Power ground for left-channel H-bridge
VCLAMP	11	P	Internally generated voltage supply for bootstrap capacitors
BSR	16	I/O	Bootstrap I/O for right channel
ROUT	15	O	Class-D 1/2-H-bridge negative output for right channel
PGNDR	13, 14	P	Power ground for right-channel H-bridge.
PVCCR	10, 12	P	Power supply for right-channel H-bridge, not connected to PVCCL or AVCC
AGND	9	P	Analog ground for digital/analog cells in core
AGND	8	P	Analog ground for analog cells in core
BYPASS	7	O	Reference for preamplifier inputs. Nominally equal to AVCC/8. Also controls start-up time via external capacitor sizing.
AVCC	19, 20	P	High-voltage analog power supply. Not internally connected to PVCCR or PVCCL
Thermal pad	Die pad	P	Connect to ground. Thermal pad should be soldered down on all applications to properly secure device to printed wiring board.

18440_302_090303.eps
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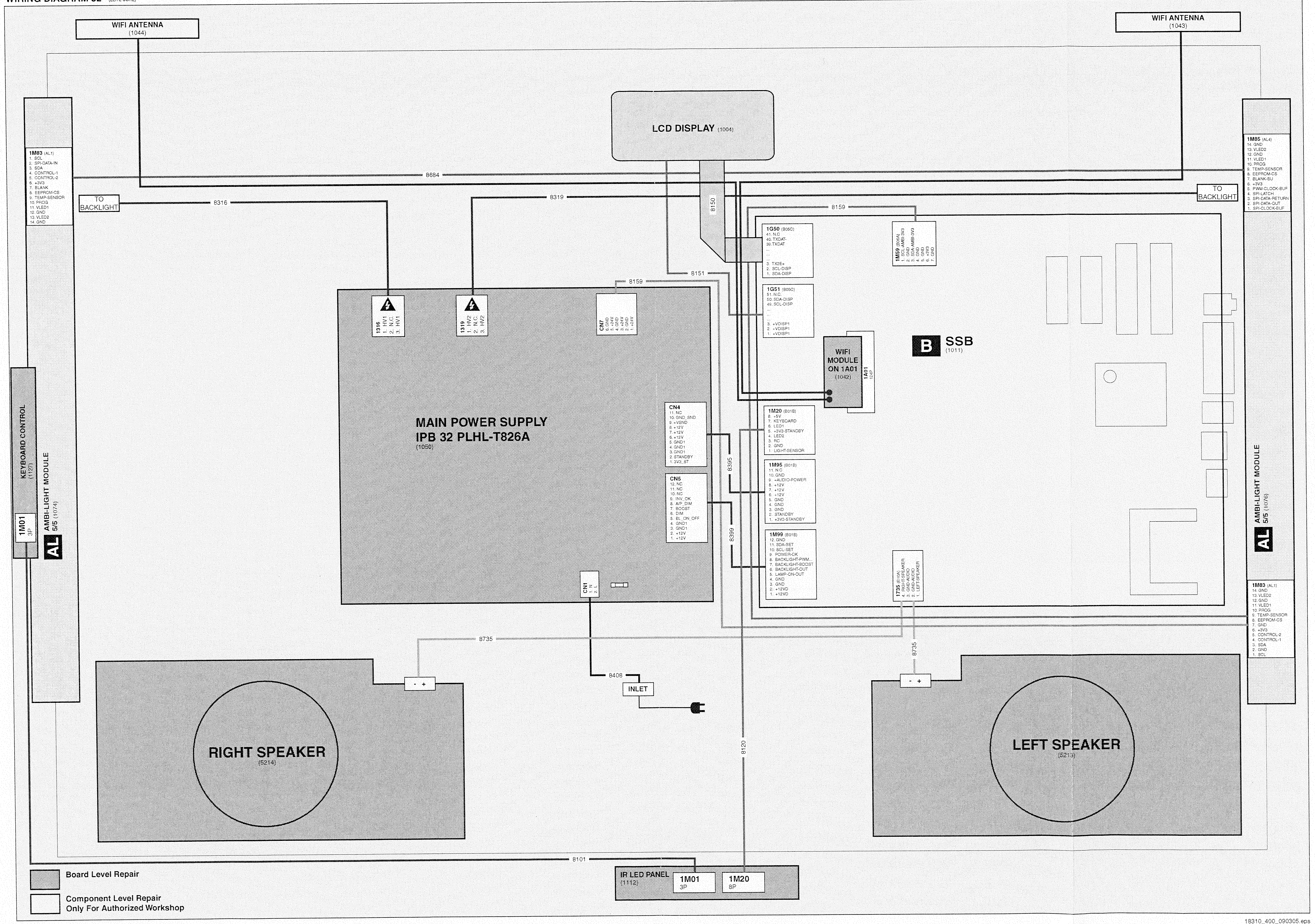
Figure 8-6 Internal block diagram and pin configuration

9. Block Diagrams

Wiring Diagram 32" (Elite Core)

WIRING DIAGRAM 32" (ELITE CORE)


WIFI ANTENNA
(1044)
WIFI ANTENNA
(1043)
LCD DISPLAY (1004)
1M83 (AL1)
1. SCL
2. SPI-DATA-IN
3. SDA
4. CONTROL-1
5. CONTROL-2
6. +3V3
7. BLANK
8. EEPROM-CS
9. TEMP-SENSOR
10. PROG
11. VLED1
12. GND
13. VLED2
14. GND
TO BACKLIGHT
8684
8316
8319
8150
8159
8151
TO BACKLIGHT
1M85 (AL4)
14. GND
13. VLED2
12. GND
11. VLED1
10. PROG
9. TEMP-SENSOR
8. EEPROM-CS
7. BLANK-BU
6. +3V3
5. PWM-CLOCK-BUF
4. SPI-LATCH
3. SPI-DATA-RETURN
2. SPI-DATA-OUT
1. SPI-CLOCK-BUF
1G50 (B05C)
41. N.C
40. TXDAT-
39. TXDAT
...
3. TX2E+
2. SCL-DISP
1. SDA-DISP
1G51 (B05C)
51. N.C.
50. SDA-DISP
49. SCL-DISP
...
3. +VDISP1
2. +VDISP1
1. +VDISP1
1M59 (B06A)
1. SCL-AMBI-3V3
2. GND
3. SDA-AMBI-3V3
4. GND
5. GND
6. +3V3
7. GND
WIFI MODULE ON 1A01
(1042)
1A01
124P
B SSB
(1011)
1316
1. HV1
2. N.C.
3. HV1
1319
1. HV2
2. N.C.
3. HV2
CN7
6. GND
5. +24V
4. GND
3. +24V
2. GND
1. +24V
MAIN POWER SUPPLY
IPB 32 PLHL-T826A
(1050)
CN4
11. NC
10. GND_SND
9. +VSND
8. +12V
7. +12V
6. +12V
5. GND1
4. GND1
3. GND1
2. STANDBY
1. 3V3_ST
CN5
12. NC
11. NC
10. NC
9. INV_OK
8. A/P_DIM
7. BOOST
6. DIM
5. BL_ON_OFF
4. GND1
3. GND1
2. +12V
1. +12V
8395
8399
1M20 (B01B)
8. +5V
7. KEYBOARD
6. LED1
5. +3V3-STANDBY
4. LED2
3. RC
2. GND
1. LIGHT-SENSOR
1M95 (B01B)
11. N.C
10. GND
9. +AUDIO-POWER
8. +12V
7. +12V
6. +12V
5. GND
4. GND
3. GND
2. STANDBY
1. +3V3-STANDBY
1M99 (B01B)
12. GND
11. SDA-SET
10. SCL-SET
9. POWER-OK
8. BACKLIGHT-PWM...
7. BACKLIGHT-BOOST
6. BACKLIGHT-OUT
5. LAMP-ON-OUT
4. GND
3. GND
2. +12VD
1. +12VD
1735 (B10A)
4. RIGHT-SPEAKER
3. GND-AUDIO
2. GND-AUDIO
1. LEFT-SPEAKER
KEYBOARD CONTROL
(1127)
1M01
3P
AL AMBI-LIGHT MODULE
5/5 (1074)
AL AMBI-LIGHT MODULE
5/5 (1076)
1M83 (AL1)
14. GND
13. VLED2
12. GND
11. VLED1
10. PROG
9. TEMP-SENSOR
8. EEPROM-CS
7. GND
6. +3V3
5. CONTROL-2
4. CONTROL-1
3. SDA
2. GND
1. SCL
CN1
1. N
2. L
8735
8408
INLET
- +
- +
8735
8120
RIGHT SPEAKER
(5214)
LEFT SPEAKER
(5213)
8101
IR LED PANEL
(1112)
1M01
3P
1M20
8P
Board Level Repair
Component Level Repair
Only For Authorized Workshop

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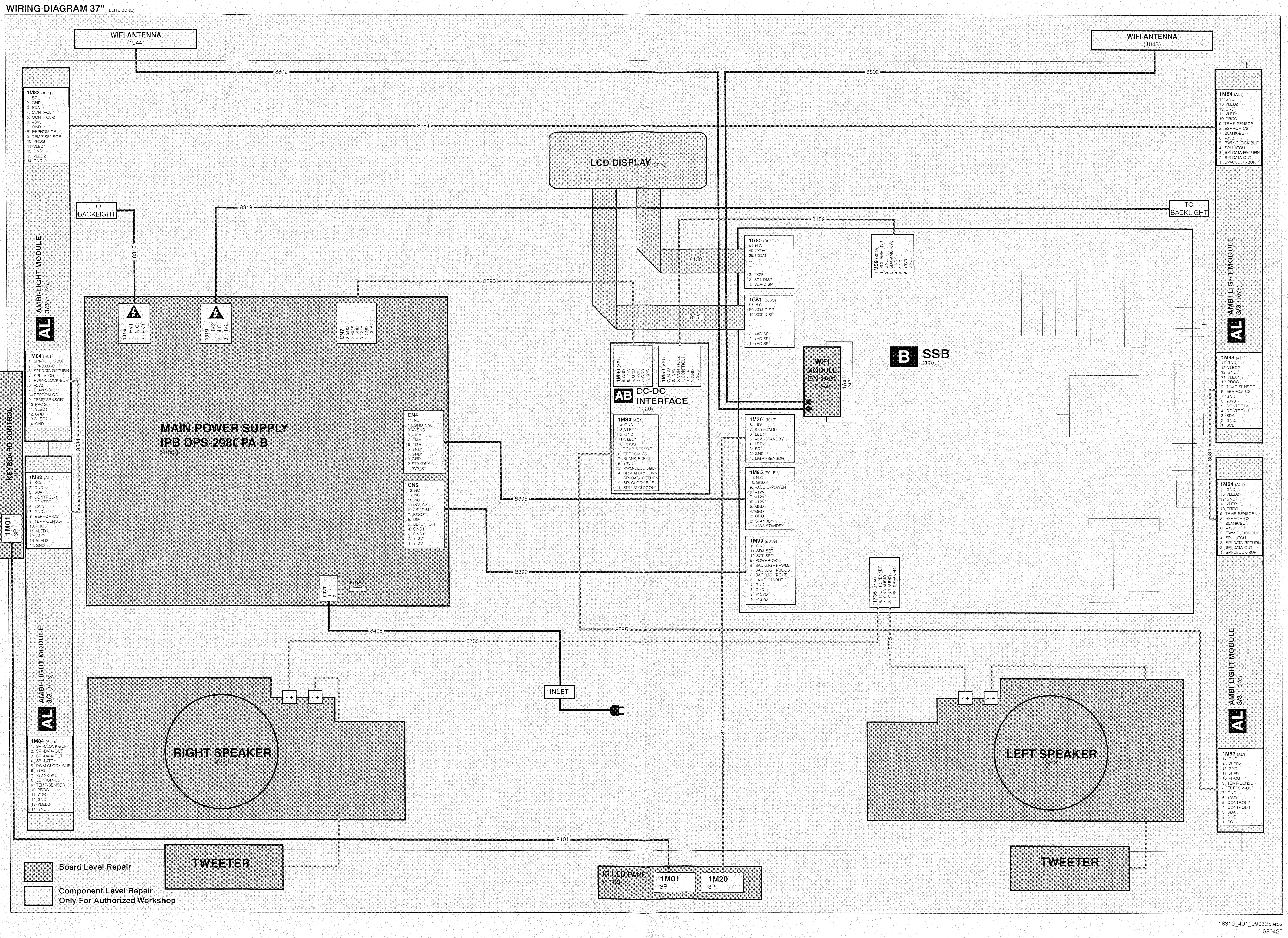
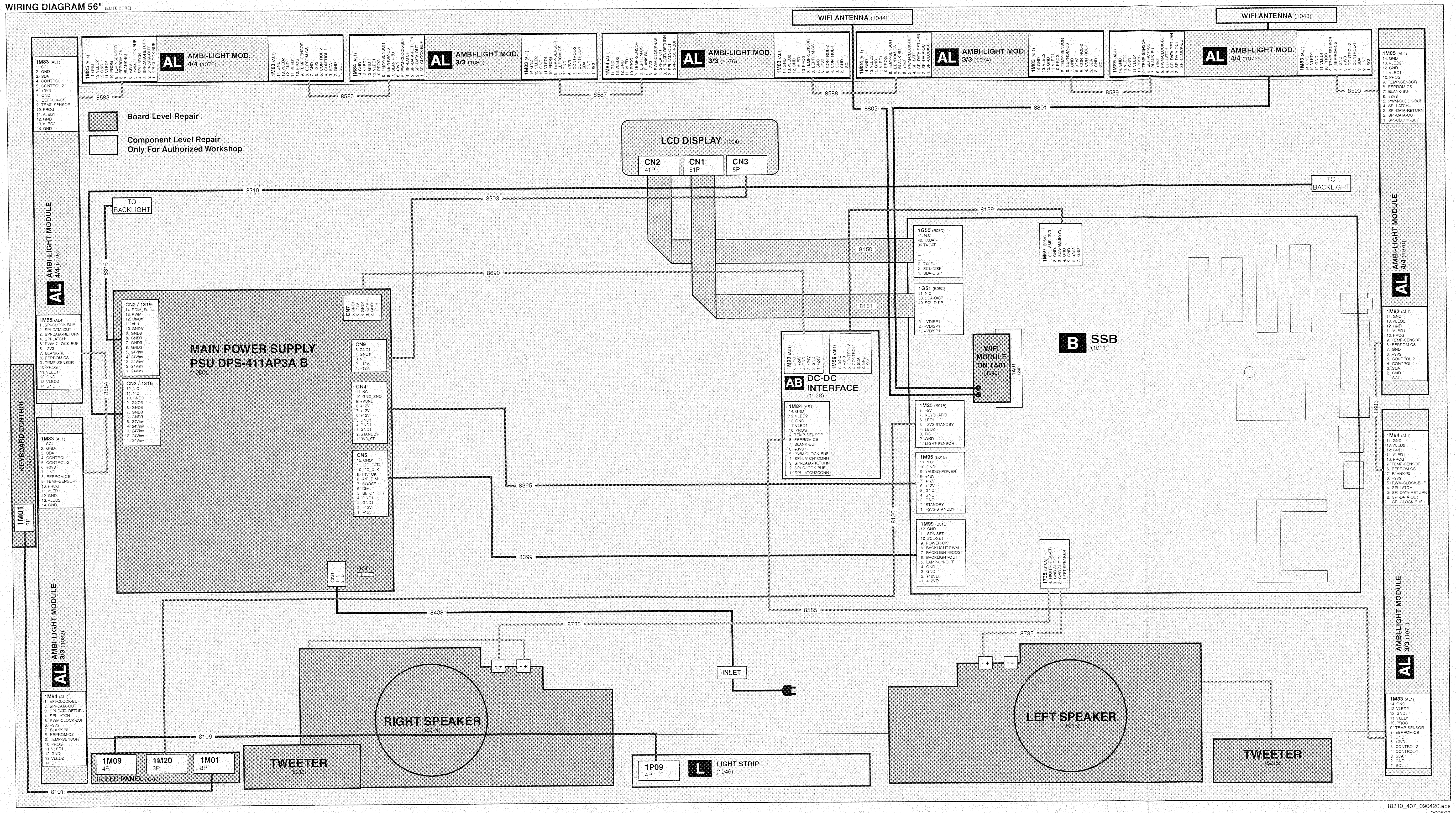
090421

Wiring Diagram 37" (Elite Core)


WIRING DIAGRAM 37" (ELITE CORE)
WIFI ANTENNA (1044)
WIFI ANTENNA (1043)
8802
8684
LCD DISPLAY (1004)
TO BACKLIGHT
8319
8316
8159
8150
8151
8590
1G50 (B05C)
1G51 (B05C)
1M59 (B05B)
AMBI-LIGHT MODULE 3/3 (1074)
AMBI-LIGHT MODULE 3/3 (1075)
AMBI-LIGHT MODULE 3/3 (1073)
AMBI-LIGHT MODULE 3/3 (1076)
AL
1M83 (AL1)
1M84 (AL1)
1316
1319
CN7
CN4
CN5
CN1
FUSE
MAIN POWER SUPPLY
IPB DPS-298CPA B
(1050)
1M90 (AB1)
1M59 (AB1)
AB
DC-DC INTERFACE (1028)
1M84 (AB1)
WIFI MODULE ON 1A01 (1042)
1A01
B
SSB (1150)
1M20 (B01B)
1M95 (B01B)
1M99 (B01B)
1735 (B01B)
KEYBOARD CONTROL (1114)
1M01 3P
8584
8395
8399
8408
8735
8585
8120
8101
INLET
RIGHT SPEAKER (5214)
LEFT SPEAKER (5213)
TWEETER
TWEETER
IR LED PANEL (1112)
1M01 3P
1M20 8P
Board Level Repair
Component Level Repair Only For Authorized Workshop
18310_401_090305.eps
090420

Wiring Diagram 56" (Elite Core)


WIRING DIAGRAM 56" (ELITE CORE)
Board Level Repair
Component Level Repair
Only For Authorized Workshop
WIFI ANTENNA (1044)
WIFI ANTENNA (1043)
AL AMBI-LIGHT MOD. 4/4 (1073)
AL AMBI-LIGHT MOD. 3/3 (1080)
AL AMBI-LIGHT MOD. 3/3 (1076)
AL AMBI-LIGHT MOD. 3/3 (1074)
AL AMBI-LIGHT MOD. 4/4 (1072)
AL AMBI-LIGHT MODULE 4/4 (1075)
AL AMBI-LIGHT MODULE 3/3 (1082)
AL AMBI-LIGHT MODULE 4/4 (1070)
AL AMBI-LIGHT MODULE 3/3 (1071)
KEYBOARD CONTROL (1127)
1M01 3P
LCD DISPLAY (1004)
CN2 41P
CN1 51P
CN3 5P
TO BACKLIGHT
TO BACKLIGHT
MAIN POWER SUPPLY
PSU DPS-411AP3A B
(1050)
CN2 / 1319
CN3 / 1316
CN7
CN9
CN4
CN5
CN1
FUSE
AB DC-DC INTERFACE (1028)
1M90
1M59
1M84
B SSB (1011)
1G50
1G51
1M59
WIFI MODULE ON 1A01 (1042)
1A01 12P
1M20
1M95
1M99
1735
INLET
RIGHT SPEAKER (5214)
LEFT SPEAKER (5213)
TWEETER (5216)
TWEETER (5215)
1M09 4P
1M20 3P
1M01 8P
IR LED PANEL (1047)
1P09 4P
L LIGHT STRIP (1046)
8583
8586
8587
8588
8589
8590
8802
8801
8319
8303
8159
8150
8151
8316
8690
8584
8395
8399
8120
8683
8406
8735
8735
8585
8109
8101

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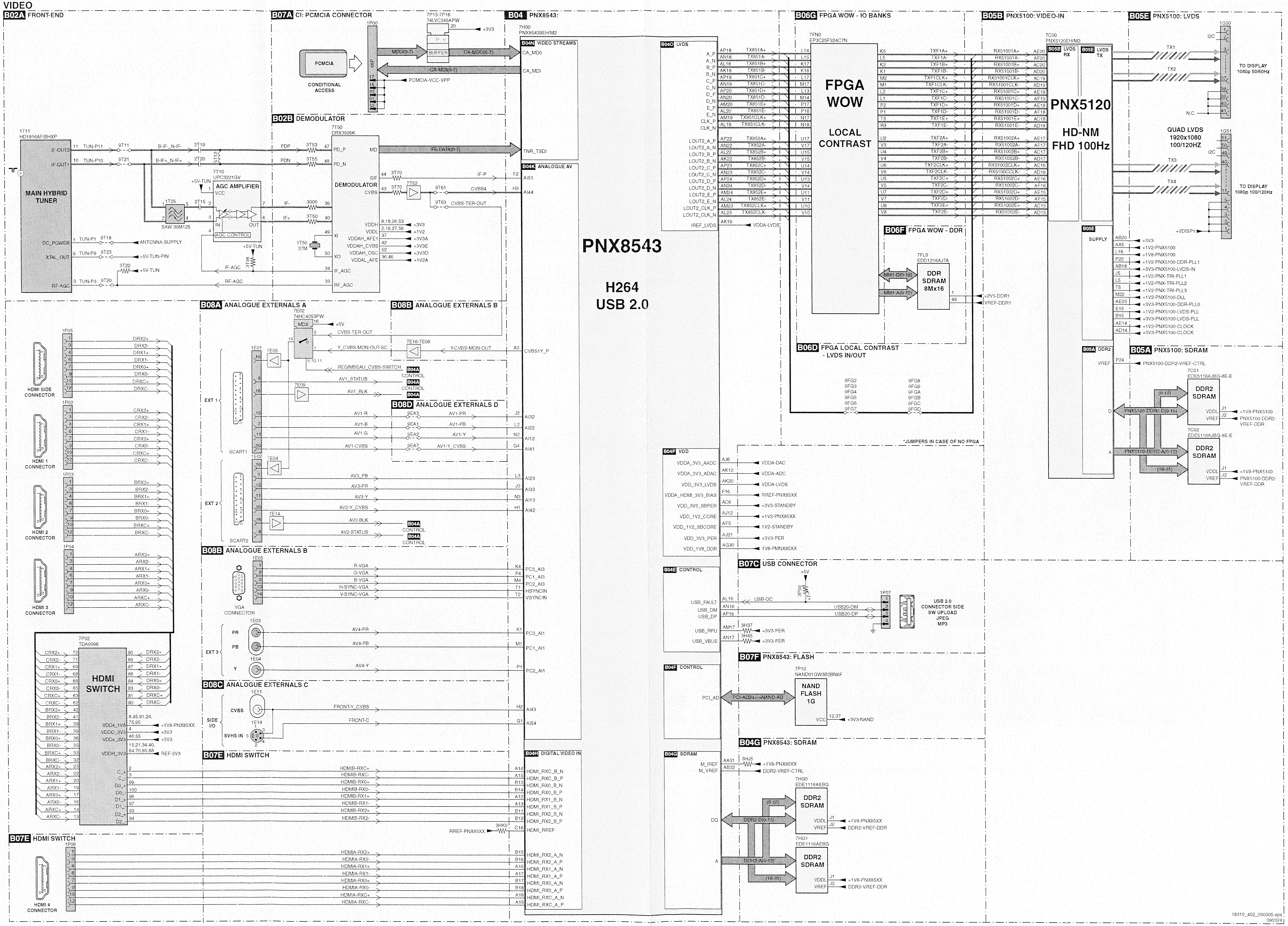
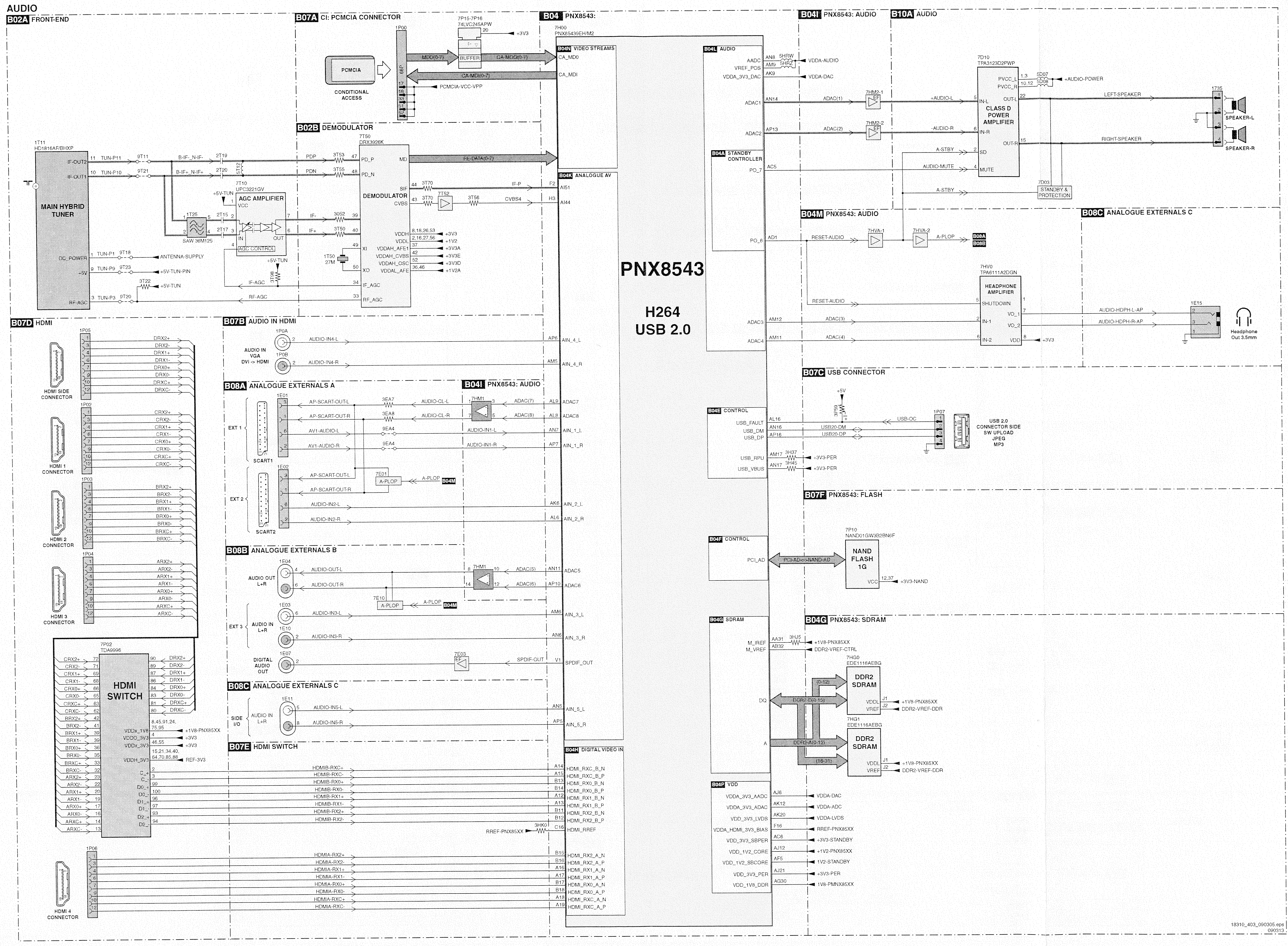
090508

Block Diagram Video



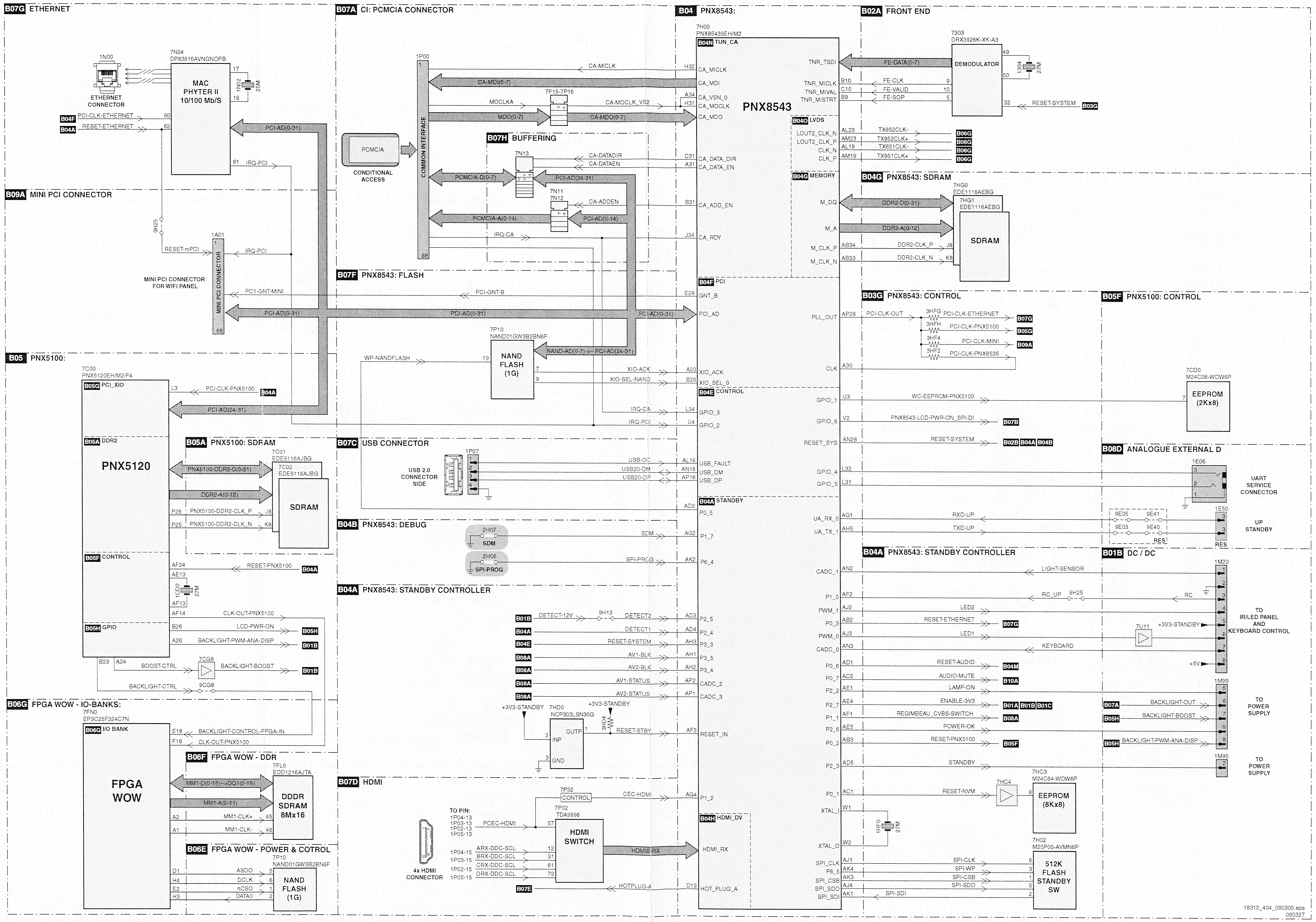
VIDEO
B02A FRONT-END
MAIN HYBRID TUNER
1T11 HD1816AF/BHXP
IF-OUT2
IF-OUT1
DC_POWER
XTAL_OUT
RF-AGC
AGC AMPLIFIER
7T10 UPC3221GV
AGC CONTROL
SAW 36M125
B07A CI: PCMCIA CONNECTOR
PCMCIA
CONDITIONAL ACCESS
7P15-7P16 74LVC245APW
BUFFER
MDX(0-7)
CA-MDO(0-7)
CA-MDI(0-7)
PCMCIA-VCC-VPP
B02B DEMODULATOR
7T50 DRX3926K
DEMODULATOR
FE-DATA(0-7)
CVBS-TER-OUT
B04 PNX8543:
7H00 PNX85439EH/M2
B04N VIDEO STREAMS
CA_MDO
CA_MDI
TNR_TSDI
B04K ANALOGUE AV
PNX8543
H264
USB 2.0
B04O LVDS
B06G FPGA WOW - IO BANKS
7FN0 EP3C25F324C7N
FPGA WOW
LOCAL CONTRAST
B06F FPGA WOW - DDR
7FL0 EDD1216AJTA
DDR SDRAM 8Mx16
B06D FPGA LOCAL CONTRAST - LVDS IN/OUT
*JUMPERS IN CASE OF NO FPGA
B05B PNX5100: VIDEO-IN
7C00 PNX5120EH/M2
B05B LVDS RX
B05E LVDS TX
PNX5120
HD-NM
FHD 100Hz
B05E PNX5100: LVDS
TO DISPLAY 1080p 50/60Hz
QUAD LVDS 1920x1080 100/120HZ
TO DISPLAY 1080p 100/120Hz
B05E SUPPLY
B05A DDR2
B05A PNX5100: SDRAM
7C01 EDE5116AJBG-8E-E
7C02 EDE5116AJBG-8E-E
DDR2 SDRAM
B08A ANALOGUE EXTERNALS A
7E02 74HC4053PW
MDX
EXT 1
SCART1
EXT 2
SCART2
B08B ANALOGUE EXTERNALS B
B08D ANALOGUE EXTERNALS D
B04A CONTROL
B08B ANALOGUE EXTERNALS B
VGA CONNECTOR
EXT 3
B08C ANALOGUE EXTERNALS C
SIDE I/O
CVBS
SVHS IN
HDMI SIDE CONNECTOR
HDMI 1 CONNECTOR
HDMI 2 CONNECTOR
HDMI 3 CONNECTOR
HDMI 4 CONNECTOR
7P02 TDA9996
HDMI SWITCH
B07E HDMI SWITCH
B04H DIGITAL VIDEO IN
B04P VDD
B04E CONTROL
B07C USB CONNECTOR
USB 2.0 CONNECTOR SIDE SW UPLOAD JPEG MP3
B04F CONTROL
B07F PNX8543: FLASH
7P10 NAND01GW3B2BN6F
NAND FLASH 1G
B04G SDRAM
B07G PNX8543: SDRAM
7HG0 EDE1116AEBG
7HG1 EDE1116AEBG
DDR2 SDRAM
18310_402_090305.eps 090324

Block Diagram Audio


AUDIO
B02A FRONT-END
B07A CI: PCMCIA CONNECTOR
B04 PNX8543:
B04I PNX8543: AUDIO
B10A AUDIO
PCMCIA
CONDITIONAL ACCESS
BUFFER
B04N VIDEO STREAMS
B04L AUDIO
B02B DEMODULATOR
7T50 DRX3926K
DEMODULATOR
1T11 HD1816AF/BHXP
MAIN HYBRID TUNER
7T10 UPC3221GV
AGC AMPLIFIER
AGC CONTROL
SAW 36M125
B04K ANALOGUE AV
B04A STANDBY CONTROLLER
7D10 TPA3123D2PWP
CLASS D POWER AMPLIFIER
LEFT-SPEAKER
RIGHT-SPEAKER
SPEAKER-L
SPEAKER-R
STANDBY & PROTECTION
+AUDIO-POWER
B04M PNX8543: AUDIO
B08C ANALOGUE EXTERNALS C
7HV0 TPA6111A2DGN
HEADPHONE AMPLIFIER
Headphone Out 3.5mm
PNX8543
H264
USB 2.0
B07D HDMI
HDMI SIDE CONNECTOR
HDMI 1 CONNECTOR
HDMI 2 CONNECTOR
HDMI 3 CONNECTOR
HDMI 4 CONNECTOR
B07B AUDIO IN HDMI
AUDIO IN VGA DVI -> HDMI
B08A ANALOGUE EXTERNALS A
EXT 1
SCART1
EXT 2
SCART2
B04I PNX8543: AUDIO
B07C USB CONNECTOR
B04E CONTROL
USB 2.0 CONNECTOR SIDE SW UPLOAD JPEG MP3
B07F PNX8543: FLASH
B04F CONTROL
NAND FLASH 1G
B08B ANALOGUE EXTERNALS B
AUDIO OUT L+R
EXT 3
AUDIO IN L+R
DIGITAL AUDIO OUT
B08C ANALOGUE EXTERNALS C
SIDE I/O
B04G SDRAM
B04G PNX8543: SDRAM
DDR2 SDRAM
7P02 TDA9996
HDMI SWITCH
B07E HDMI SWITCH
B04H DIGITAL VIDEO IN
B04P VDD
18310_403_090305.eps 090313

Block Diagram Control & Clock Signals

CONTROL + CLOCK SIGNALS


B07G ETHERNET
1N00
ETHERNET CONNECTOR
7N04
DP83816AVNGNOPB
MAC PHYTER II 10/100 Mb/S
1N02
25M
B04F PCI-CLK-ETHERNET
B04A RESET-ETHERNET
PCI-AD(0-31)
IRQ-PCI
B09A MINI PCI CONNECTOR
9H25
1A01
RESET-mPCI
IRQ-PCI
MINI PCI CONNECTOR FOR WIFI PANEL
MINI PCI CONNECTOR
PC1-GNT-MINI
PCI-AD(0-31)
B07A CI: PCMCIA CONNECTOR
1P00
COMMON INTERFACE
PCMCIA
CONDITIONAL ACCESS
CA-MICLK
CA-MDI(0-7)
7P15-7P16
MOCLKA
CA-MOCLK_VS2
MDO(0-7)
CA-MDO(0-7)
B07H BUFFERING
7N13
CA-DATADIR
CA-DATAEN
PCMCIA-D(0-7)
PCI-AD(24-31)
7N11
7N12
CA-ADDEN
PCMCIA-A(0-14)
PCI-AD(0-14)
IRQ-CA
B07F PNX8543: FLASH
PCI-GNT-B
PCI-AD(0-31)
7P10
NAND01GW3B2BN6F
NAND FLASH (1G)
WP-NANDFLASH
NAND-AD(0-7) <-- PCI-AD(24-31)
XIO-ACK
XIO-SEL-NAND
IRQ-CA
IRQ-PCI
B05 PNX5100:
7C00
PNX5120EH/M2/F4
B05G PCI_XIO
PCI-CLK-PNX5100 B04A
PCI-AD(24-31)
B05A DDR2
PNX5120
B05A PNX5100: SDRAM
7C01
EDE5116AJBG
7C02
EDE5116AJBG
SDRAM
PNX5100-DDR2-D(0-31)
DDR2-A(0-12)
PNX5100-DDR2-CLK_P
PNX5100-DDR2-CLK_N
B05F CONTROL
RESET-PNX5100 B04A
1CD0
27M
CLK-OUT-PNX5100
B05H GPIO
LCD-PWR-ON B05H
BACKLIGHT-PWM-ANA-DISP B01B
7CG8
BOOST-CTRL
BACKLIGHT-BOOST B01B
BACKLIGHT-CTRL
9CG8
B07C USB CONNECTOR
1P07
USB 2.0 CONNECTOR SIDE
USB-OC
USB20-DM
USB20-DP
B04B PNX8543: DEBUG
2H07
SDM
2H06
SPI-PROG
B04A PNX8543: STANDBY CONTROLLER
B01B DETECT-12V
9H13
DETECT2
B04A DETECT1
B04E RESET-SYSTEM
B08A AV1-BLK
B08A AV2-BLK
B08A AV1-STATUS
B08A AV2-STATUS
+3V3-STANDBY
7HD0
NCP303LSN30G
3HD4
OUTP
INP
GND
RESET-STBY
B06G FPGA WOW - IO-BANKS:
7FN0
EP3C25F324C7N
B06G I/O BANK
FPGA WOW
BACKLIGHT-CONTROL-FPGA-IN
CLK-OUT-PNX5100
B06F FPGA WOW - DDR
7FL0
EDD1216AJTA
DDDR SDRAM 8Mx16
MM1-D(0-15)-->DQ1(0-15)
MM1-A(0-11)
MM1-CLK+
MM1-CLK-
B06E FPGA WOW - POWER & COTROL
7P10
NAND01GW3B2BN6F
NAND FLASH (1G)
ASDO
DCLK
nCSO
DATA0
B07D HDMI
4x HDMI CONNECTOR
TO PIN:
1P04-13
1P03-13
1P02-13
1P05-13
PCEC-HDMI
1P04-15 ARX-DDC-SCL
1P03-15 BRX-DDC-SCL
1P02-15 CRX-DDC-SCL
1P05-15 DRX-DDC-SCL
7P32
CONTROL
CEC-HDMI
7P02
TDA9996
HDMI SWITCH
HDMIB-RX
B07E HOTPLUG-A
B04 PNX8543:
7H00
PNX85439EH/M2
B04N TUN_CA
PNX8543
CA_MICLK
CA_MDI
CA_VSN_0
CA_MOCLK
CA_MDO
CA_DATA_DIR
CA_DATA_EN
CA_ADD_EN
CA_RDY
TNR_TSDI
TNR_MICLK
TNR_MIVAL
TNR_MISTRT
B04O LVDS
LOUT2_CLK_N
LOUT2_CLK_P
CLK_N
CLK_P
B04G MEMORY
M_DQ
M_A
M_CLK_P
M_CLK_N
B04F PCI
GNT_B
PCI_AD
PLL_OUT
CLK
XIO_ACK
XIO_SEL_0
B04E CONTROL
GPIO_1
GPIO_3
GPIO_2
GPIO_6
RESET_SYS
USB_FAULT
USB_DM
USB_DP
GPIO_4
GPIO_5
B04A STANDBY
P0_5
P1_7
P6_4
UA_RX_0
UA_TX_1
CADC_1
P1_0
PWM_1
P0_3
PWM_0
CADC_0
P2_5
P2_4
P3_3
P3_5
P3_4
CADC_2
CADC_3
RESET_IN
P0_6
P0_7
P2_2
P2_7
P1_1
P2_6
P0_2
P2_3
P1_2
P0_1
XTAL_I
XTAL_O
B04H HDMI_DV
HDMI_RX
HOT_PLUG_A
SPI_CLK
P6_5
SPI_CSB
SPI_SDO
SPI_SDI
B02A FRONT END
7303
DRX3926K-XK-A3
DEMODULATOR
1304
27M
FE-DATA(0-7)
FE-CLK
FE-VALID
FE-SOP
RESET-SYSTEM B03G
TX852CLK- B06G
TX852CLK+ B06G
TX851CLK- B06G
TX851CLK+ B06G
B04G PNX8543: SDRAM
7HG0
EDE1116AEBG
7HG1
EDE1116AEBG
SDRAM
DDR2-D(0-31)
DDR2-A(0-12)
DDR2-CLK_P
DDR2-CLK_N
B03G PNX8543: CONTROL
PCI-CLK-OUT
3HFG PCI-CLK-ETHERNET B07G
3HFH PCI-CLK-PNX5100 B05G
3HF4 PCI-CLK-MINI B09A
3HF2 PCI-CLK-PNX8535
B05F PNX5100: CONTROL
7CD0
M24C08-WDW6P
EEPROM (2Kx8)
WC-EEPROM-PNX5100
PNX8543-LCD-PWR-ON_SPI-DI B07B
RESET-SYSTEM B02B B04A B04B
B08D ANALOGUE EXTERNAL D
1E06
UART SERVICE CONNECTOR
RXD-UP
TXD-UP
9E05
9E41
9E03
9E40
RES
1E50
UP STANDBY
B04A PNX8543: STANDBY CONTROLLER
LIGHT-SENSOR
RC_UP
9H25
RC
LED2
RESET-ETHERNET B07G
LED1
KEYBOARD
RESET-AUDIO B04M
AUDIO-MUTE B10A
LAMP-ON
ENABLE-3V3 B01A B01B B01C
REGIMBEAU_CVBS-SWITCH B08A
POWER-OK
RESET-PNX5100 B05F
STANDBY
7HC4
RESET-NVM
7HC3
M24C64-WDW6P
EEPROM (8Kx8)
1HF0
27M
7H02
M25P05-AVMN6P
512K FLASH STANDBY SW
SPI-CLK
SPI-WP
SPI-CSB
SPI-SDO
SPI-SDI
B01B DC / DC
1M20
TO IR/LED PANEL AND KEYBOARD CONTROL
7U11
+3V3-STANDBY
+5V
1M99
B07A BACKLIGHT-OUT
B05H BACKLIGHT-BOOST
B05H BACKLIGHT-PWM-ANA-DISP
TO POWER SUPPLY
1M95
TO POWER SUPPLY
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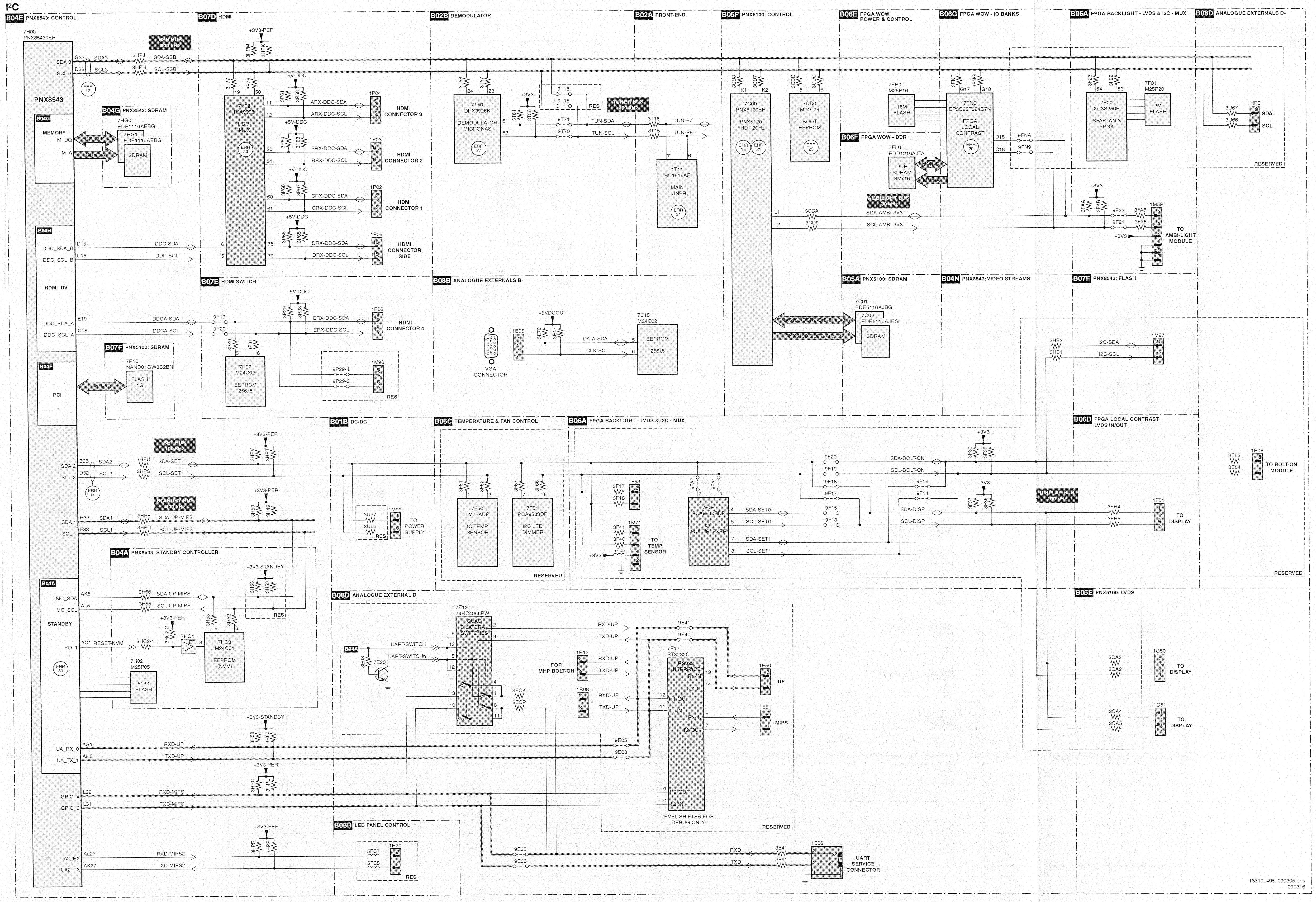
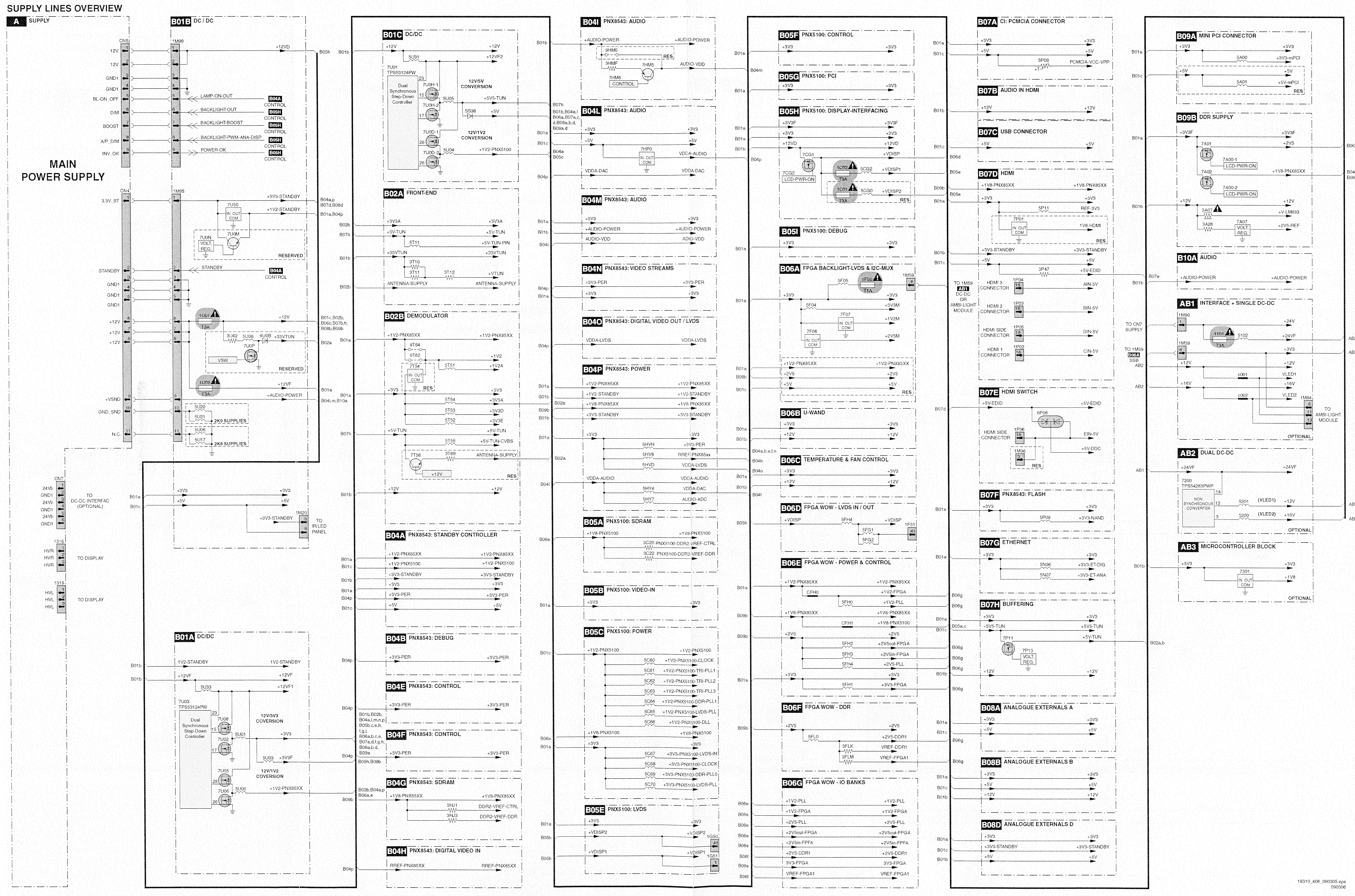
Block Diagram I^{2}C


I²C
B04E PNX8543: CONTROL
7H00
PNX85439EH
PNX8543
SSB BUS 400 kHz
SDA 3
SCL 3
SDA-SSB
SCL-SSB
B04G PNX8543: SDRAM
7HG0 EDE1116AEBG
7HG1 EDE1116AEBG
SDRAM
MEMORY
M_DQ
M_A
DDR2-D
DDR2-A
B04H
DDC_SDA_B
DDC_SCL_B
HDMI_DV
DDC_SDA_A
DDC_SCL_A
B04F
PCI
PCI-AD
B07F PNX5100: SDRAM
7P10 NAND01GW3B2BN
FLASH 1G
B07D HDMI
+3V3-PER
+5V-DDC
7P02 TDA9996
HDMI MUX
ARX-DDC-SDA
ARX-DDC-SCL
HDMI CONNECTOR 3
BRX-DDC-SDA
BRX-DDC-SCL
HDMI CONNECTOR 2
CRX-DDC-SDA
CRX-DDC-SCL
HDMI CONNECTOR 1
DRX-DDC-SDA
DRX-DDC-SCL
HDMI CONNECTOR SIDE
DDC-SDA
DDC-SCL
B07E HDMI SWITCH
DDCA-SDA
DDCA-SCL
ERX-DDC-SDA
ERX-DDC-SCL
HDMI CONNECTOR 4
7P07 M24C02
EEPROM 256x8
RES
B02B DEMODULATOR
7T50 DRX3926K
DEMODULATOR MICRONAS
TUNER BUS 400 kHz
TUN-SDA
TUN-SCL
TUN-P7
TUN-P6
B02A FRONT-END
1T11 HD1816AF
MAIN TUNER
B05F PNX5100: CONTROL
7C00 PNX5120EH
PNX5120 FHD 120Hz
7CD0 M24C08
BOOT EEPROM
B06E FPGA WOW POWER & CONTROL
7FH0 M25P16
16M FLASH
B06G FPGA WOW - IO BANKS
7FN0 EP3C25F324C7N
FPGA LOCAL CONTRAST
B06F FPGA WOW - DDR
7FL0 EDD1216AJTA
DDR SDRAM 8Mx16
MM1-D
MM1-A
AMBILIGHT BUS 30 kHz
SDA-AMBI-3V3
SCL-AMBI-3V3
TO AMBI-LIGHT MODULE
B06A FPGA BACKLIGHT - LVDS & I2C - MUX
7F00 XC3S250E
SPARTAN-3 FPGA
7F01 M25P20
2M FLASH
B08D ANALOGUE EXTERNALS D-
SDA
SCL
RESERVED
B08B ANALOGUE EXTERNALS B
+5VDCOUT
VGA CONNECTOR
7E18 M24C02
EEPROM 256x8
DATA-SDA
CLK-SCL
B05A PNX5100: SDRAM
7C01 EDE5116AJBG
7C02 EDE5116AJBG
SDRAM
PNX5100-DDR2-D(0-31)(0-31)
PNX5100-DDR2-A(0-12)
B04N PNX8543: VIDEO STREAMS
B07F PNX8543: FLASH
I2C-SDA
I2C-SCL
B01B DC/DC
SET BUS 100 kHz
SDA 2
SCL 2
SDA-SET
SCL-SET
TO POWER SUPPLY
STANDBY BUS 400 kHz
SDA 1
SCL 1
SDA-UP-MIPS
SCL-UP-MIPS
B06C TEMPERATURE & FAN CONTROL
7F50 LM75ADP
IC TEMP SENSOR
7F51 PCA9533DP
I2C LED DIMMER
TO TEMP SENSOR
B06A FPGA BACKLIGHT - LVDS & I2C - MUX
7F08 PCA9540BDP
I2C MULTIPLEXER
SDA-SET0
SCL-SET0
SDA-SET1
SCL-SET1
SDA-BOLT-ON
SCL-BOLT-ON
TO BOLT-ON MODULE
SDA-DISP
SCL-DISP
DISPLAY BUS 100 kHz
TO DISPLAY
B06D FPGA LOCAL CONTRAST LVDS IN/OUT
B04A PNX8543: STANDBY CONTROLLER
+3V3-STANDBY
7HC4
7HC3 M24C64
EEPROM (NVM)
7H02 M25P05
512K FLASH
B04A
MC_SDA
MC_SCL
STANDBY
PO_1
RESET-NVM
UA_RX_0
UA_TX_1
RXD-UP
TXD-UP
GPIO_4
GPIO_5
RXD-MIPS
TXD-MIPS
UA2_RX
UA2_TX
RXD-MIPS2
TXD-MIPS2
B08D ANALOGUE EXTERNAL D
7E19 74HC4066PW
QUAD BILATERAL SWITCHES
UART-SWITCH
UART-SWITCHn
FOR MHP BOLT-ON
7E17 ST3232C
RS232 INTERFACE
R1-IN
T1-OUT
R1-OUT
T1-IN
R2-IN
T2-OUT
R2-OUT
T2-IN
LEVEL SHIFTER FOR DEBUG ONLY
UP
MIPS
B05E PNX5100: LVDS
B06B LED PANEL CONTROL
RXD
TXD
UART SERVICE CONNECTOR
18310_405_090305.eps 090316

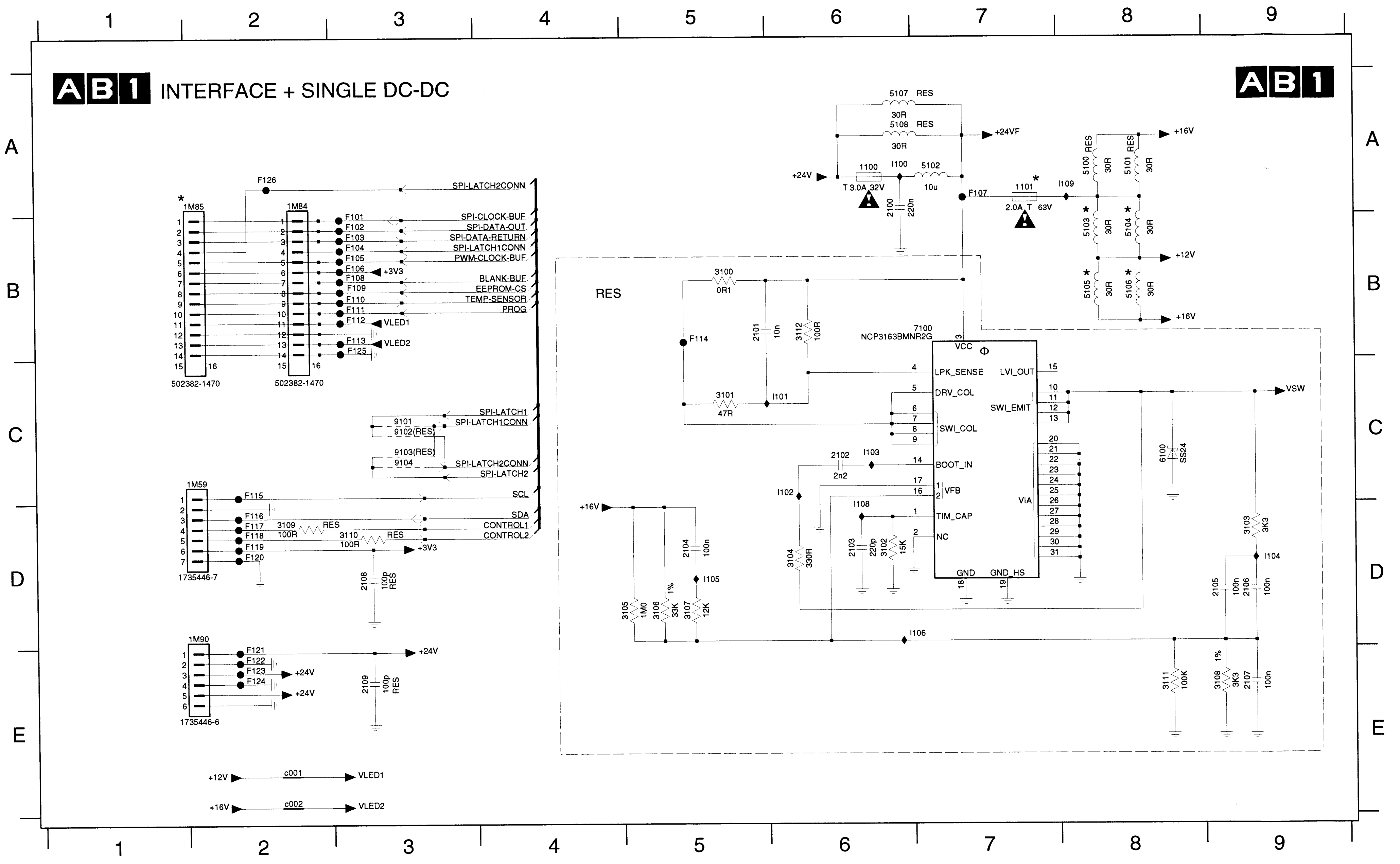
Supply Lines Overview


SUPPLY LINES OVERVIEW
A SUPPLY
MAIN POWER SUPPLY
CN5
12V
GND1
BL-ON_OFF
DIM
BOOST
A/P_DIM
INV_OK
CN4
3.3V_ST
STANDBY
+12V
+VSND
GND_SND
N.C.
CN7
24Vb
TO DC-DC INTERFAC (OPTIONAL)
1316
HVR
TO DISPLAY
1319
HVL
TO DISPLAY
B01B DC / DC
1M99
+12VD
LAMP-ON-OUT
BACKLIGHT-OUT
BACKLIGHT-BOOST
BACKLIGHT-PWM-ANA-DISP
POWER-OK
B04A CONTROL
B05H CONTROL
1M95
+3V3-STANDBY
+1V2-STANDBY
7U50
7U0N VOLT REG.
7U0M
RESERVED
1U01 T3A
+3VTUN
7U0P
VSW
1U03 T3A
+12VF
+AUDIO-POWER
2K9 SUPPLIES
2K8 SUPPLIES
1M20
TO IR/LED PANEL
B01A DC/DC
+1V2-STANDBY
+12VF1
7U03 TPS53124PW
Dual Synchronous Step-Down Controller
12V/3V3 COVERSION
12V/1V2 COVERSION
+1V2-PNX85XX
B01C DC/DC
7U01 TPS53124PW
12V/5V CONVERSION
12V/1V2 CONVERSION
+5V5-TUN
+1V2-PNX5100
B02A FRONT-END
+3V3A
+5V-TUN
+5V-TUN-PIN
+33VTUN
+VTUN
ANTENNA-SUPPLY
B02B DEMODULATOR
+1V2-PNX85XX
+1V2
+1V2A
+3V3
+3V3D
+3V3E
+5V-TUN-CVBS
ANTENNA-SUPPLY
RES
B04A PNX8543: STANDBY CONTROLLER
B04B PNX8543: DEBUG
+3V3-PER
B04E PNX8543: CONTROL
B04F PNX8543: CONTROL
B04G PNX8543: SDRAM
+1V8-PNX85XX
DDR2-VREF-CTRL
DDR2-VREF-DDR
B04H PNX8543: DIGITAL VIDEO IN
RREF-PNX85XX
B04I PNX8543: AUDIO
+AUDIO-POWER
AUDIO-VDD
B04L PNX8543: AUDIO
VDDA-AUDIO
VDDA-DAC
B04M PNX8543: AUDIO
B04N PNX8543: VIDEO STREAMS
B04O PNX8543: DIGITAL VIDEO OUT / LVDS
VDDA-LVDS
B04P PNX8543: POWER
+3V3-STANDBY
+1V8-PNX85XX
VDDA-AUDIO
VDDA-DAC
AUDIO-ADC
B05A PNX5100: SDRAM
+1V8-PNX5100
PNX5100-DDR2-VREF-CTRL
PNX5100-DDR2-VREF-DDR
B05B PNX5100: VIDEO-IN
B05C PNX5100: POWER
+1V2-PNX5100-CLOCK
+1V2-PNX5100-TRI-PLL1
+1V2-PNX5100-TRI-PLL2
+1V2-PNX5100-TRI-PLL3
+1V2-PNX5100-DDR-PLL1
+1V2-PNX5100-LVDS-PLL
+1V2-PNX5100-DLL
+3V3-PNX5100-LVDS-IN
+3V3-PNX5100-CLOCK
+3V3-PNX5100-DDR-PLL0
+3V3-PNX5100-LVDS-PLL
B05E PNX5100: LVDS
+VDISP2
+VDISP1
B05F PNX5100: CONTROL
B05G PNX5100: PCI
B05H PNX5100: DISPLAY-INTERFACING
+3V3F
+12VD
+VDISP
LCD-PWR-ON
+VDISP1
+VDISP2
B05I PNX5100: DEBUG
B06A FPGA BACKLIGHT-LVDS & I2C-MUX
+3V3M
+1V2M
+2V5M
B06B U-WAND
B06C TEMPERATURE & FAN CONTROL
B06D FPGA WOW - LVDS IN / OUT
B06E FPGA WOW - POWER & CONTROL
+1V2-FPGA
+1V2-PLL
+1V8-PNX5100
+2V5out-FPGA
+2V5in-FPGA
+2V5-PLL
+3V3-FPGA
B06F FPGA WOW - DDR
+2V5-DDR1
VREF-DDR1
VREF-FPGA1
B06G FPGA WOW - IO BANKS
B07A CI: PCMCIA CONNECTOR
PCMCIA-VCC-VPP
B07B AUDIO IN HDMI
B07C USB CONNECTOR
B07D HDMI
+1V8-HDMI
REF-3V3
+5V-EDID
HDMI 3 CONNECTOR
HDMI 2 CONNECTOR
HDMI SIDE CONNECTOR
HDMI 1 CONNECTOR
TO 1M59 AB1 DC-DC OR AMBI-LIGHT MODULE
B07E HDMI SWITCH
+5V-DDC
B07F PNX8543: FLASH
+3V3-NAND
B07G ETHERNET
+3V3-ET-DIG
+3V3-ET-ANA
B07H BUFFERING
B08A ANALOGUE EXTERNALS A
B08B ANALOGUE EXTERNALS B
B08D ANALOGUE EXTERNALS D
B09A MINI PCI CONNECTOR
+3V3-mPCI
+5V-mPCI
B09B DDR SUPPLY
LCD-PWR-ON
+V-LM833
+2V5-REF
B10A AUDIO
AB1 INTERFACE + SINGLE DC-DC
TO CN7 SUPPLY
TO 1M59 B06A SSB
+24VF
VLED1
VLED2
TO AMBI-LIGHT MODULE
OPTIONAL
AB2 DUAL DC-DC
7200 TPS54283PWP
NON SYNCHRONOUS CONVERTER
AB3 MICROCONTROLLER BLOCK
18310_406_090305.eps
090306

10. Circuit Diagrams and PWB Layouts

Interface Ambilight: Interface + Single DC-DC

PHILIPS


AB1 INTERFACE + SINGLE DC-DC
AB1
1M85
1M84
502382-1470
502382-1470
F126
SPI-LATCH2CONN
F101 SPI-CLOCK-BUF
F102 SPI-DATA-OUT
F103 SPI-DATA-RETURN
F104 SPI-LATCH1CONN
F105 PWM-CLOCK-BUF
F106 +3V3
F108 BLANK-BUF
F109 EEPROM-CS
F110 TEMP-SENSOR
F111 PROG
F112 VLED1
F113 VLED2
F125
9101
9102(RES)
9103(RES)
9104
SPI-LATCH1
SPI-LATCH1CONN
SPI-LATCH2CONN
SPI-LATCH2
1M59
1735446-7
F115 SCL
F116 SDA
F117 3109 100R RES CONTROL1
F118 3110 100R RES CONTROL2
F119 +3V3
F120
2108 100p RES
1M90
1735446-6
F121 +24V
F122
F123 +24V
F124 +24V
2109 100p RES
+12V c001 VLED1
+16V c002 VLED2
5107 RES 30R
5108 RES 30R
+24VF
+24V
1100 T 3.0A 32V
I100
5102 10u
2100 220n
F107
1101 * 2.0A T 63V
I109
5100 RES 30R
5101 RES 30R
+16V
5103 * 30R
5104 * 30R
+12V
5105 * 30R
5106 * 30R
+16V
RES
3100 0R1
F114
2101 10n
3112 100R
7100 NCP3163BMNR2G
VCC
LPK_SENSE
LVI_OUT
DRV_COL
SWI_EMIT
SWI_COL
BOOT_IN
VFB
TIM_CAP
NC
VIA
GND
GND_HS
3101 47R
I101
2102 2n2
I103
I102
I108
3104 330R
2103 220p
3102 15K
6100 SS24
VSW
3103 3K3
I104
2105 100n
2106 100n
+16V
2104 100n
I105
3105 1M0
3106 33K 1%
3107 12K
I106
3111 100K
3108 3K3 1%
2107 100n

1100	A6	F123	E2
1101	A7	F124	E2
1M59	C2	F125	B3
1M84	A2	F126	A2
1M85	A2	I100	A6
1M90	D2	I101	C6
2100	A6	I102	C6
2101	B5	I103	C6
2102	C6	I104	D9
2103	D6	I105	D5
2104	D5	I106	D7
2105	D9	I108	D6
2106	D9	I109	A8
2107	E9	c001	E2
2108	D3	c002	E2
2109	E3		
3100	B5		
3101	C5		
3102	D6		
3103	D9		
3104	D6		
3105	D5		
3106	D5		
3107	D5		
3108	E9		
3109	D2		
3110	D3		
3111	E8		
3112	B6		
5100	A8		
5101	A8		
5102	A7		
5103	B8		
5104	B8		
5105	B8		
5106	B8		
5107	A6		
5108	A6		
6100	C8		
7100	B7		
9101	C3		
9102	C3		
9103	C3		
9104	C3		
F101	B3		
F102	B3		
F103	B3		
F104	B3		
F105	B3		
F106	B3		
F107	A7		
F108	B3		
F109	B3		
F110	B3		
F111	B3		
F112	B3		
F113	B3		
F114	B5		
F115	C2		
F116	D2		
F117	D2		
F118	D2		
F119	D2		
F120	D2		
F121	E2		
F122	E2		

STUFFING DIVERSITIES FOR DC/DC INTERFACE AMBI 2K9

DC/DC INTERFACE	1101	1M85	5103/5104	5105/5106	VLED1	VLED2
3104 328 58341	in	in	in	out	24V	16V
3104 328 58351	out	out	out	in	12V	12V
3104 328 58361	out	out	out	in	16V	16V
3104 328 58371	out	out	out	out	12V	16V

See the stuffing diversities table in the case of components marked with one star (*)

CHN
SETNAME
CLASS_NO
DC-DC INTERFACE
AMBI 2K9
3104 313 6325

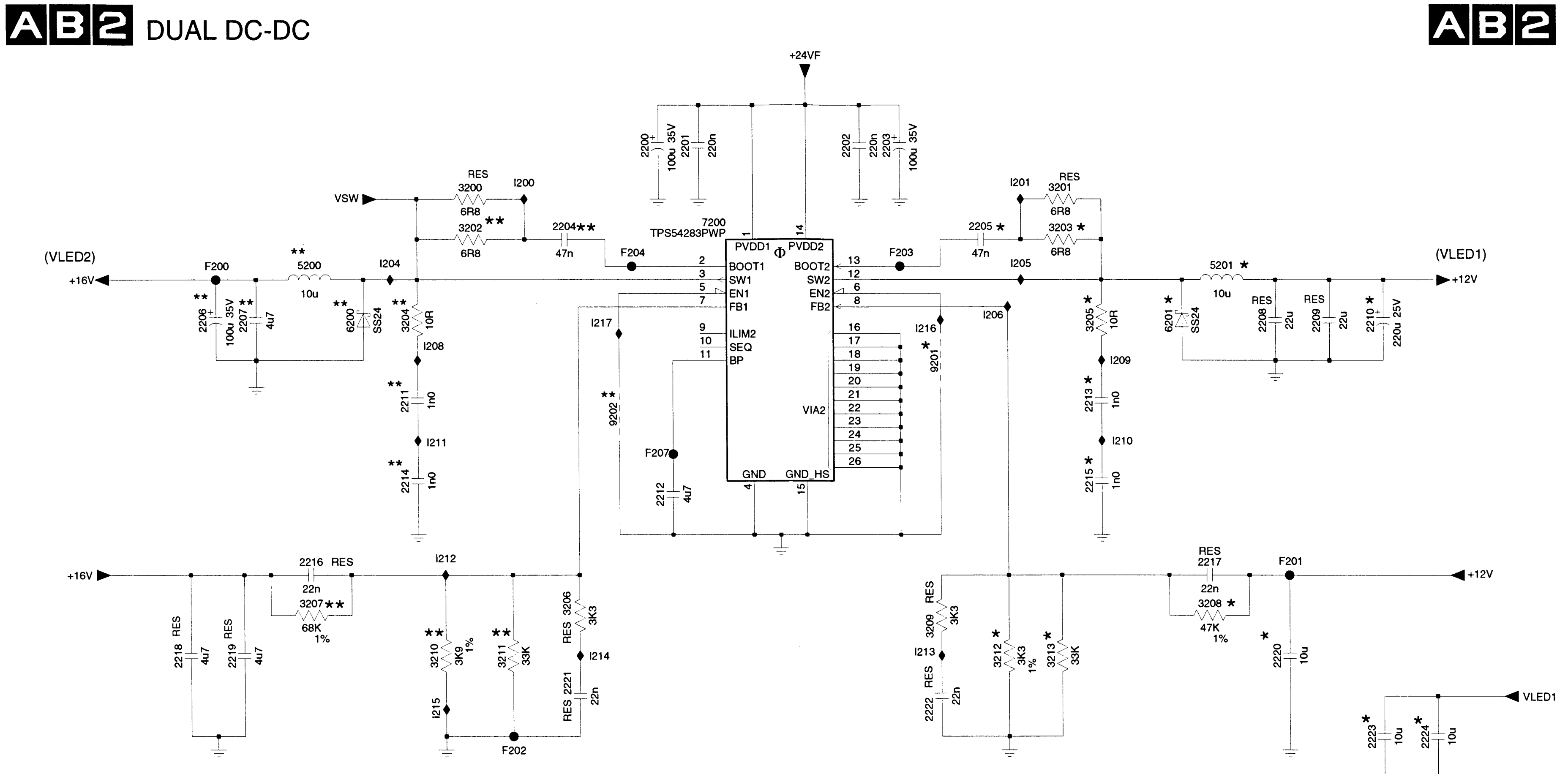
08-06-19	1
08-08-06	2
08-10-23	3

1	08-06-19
2	08-08-06
3	08-09-18
4	08-10-23
5	08-12-06

NAME Peter Van Hove
SUPERS. 3
CT MGr CHECK ********
DATE 08-06-06
** 130 - 1
*** A3

18310_600_090305.eps
090305

Interface Ambilight: Dual DC-DC


AB2
DUAL DC-DC
AB2
+24VF
2200 100u 35V
2201 220n
2202 220n
2203 100u 35V
VSW
RES 3200 6R8
I200
3202 ** 6R8
2204** 47n
7200 TPS54283PWP
PVDD1
PVDD2
BOOT1
SW1
EN1
FB1
ILIM2
SEQ
BP
BOOT2
SW2
EN2
FB2
VIA2
GND
GND_HS
F204
F203
F207
2212 4u7
I217
9202 **
I216
9201 *
I206
(VLED2)
+16V
F200
5200 ** 10u
I204
2206 ** 100u 35V
2207 ** 4u7
6200 ** SS24
3204 ** 10R
I208
2211 ** 1n0
I211
2214 ** 1n0
I201
RES 3201 6R8
2205 * 47n
3203 * 6R8
I205
(VLED1)
+12V
5201 * 10u
3205 * 10R
I209
2213 * 1n0
I210
2215 * 1n0
6201 * SS24
RES 2208 22u
RES 2209 22u
2210 * 220u 25V
+16V
2216 RES 22n
3207 ** 68K 1%
I212
RES 2218 4u7
RES 2219 4u7
3210 ** 3K9 1%
3211 ** 33K
RES 3206 3K3
I214
RES 2221 22n
I215
F202
RES 3209 3K3
I213
RES 2222 22n
3212 * 3K3 1%
3213 * 33K
RES 2217 22n
3208 * 47K 1%
F201
+12V
2220 * 10u
VLED1
2223 * 10u
2224 * 10u

7200 : TPS54383 in case of 16V or dual dc-dc converter

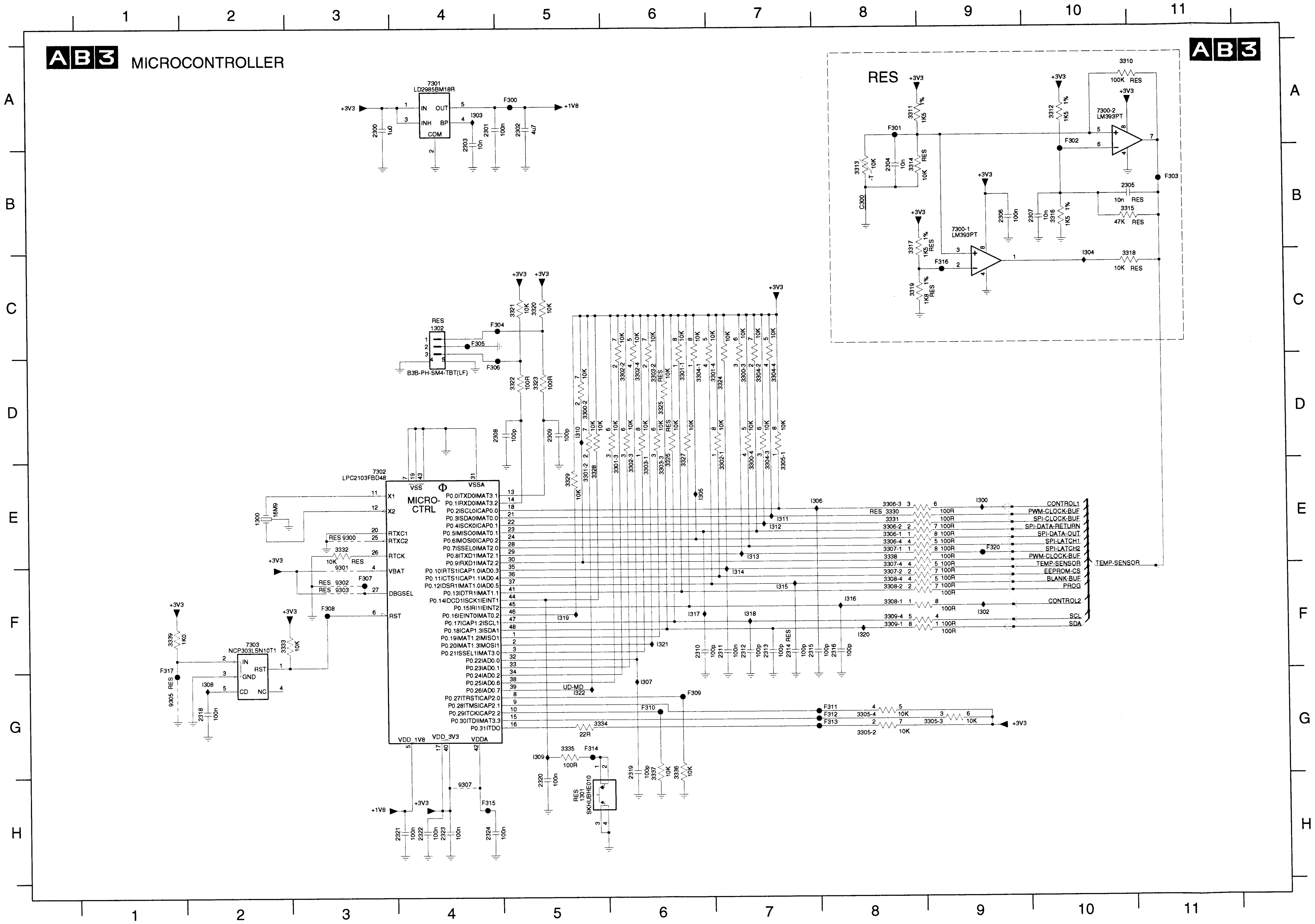
The components marked with one star (*) belong to the 12V versions (3104 328 58351, 3104 328 58371).

The components marked with two stars (**) belong to the 16V versions (3104 328 58331, 3104 328 58341, 3104 328 58361, 3104 328 58371).

2200	A4
2201	A4
2202	A5
2203	A5
2204	B3
2205	B6
2206	B1
2207	B2
2208	B7
2209	B7
2210	B8
2211	C3
2212	C4
2213	C6
2214	C3
2215	C6
2216	C2
2217	C7
2218	D1
2219	D2
2220	D7
2221	D3
2222	D5
2223	D8
2224	D8
3200	A3
3201	A6
3202	B3
3203	B6
3204	B3
3205	B6
3206	D3
3207	D2
3208	D7
3209	D5
3210	D3
3211	D3
3212	D6
3213	D6
5200	B2
5201	B7
6200	B2
6201	B7
7200	B4
9201	B5
9202	C4
F200	B2
F201	C7
F202	D3
F203	B5
F204	B4
F207	C4
I200	A3
I201	A6
I204	B2
I205	B6
I206	B6
I208	B3
I209	B6
I210	C6
I211	C3
I212	C3
I213	D5
I214	D4
I215	D3
I216	B5
I217	B4

CHN	SETNAME		
CLASS_NO	DC-DC INTERFACE AMBI 2K9	3104 313 6325	
08-06-19 1 08-08-06 2 08-10-23 3			1 08-06-19 2 08-08-06 3 08-09-18 4 08-10-23 5 08-12-06
NAME Peter Van Hove	SUPERS. 3	130 - 2	A3
CHECK	DATE 08-06-09		

Interface Ambilight: Microcontrollerblock


AB3
MICROCONTROLLER
RES
7301
LD2985BM18R
IN
OUT
INH
BP
COM
+3V3
+1V8
F300
7300-1
LM393PT
7300-2
LM393PT
TEMP-SENSOR
7302
LPC2103FBD48
MICRO-
CTRL
VSS
VSSA
X1
X2
RTXC1
RTXC2
RTCK
VBAT
DBGSEL
RST
VDD_1V8
VDD_3V3
VDDA
P0.0|TXD0|MAT3.1
P0.1|RXD0|MAT3.2
P0.2|SCL0|CAP0.0
P0.3|SDA0|MAT0.0
P0.4|SCK0|CAP0.1
P0.5|MISO0|MAT0.1
P0.6|MOSI0|CAP0.2
P0.7|SSEL0|MAT2.0
P0.8|TXD1|MAT2.1
P0.9|RXD1|MAT2.2
P0.10|RTS1|CAP1.0|AD0.3
P0.11|CTS1|CAP1.1|AD0.4
P0.12|DSR1|MAT1.0|AD0.5
P0.13|DTR1|MAT1.1
P0.14|DCD1|SCK1|EINT1
P0.15|RI1|EINT2
P0.16|EINT0|MAT0.2
P0.17|CAP1.2|SCL1
P0.18|CAP1.3|SDA1
P0.19|MAT1.2|MISO1
P0.20|MAT1.3|MOSI1
P0.21|SSEL1|MAT3.0
P0.22|AD0.0
P0.23|AD0.1
P0.24|AD0.2
P0.25|AD0.6
P0.26|AD0.7
P0.27|TRST|CAP2.0
P0.28|TMS|CAP2.1
P0.29|TCK|CAP2.2
P0.30|TDI|MAT3.3
P0.31|TDO
7303
NCP303LSN10T1
IN
RST
GND
CD
NC
1300
16M0
B3B-PH-SM4-TBT(LF)
RES
1302
SKHUBHE010
RES
1301
UD-MD
CONTROL1
PWM-CLOCK-BUF
SPI-CLOCK-BUF
SPI-DATA-RETURN
SPI-DATA-OUT
SPI-LATCH1
SPI-LATCH2
PWM-CLOCK-BUF
TEMP-SENSOR
EEPROM-CS
BLANK-BUF
PROG
CONTROL2
SCL
SDA

1300 E2	9303 F3
1301 H5	9305 G1
1302 C4	9307 H4
2300 A3	C300 B8
2301 A4	F300 A5
2302 A5	F301 A8
2303 A4	F302 A10
2304 B8	F303 B11
2305 B10	F304 C4
2306 B9	F305 C4
2307 B10	F306 D4
2308 D4	F307 F3
2309 D5	F308 F3
2310 F6	F309 G6
2311 F7	F310 G6
2312 F7	F311 G8
2313 F7	F312 G8
2314 F7	F313 G8
2315 F7	F314 G5
2316 F8	F315 H4
2318 G2	F316 C9
2319 G6	F317 F1
2320 H5	F320 E9
2321 H4	I300 E9
2322 H4	I302 F9
2323 H4	I303 A4
2324 H4	I304 C10
3300-2 D5	I305 E6
3300-3 D7	I306 E7
3300-4 D7	I307 G6
3301-1 D6	I308 G2
3301-2 E5	I309 G5
3301-3 E6	I310 D5
3301-4 D7	I311 E7
3302-1 D7	I312 E7
3302-2 D6	I313 E7
3302-3 E6	I314 F7
3302-4 D6	I315 F7
3303-1 E6	I316 F8
3303-2 D6	I317 F6
3303-3 E6	I318 F7
3304-1 D6	I319 F5
3304-2 D7	I320 F8
3304-3 D7	I321 F6
3304-4 D7	I322 G5
3305-1 E7	
3305-2 G8	
3305-3 G9	
3305-4 G8	
3306-1 E8	
3306-2 E8	
3306-3 E8	
3306-4 E8	
3307-1 E8	
3307-2 F8	
3307-4 F8	
3308-1 F8	
3308-2 F8	
3308-4 F8	
3309-1 F8	
3309-4 F8	
3310 A10	
3311 A8	
3312 A10	
3313 B8	
3314 B8	
3315 B10	
3316 B10	
3317 B8	
3318 C10	
3319 C8	
3320 C5	
3321 C5	
3322 D5	
3323 D5	
3324 D7	
3325 D6	
3326 D6	
3327 D6	
3328 E5	
3329 E5	
3330 E8	
3331 E8	
3332 E3	
3333 F2	
3334 G5	
3335 G5	
3336 G6	
3337 G6	
3338 E8	
3339 F1	
7300-1 B9	
7300-2 A10	
7301 A4	
7302 E3	
7303 F2	
9300 E3	
9301 F3	
9302 F3	

PHILIPS

CHN
SETNAME
CLASS_NO

08-06-19	1
08-08-06	2
08-10-23	3

DC-DC INTERFACE
AMBI 2K9

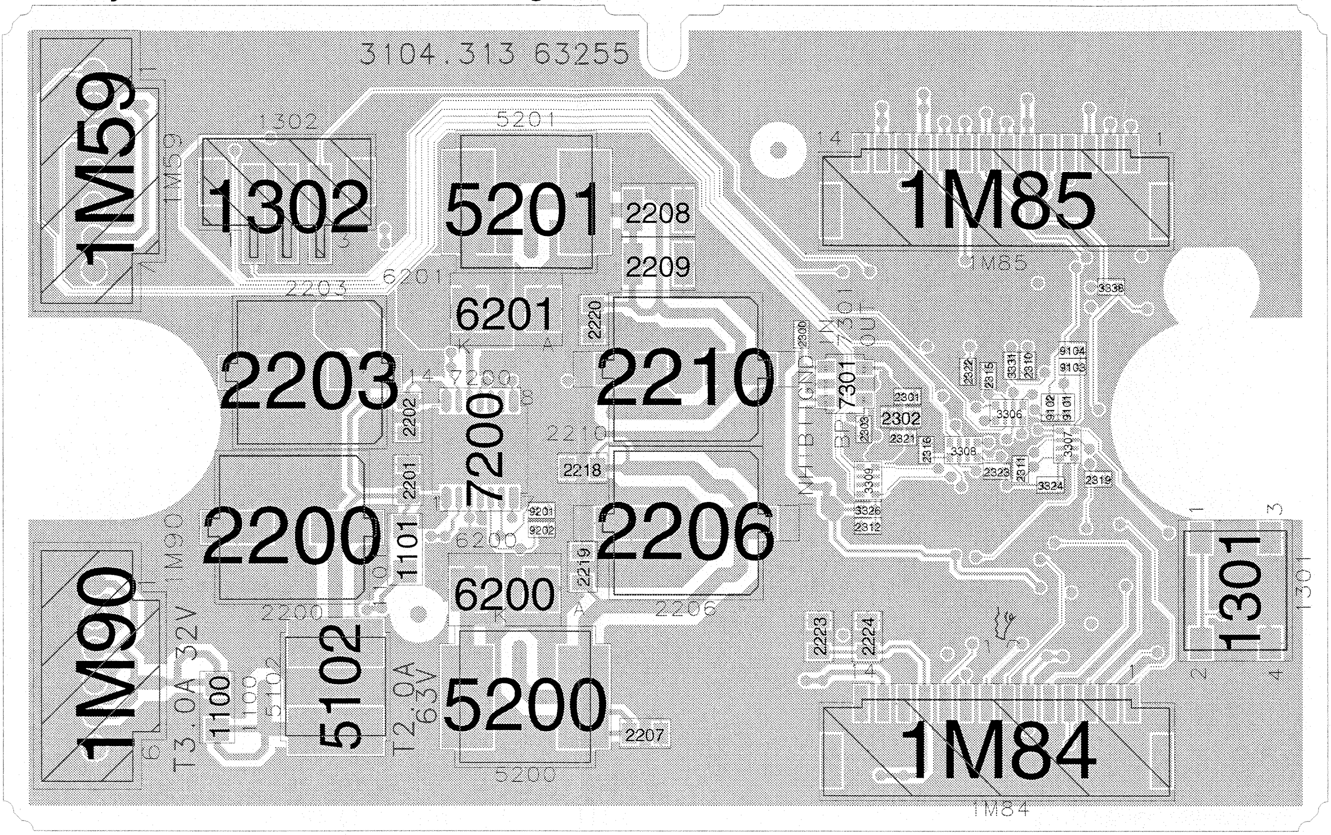
3104 313 6325

1	08-06-19
2	08-08-06
3	08-09-18
4	08-10-23
5	08-12-06

NAME Peter Van Hove
SUPERS. 3
130 – 3
A2
CHECK
DATE 08-06-09

18310_602_090305.eps
090410

Layout DC/DC Interface Ambilight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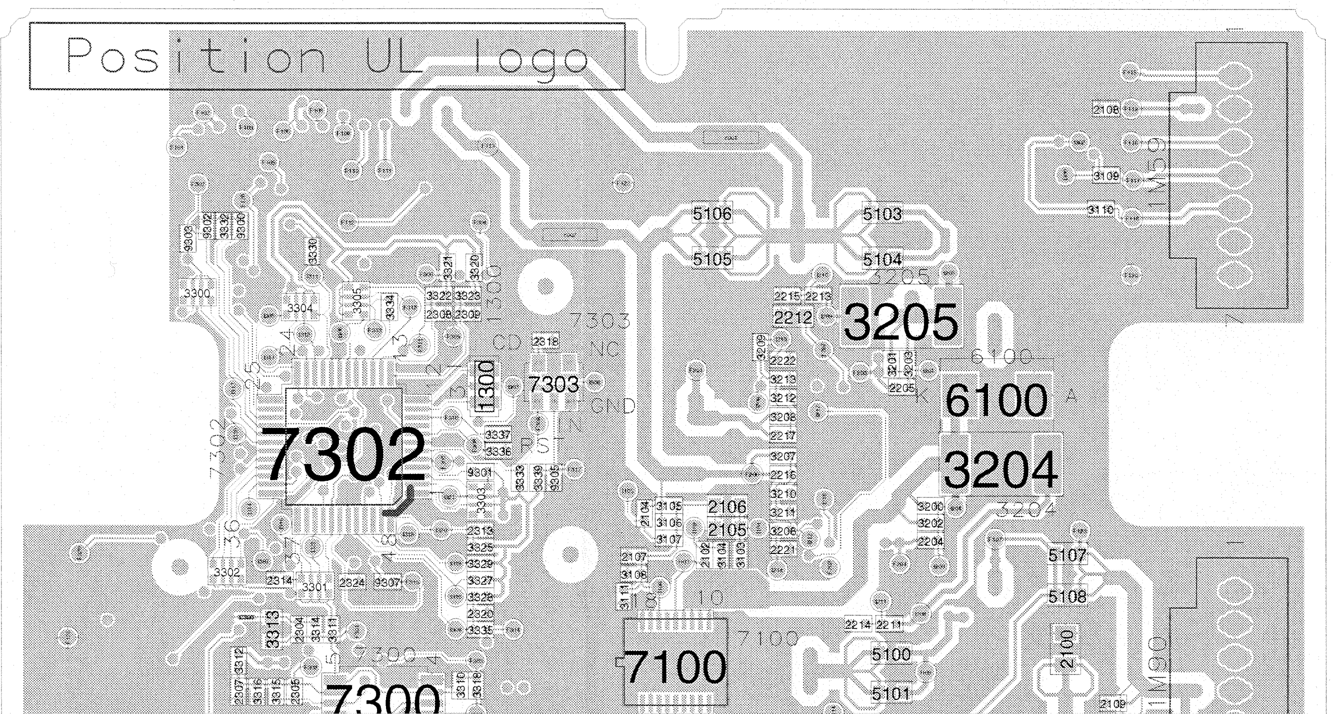
1M59
1302
5201
2208
2209
1M85
6201
2220
2203
7200
2202
2210
2201
2218
2200
1101
9201
9202
2206
6200
2219
7301
2300
2301
2302
2321
3308
2316
2323
3311
3324
2319
3309
3326
2312
2322
2315
3331
2310
9104
9103
9102
9101
3306
3307
3336
1M90
1100
5102
T3.0A 32V
T2.0A 63V
5200
2207
2223
2224
1301
1M84


Position UL logo
2108
3109
3110
5106
5103
5105
5104
3303
3302
3332
9300
3330
3300
3304
3305
3334
3321
3320
3322
3323
2308
2309
1300
7303
2318
3205
2215
2213
2212
3209
2222
3213
3212
3208
2217
3207
2216
3210
3211
3206
2221
3201
3203
2205
6100
3204
3200
3202
2204
7302
3337
3336
9801
3333
3339
9305
3303
2313
3325
3329
3327
3328
2320
3335
2104
3105
3106
3107
2106
2105
2102
3104
3103
2107
3108
3111
5107
5108
3302
2314
3301
2324
3307
3313
2304
3314
3311
2307
3312
3316
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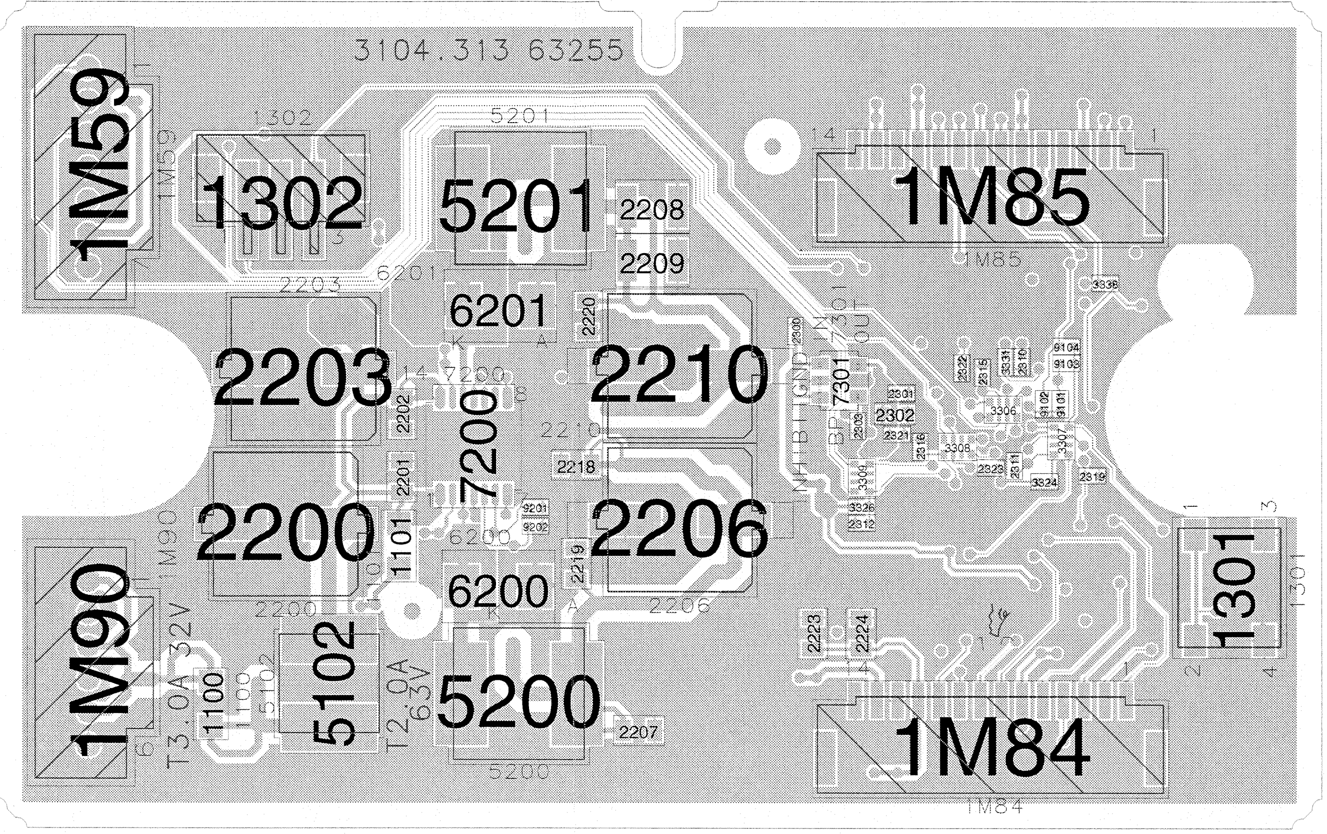
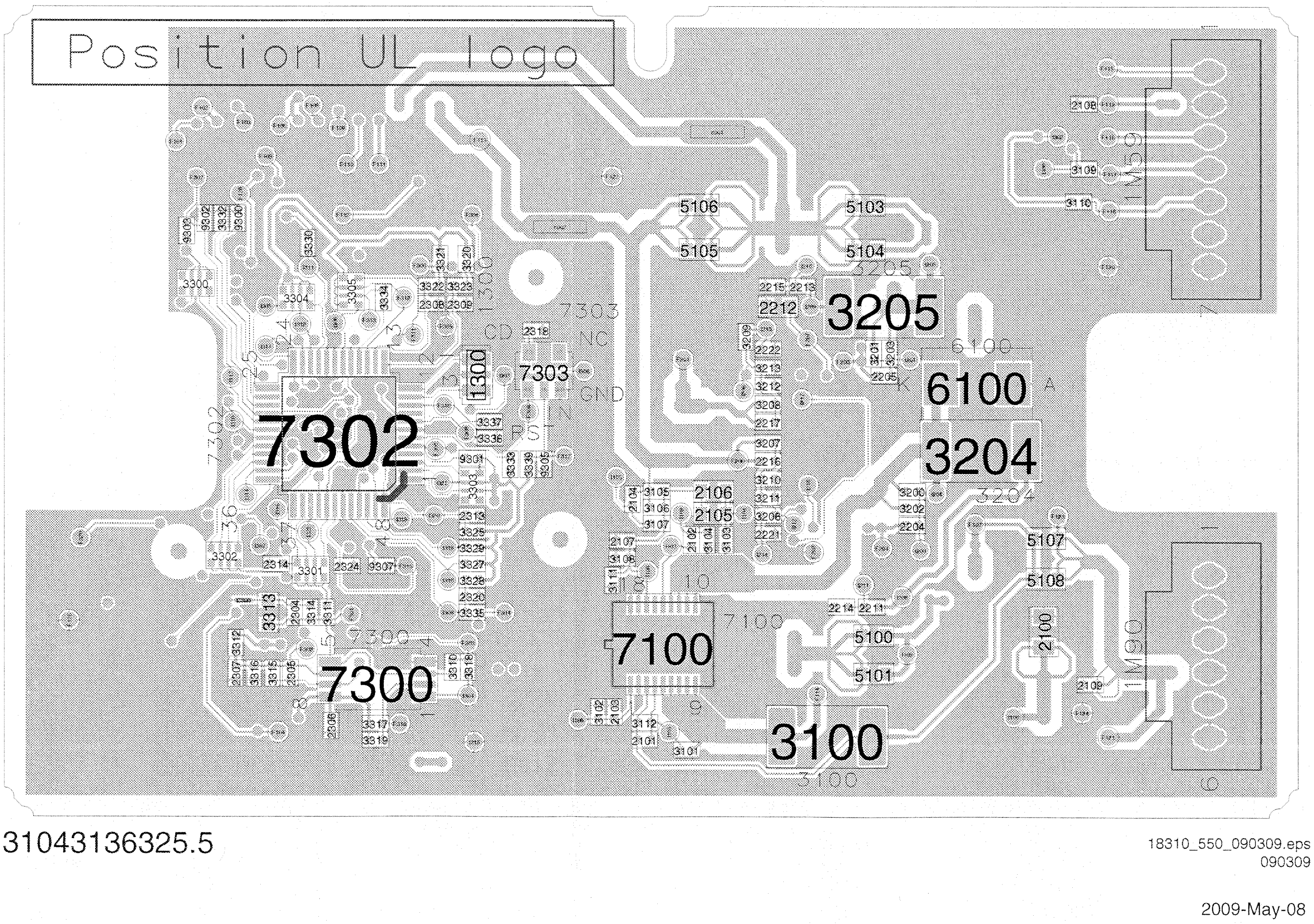
7300
3310
3318
7100
2214
2211
5100
5101
2100
2109
1M90

Layout DC/DC Interface Ambilight


3104.313 63255
1M59
1302
5201
2208
2209
1M85
2203
6201
2220
2210
7301
7200
2202
2201
2218
2200
1101
9201
9202
6200
2219
2206
1M90
1100
5102
5200
2207
2223
2224
1301
1M84
T3.0A 32V
T2.0A 63V
2301
2302
2303
2321
2316
3308
3309
3326
2312
3306
3307
3324
2319
2323
2311
9104
9103
9102
9101
3336
2322
2315
3331
2810


Position UL logo
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3109
3110
1M50
5106
5103
5105
5104
3205
2215
2213
2212
3303
3302
3332
3330
3300
3304
3305
3321
3320
3322
3323
2308
2309
2318
7303
CD
NC
GND
RST
1300
7302
3337
3336
9301
3303
3338
3339
2313
3325
3329
3327
3328
2320
3335
3302
2314
3301
2324
9307
3313
2304
3314
3311
2307
3312
3316
3315
2305
7300
3310
3318
2306
3317
3319
3209
2222
3213
3212
3208
2217
3207
2216
3211
3206
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3201
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6100
3204
3200
3202
2204
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3106
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3104
3103
2107
3108
3111
7100
3102
2103
3112
2101
3101
3100
2214
2211
5100
5101
5107
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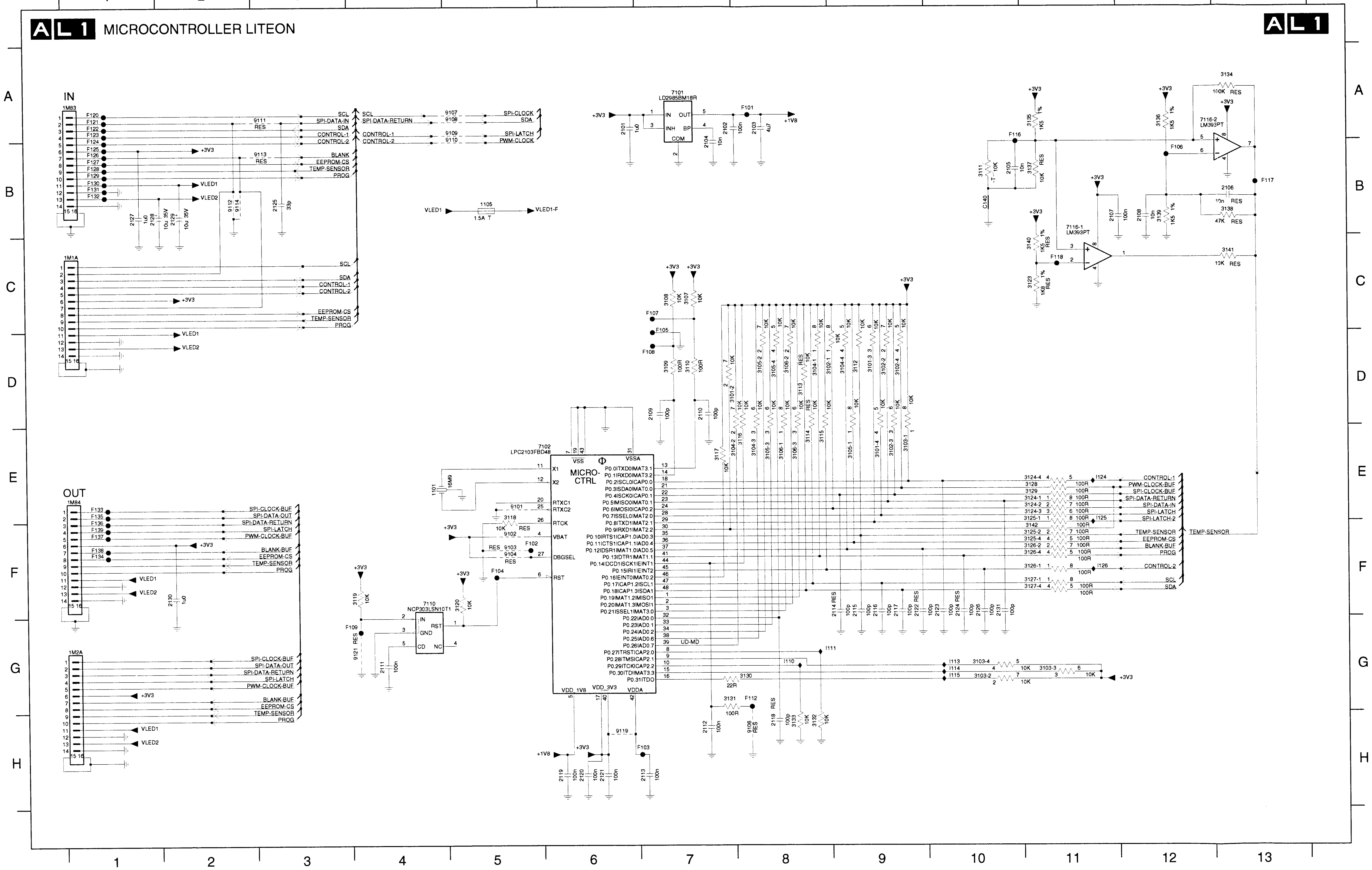
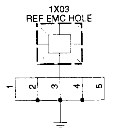
2100
2109
1M90

31043136325.5

18310_550_090309.eps
090309

6 LED Low-Pow: Microcontroller Block Liteon


AL1 MICROCONTROLLER LITEON
AL1
IN
1M83
OUT
1M84
1M1A
1M2A
SCL
SDA
SPI-DATA-IN
SPI-DATA-RETURN
SPI-CLOCK
SPI-LATCH
PWM-CLOCK
CONTROL-1
CONTROL-2
BLANK
EEPROM-CS
TEMP-SENSOR
PROG
SPI-CLOCK-BUF
SPI-DATA-OUT
SPI-LATCH
PWM-CLOCK-BUF
BLANK-BUF
VLED1
VLED2
VLED1-F
+3V3
+1V8
7101
LD2985BM18R
IN
OUT
INH
BP
COM
1105
1.5A T
7102
LPC2103FBD48
MICRO-CTRL
VSS
VSSA
X1
X2
RTXC1
RTXC2
RTCK
VBAT
DBGSEL
RST
VDD_1V8
VDD_3V3
VDDA
1101
16M
7110
NCP303LSN10T1
RST
GND
CD
NC
7116-1
LM393PT
7116-2
LM393PT
F117
TEMP-SENSOR
UD-MD
1X03
REF EMC HOLE


1X03
REF EMC HOLE

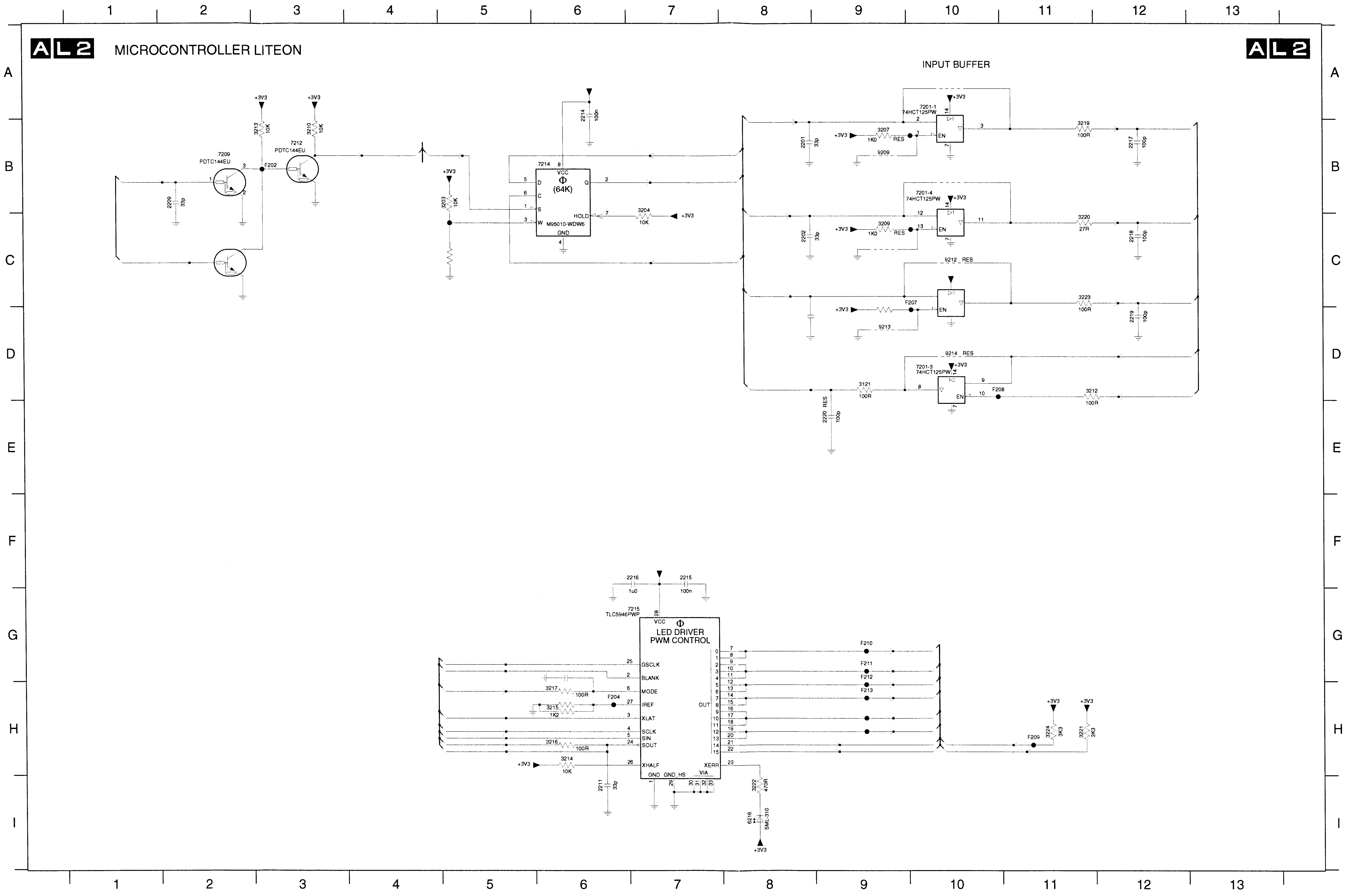
1101 E4
1105 B5
1M1A C1
1M2A G1
1M83 A1
1M84 E1
2101 A6
2102 A7
2103 A8
2104 B7
2105 B10
2106 B13
2107 B11
2108 B12
2109 D7
2110 D7
2111 G4
2112 H7
2113 H7
2114 F9
2115 F9
2116 F9
2117 F9
2118 H8
2119 H6
2120 H6
2121 H6
2122 F9
2123 F10
2124 F10
2125 B3
2126 F10
2127 B1
2128 B1
2129 B2
2130 F2
2131 F10
3101-2 D7
3101-3 D9
3101-4 E9
3102-1 D9
3102-2 D9
3102-3 E9
3102-4 D9
3103-1 E9
3103-2 G10
3103-3 G11
3103-4 G10
3104-1 D8
3104-2 E8
3104-3 E8
3104-4 D9
3105-1 E9
3105-2 D8
3105-3 E8
3105-4 D8
3106-1 E8
3106-2 D8
3106-3 E8
3107 C7
3108 C7
3109 D7
3110 D7
3111 B10
3112 D9
3113 D8
3114 E8
3115 E8
3116 E8
3117 E7
3118 E5
3119 F4
3120 F5
3123 C11
3124-1 E11
3124-2 E11
3124-3 E11
3124-4 E11
3125-1 F11
3125-2 F11
3125-4 F11
3126-1 F11
3126-2 F11
3126-4 F11
3127-1 F11
3127-4 F11
3128 E11
3129 E11
3130 G8
3131 G7
3132 H8
3133 H8
3134 A13
3135 A11
3136 A12
3137 B11
3138 B13
3139 B12
3140 C11
3141 C13
3142 F11
7101 A7
7102 E6
7110 F4
7116-1 B11
7116-2 A12
9101 E5
9102 F5
9103 F5
9104 F5
9106 H8
9107 A5
9108 A5
9109 A5
9110 B5
9111 A3
9112 B2
9113 B3
9114 B2
9119 H6
9121 G4
C140 B10
F101 A8
F102 F5
F103 H7
F104 F5
F105 D7
F106 B12
F107 C7
F108 D7
F109 G3
F112 G8
F116 A10
F117 B13
F118 C11
F120 A1
F121 A1
F122 A1
F123 A1
F124 B1
F125 B1
F126 B1
F127 B1
F128 B1
F129 B1
F130 B1
F131 B1
F132 B1
F133 E1
F134 F1
F135 E1
F136 F1
F137 F1
F138 F1
F139 F1
I110 G8
I111 G8
I113 G10
I114 G10
I115 G10
I124 E11
I125 E11
I126 F11

CHN	SETNAME			
CLASS_NO	DRIVER 6LED LITEON 2K9	8204 000 8857	1	2008-06-10
			2	2008-08-08
2008-08-08 2			3	2008-10-27
2008-10-27 3				
NAME Peter Van Hove	SUPERS. 3	130 - 1		A2
CHECK	DATE 2008-06-02			

PHILIPS

18310_610_090305.eps
090410

6 LED Low-Pow: Microcontroller Block Liteon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MICROCONTROLLER LITEON
INPUT BUFFER
+3V3
3213 10K
3210 10K
7209 PDTC144EU
7212 PDTC144EU
F202
2209 33p
2214 100n
3203 10K
7214
VCC
(64K)
D
C
S
W
Q
HOLD
M95010-WDW6
GND
3204 10K
7201-1 74HCT125PW
7201-4 74HCT125PW
7201-3 74HCT125PW
EN
2201 33p
2202 33p
3207 1K0 RES
3209 1K0 RES
9209
9212 RES
9213
9214 RES
F207
F208
3121 100R
2220 RES 100p
3219 100R
3220 27R
3223 100R
3212 100R
2217 100p
2218 100p
2219 100p
2216 1u0
2215 100n
7215 TLC5946PWP
LED DRIVER PWM CONTROL
GSCLK
BLANK
MODE
IREF
XLAT
SCLK
SIN
SOUT
XHALF
XERR
GND
GND_HS
VIA
OUT
3217 100R
3215 1K2
3216 100R
3214 10K
F204
2211 33p
3222 470R
6216 SML-310
F209
F210
F211
F212
F213
3224 3K3
3221 3K3

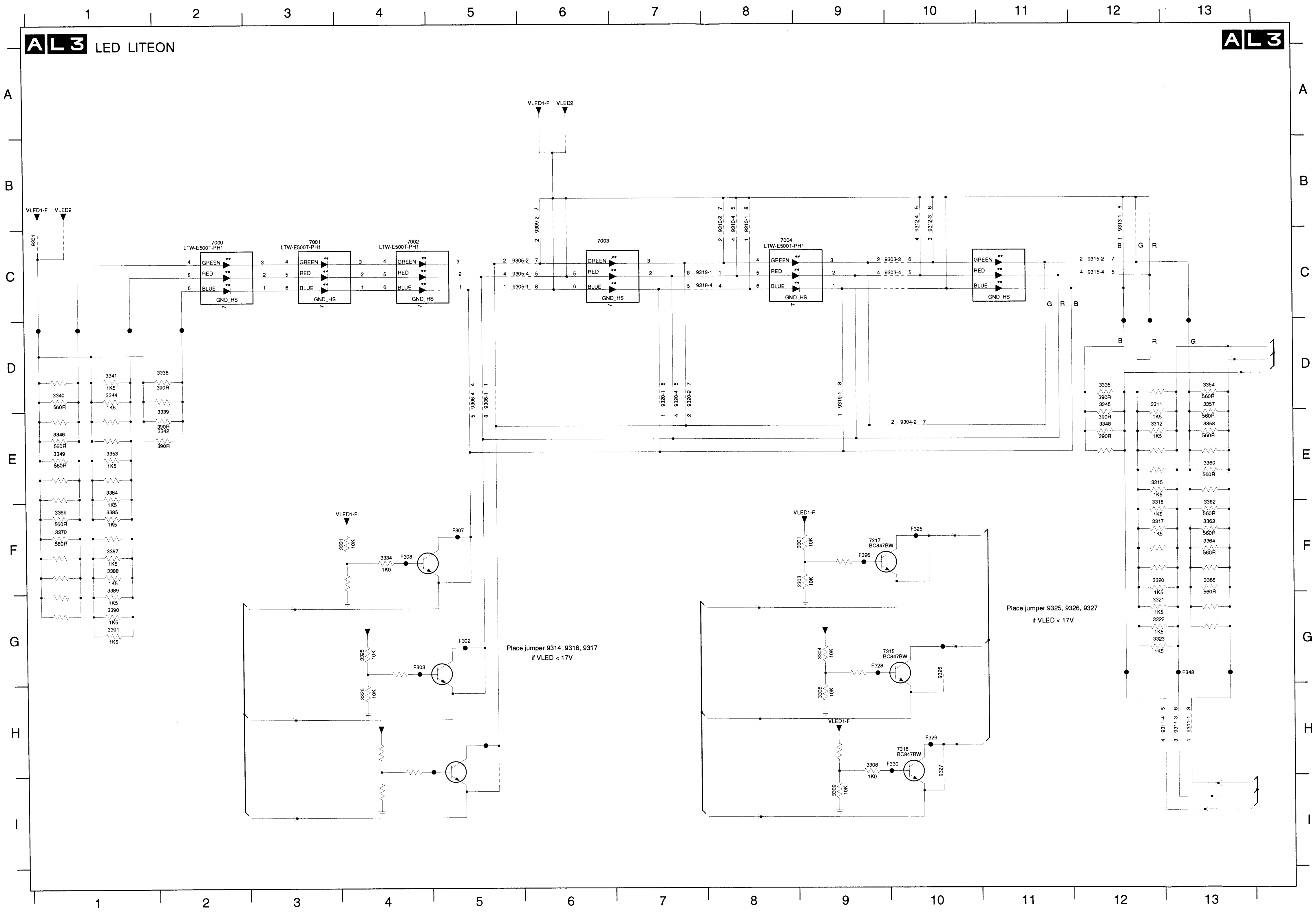
2201	B8
2202	C8
2203	D8
2209	B2
2210	G6
2211	I6
2214	A6
2215	F7
2216	F7
2217	B12
2218	C12
2219	D12
2220	E9
3121	D9
3203	B5
3204	B7
3205	C5
3207	B9
3209	C9
3210	B3
3211	C9
3212	D11
3213	B3
3214	H6
3215	H6
3216	H6
3217	H6
3218	H6
3219	B11
3220	C11
3221	H11
3222	I8
3223	C11
3224	H11
6216	I8
7201-1	A10
7201-2	C10
7201-3	D10
7201-4	B10
7209	B2
7210	C2
7212	B3
7214	B6
7215	G7
9208	A10
9209	B9
9210	B10
9211	C9
9212	C10
9213	D9
9214	D10
F202	B3
F203	C5
F204	H6
F205	B10
F206	C10
F207	C10
F208	D10
F209	H11
F210	G9
F211	G9
F212	G9
F213	H9
F214	H9
F215	H9

PHILIPS

2008-08-08	2	DRIVER 6LED LITEON 2K9	8204 000 8857
2008-10-27	3		
NAME		SUPERS.	- A2
CHECK		DATE	

18310_611_090305.eps
090410

6 LED Low-Pow: LED Liteon


AL3
LED LITEON
VLED1-F
VLED2
9301
7000
LTW-E500T-PH1
7001
LTW-E500T-PH1
7002
LTW-E500T-PH1
7003
7004
LTW-E500T-PH1
GREEN
RED
BLUE
GND_HS
9305-2
9305-4
9305-1
9309-2
9310-2
9310-4
9310-1
9318-1
9318-4
9312-4
9312-3
9303-3
9303-4
9313-1
9315-2
9315-4
B
G
R
9306-4
9306-1
9320-1
9320-4
9320-2
9319-1
9304-2
3341
1K5
3336
390R
3340
560R
3344
3339
3342
3346
3349
3353
3384
3385
3369
3370
3387
3388
3389
3390
3391
VLED1-F
3331
10K
3334
1K0
F308
F307
3325
F302
F303
3326
Place jumper 9314, 9316, 9317
if VLED < 17V
3301
3303
7317
BC847BW
F325
F326
3304
7315
BC847BW
F328
9326
3306
7316
BC847BW
F329
3308
F330
3309
9327
Place jumper 9325, 9326, 9327
if VLED < 17V
3335
3345
3348
3311
3312
3315
3316
3317
3320
3321
3322
3323
3354
3357
3358
3360
3362
3363
3364
3366
F348
9311-4
9311-3
9311-1

3301	F9
3302	F9
3303	F9
3304	G9
3305	G9
3306	H9
3307	H9
3308	H9
3309	I9
3310	D12
3311	D12
3312	E12
3313	E12
3314	E12
3315	E12
3316	E12
3317	F12
3318	F12
3319	F12
3320	F12
3321	G12
3322	G12
3323	G12
3325	G4
3326	H4
3327	H4
3328	G4
3330	I4
3331	F4
3332	F4
3333	H4
3334	F4
3335	D12
3336	D2
3337	D2
3338	D1
3339	D2
3340	D1
3341	D1
3342	E2
3343	D1
3344	D1
3345	D12
3346	E1
3347	D1
3348	E12
3349	E1
3350	E1
3351	E12
3352	E1
3353	E1
3354	D13
3355	E1
3356	E1
3357	D13
3358	E13
3359	E13
3360	E13
3361	E13
3362	E13
3363	F13
3364	F13
3365	F13
3366	F13
3367	G13
3368	G13
3369	F1
3370	F1
3371	F1
3372	F1
3373	F1
3374	G1
3384	E1
3385	F1
3386	F1
3387	F1
3388	F1
3389	F1
3390	G1
3391	G1
7000	C2
7001	C3
7002	C4
7003	C6
7004	C8
7005	C11
7305	G4
7306	H5
7307	F4
7315	G9
7316	H10
7317	F9
9301	C1
9302	C1
9303-1	C10
9303-3	C10
9303-4	C10
9304-1	E10
9304-2	E10
9304-4	E10
9305-1	C6
9305-2	C6
9305-4	C6
9306-1	D5
9306-3	D5
9306-4	D5
9307	A6
9308	A6
9309-1	B6
9309-2	B6
9309-4	B6
9310-1	B8
9310-2	B8
9310-4	B8
9311-1	H13
9311-3	H13
9311-4	H12
9312-1	B10
9312-3	B10
9312-4	B10
9313-1	B12
9313-2	B12
9313-4	B12
9314	G5
9315-1	C12
9315-2	C12
9315-4	C12
9316	H5
9317	F5
9318-1	C8
9318-3	C8
9318-4	C8
9319-1	D9
9319-3	D9
9319-4	D9
9320-1	D7
9320-2	D7
9320-4	D7
9325	F10
9326	G10
9327	H10
F302	G5
F303	G4
F304	H5
F305	H5
F307	F5
F308	F4
F325	F10
F326	F9
F327	G10
F328	G9
F329	H10
F330	H10
F340	D1
F341	D1
F342	D1
F343	D2
F344	D12
F345	D12
F346	D13
F347	G12
F348	G13
F349	G13

CHN
SETNAME
CLASS_NO

DRIVER 6LED LITEON
2K9

8204 000 8857

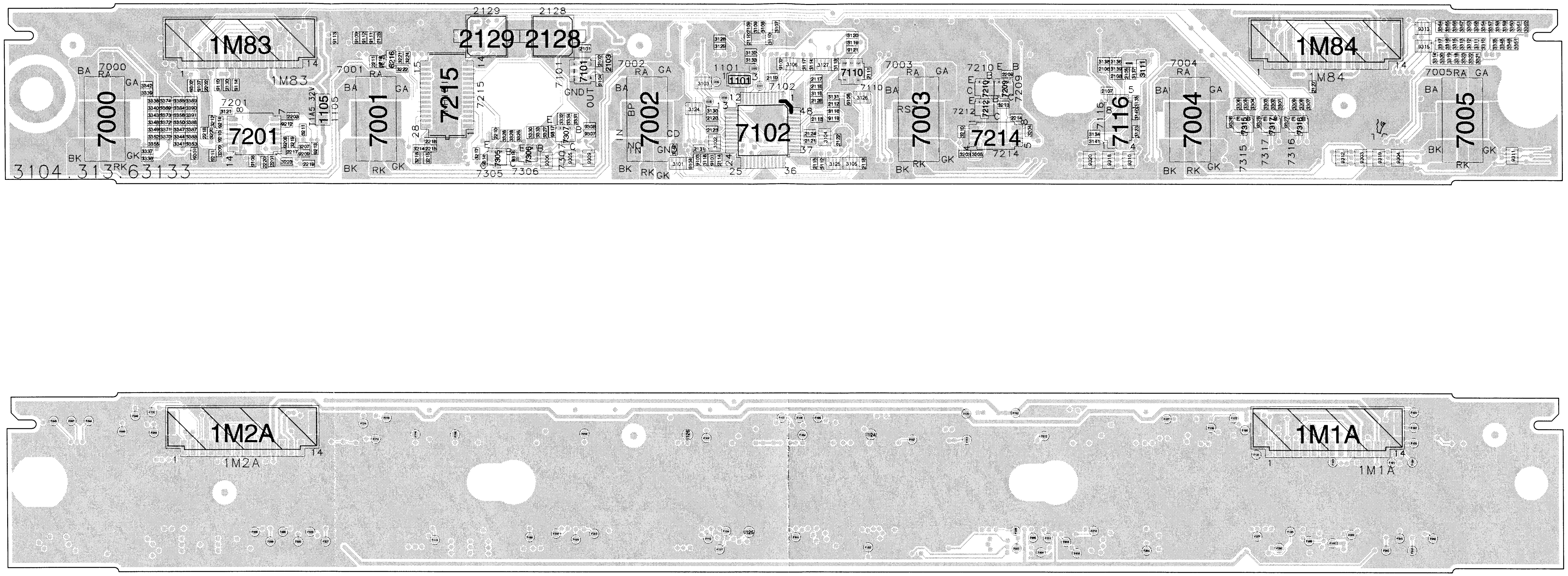
1	2008-06-10
2	2008-08-08
3	2008-10-27

2008-08-08	2
2008-10-27	3

NAME Peter Van Hove
SUPERS. 3
130 – 3
A2
CHECK
DATE 2008-06-02

18310_612_090305.eps
090305

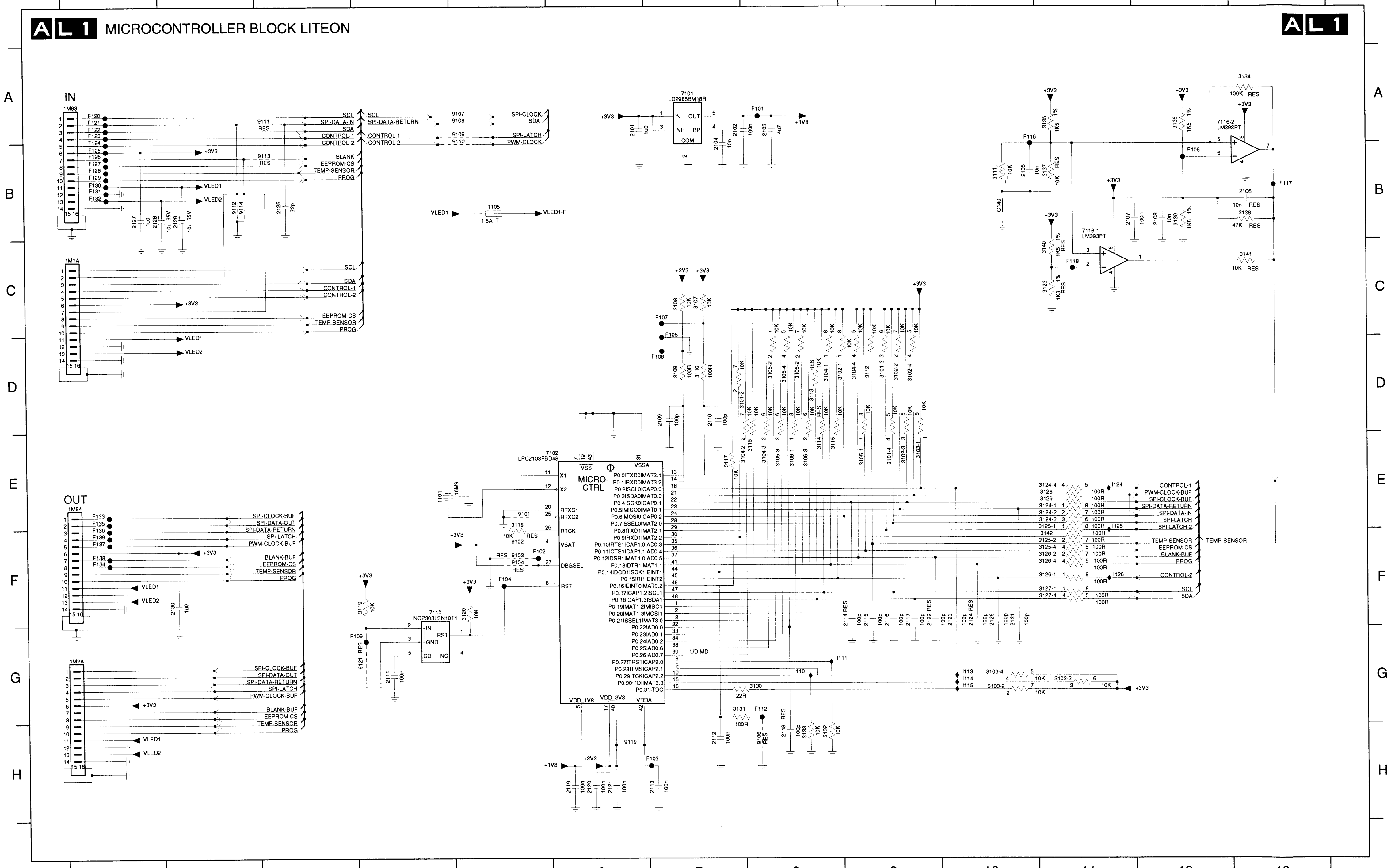
Layout 6 LED Low-Pow

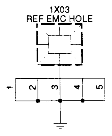

1M83
2129
2128
7215
7000
7201
7001
1105
7002
1101
7102
7110
7003
7210
7214
7116
7004
1M84
7005
3104 313 63133
1M2A
1M1A

3104 313 6313.3

18310_551_090309
090309

8 LED Low-Pow: Microcontroller Block Liteon


AL1
MICROCONTROLLER BLOCK LITEON
AL1
IN
1M83
F120
F121
F122
F123
F124
F125
F126
F127
F128
F129
F130
F131
F132
SCL
SPI-DATA-IN
SDA
CONTROL-1
CONTROL-2
BLANK
EEPROM-CS
TEMP-SENSOR
PROG
9111
RES
9113
RES
+3V3
VLED1
VLED2
2127
2128
1u0
2129
10u 35V
10u 35V
9112
9114
2125
33p
SPI-DATA-RETURN
9107
9108
9109
9110
SPI-CLOCK
SPI-LATCH
PWM-CLOCK
1M1A
7101
LD2985BM18R
IN OUT
INH BP
COM
2101
1u0
2102
10n
2104
100n
2103
4u7
F101
+1V8
1105
1.5A T
VLED1-F
+3V3
3135
1K5 1%
3136
1K5 1%
3134
100K RES
7116-2
LM393PT
F116
F106
3111
10K
2105
10n
3137
10K RES
C140
3123
1K5 1%
3140
1K5 1%
RES
7116-1
LM393PT
F118
2107
100n
2108
10n
3139
1K5 1%
2106
10n RES
3138
47K RES
3141
10K RES
F117
3108
3107
10K
F107
F105
F108
3109
3110
100R
2109
100p
2110
100p
3101-2
3101-3
3101-4
3102-1
3102-2
3102-3
3102-4
3104-1
3104-2
3104-3
3104-4
3105-1
3105-2
3105-3
3105-4
3106-1
3106-2
3106-3
3112
3113
3114
3115
3116
3117
7102
LPC2103FBD48
VSS
VSSA
MICRO-CTRL
X1
X2
RTXC1
RTXC2
RTCK
VBAT
DBGSEL
RST
P0.0/TXD0/MAT3.1
P0.1/RXD0/MAT3.2
P0.2/SCL0/CAP0.0
P0.3/SDA0/MAT0.0
P0.4/SCK0/CAP0.1
P0.5/MISO0/MAT0.1
P0.6/MOSI0/CAP0.2
P0.7/SSEL0/MAT2.0
P0.8/TXD1/MAT2.1
P0.9/RXD1/MAT2.2
P0.10/RTS1/CAP1.0/AD0.3
P0.11/CTS1/CAP1.1/AD0.4
P0.12/DSR1/MAT1.0/AD0.5
P0.13/DTR1/MAT1.1
P0.14/DCD1/SCK1/EINT1
P0.15/RI1/EINT2
P0.16/EINT0/MAT0.2
P0.17/CAP1.2/SCL1
P0.18/CAP1.3/SDA1
P0.19/MAT1.2/MISO1
P0.20/MAT1.3/MOSI1
P0.21/SSEL1/MAT3.0
P0.22/AD0.0
P0.23/AD0.1
P0.24/AD0.2
P0.25/AD0.6
P0.26/AD0.7
P0.27/TRST/CAP2.0
P0.28/TMS/CAP2.1
P0.29/TCK/CAP2.2
P0.30/TDI/MAT3.3
P0.31/TDO
VDD_1V8
VDD_3V3
VDDA
1101
16M0
9101
3118
10K RES
9102
RES 9103
9104
RES
F102
F104
+3V3
3119
10K
F109
9121
RES
7110
NCP303LSN10T1
IN
RST
GND
CD NC
2111
100n
3120
10K
UD-MD
I110
I111
I113
I114
I115
3103-4
3103-3
3103-2
10K
3130
22R
3131
100R
F112
2112
100n
9106
RES
2118
RES
2113
100p
3132
10K
3133
10K
+1V8
+3V3
9119
F103
2119
2120
2121
2113
100n
3124-4
3128
3129
3124-1
3124-2
3124-3
3125-1
3142
3125-2
3125-4
3126-2
3126-4
3126-1
3127-1
3127-4
100R
I124
I125
I126
CONTROL-1
PWM-CLOCK-BUF
SPI-CLOCK-BUF
SPI-DATA-RETURN
SPI-DATA-IN
SPI-LATCH
SPI-LATCH-2
TEMP-SENSOR
EEPROM-CS
BLANK-BUF
PROG
CONTROL-2
SCL
SDA
2114
2115
2116
2117
2122
2123
2124
2126
2131
100p
RES
OUT
1M84
F133
F135
F136
F139
F137
F138
F134
SPI-CLOCK-BUF
SPI-DATA-OUT
SPI-DATA-RETURN
SPI-LATCH
PWM-CLOCK-BUF
BLANK-BUF
EEPROM-CS
TEMP-SENSOR
PROG
2130
1u0
1M2A


1X03
REF EMC HOLE
1
2
3
4
5

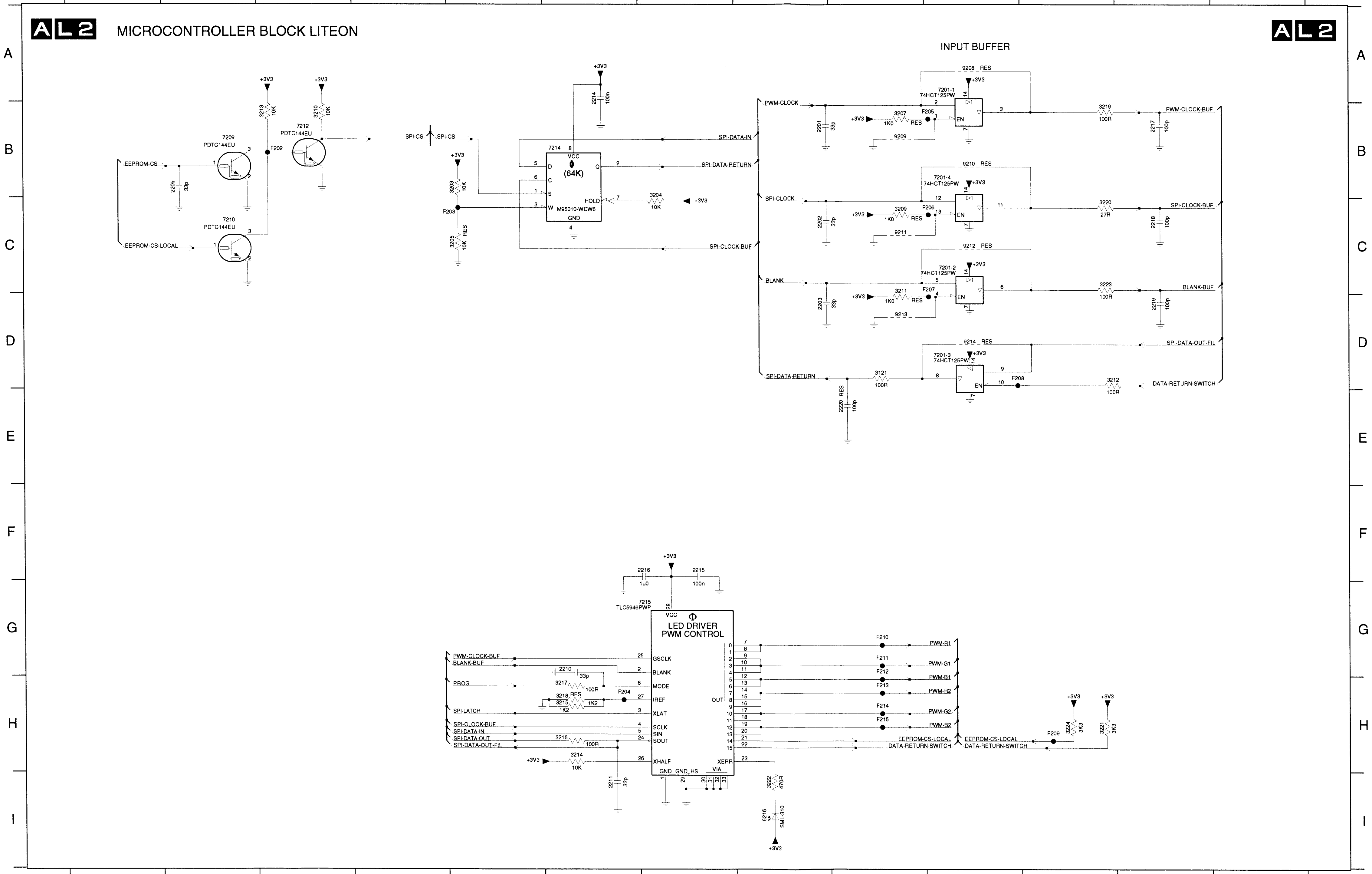
1101	E4
1105	B5
1M1A	C1
1M2A	G1
1M83	A1
1M84	E1
2101	A6
2102	A7
2103	A8
2104	B7
2105	B10
2106	B13
2107	B11
2108	B12
2109	D7
2110	D7
2111	G4
2112	H7
2113	H7
2114	F9
2115	F9
2116	F9
2117	F9
2118	H8
2119	H6
2120	H6
2121	H6
2122	F9
2123	F10
2124	F10
2125	B3
2126	F10
2127	B1
2128	B1
2129	B2
2130	F2
2131	F10
3101-2	D7
3101-3	D9
3101-4	E9
3102-1	D9
3102-2	D9
3102-3	E9
3102-4	D9
3103-1	E9
3103-2	G10
3103-3	G11
3103-4	G10
3104-1	D8
3104-2	E8
3104-3	E8
3104-4	D9
3105-1	E9
3105-2	D8
3105-3	E8
3105-4	D8
3106-1	E8
3106-2	D8
3106-3	E8
3107	C7
3108	C7
3109	D7
3110	D7
3111	B10
3112	D9
3113	D8
3114	E8
3115	E8
3116	E8
3117	E7
3118	E5
3119	F4
3120	F5
3123	C11
3124-1	E11
3124-2	E11
3124-3	E11
3124-4	E11
3125-1	F11
3125-2	F11
3125-4	F11
3126-1	F11
3126-2	F11
3126-4	F11
3127-1	F11
3127-4	F11
3128	E11
3129	E11
3130	G8
3131	G7
3132	H8
3133	H8
3134	A13
3135	A11
3136	A12
3137	B11
3138	B13
3139	B12
3140	C11
3141	C13
3142	F11
7101	A7
7102	E6
7110	F4
7116-1	B11
7116-2	A12
9101	E5
9102	F5
9103	F5
9104	F5
9106	H8
9107	A5
9108	A5
9109	A5
9110	B5
9111	A3
9112	B2
9113	B3
9114	B2
9119	H6
9121	G4
C140	B10
F101	A8
F102	F5
F103	H7
F104	F5
F105	D7
F106	B12
F107	C7
F108	D7
F109	G3
F112	G8
F116	A10
F117	B13
F118	C11
F120	A1
F121	A1
F122	A1
F123	A1
F124	B1
F125	B1
F126	B1
F127	B1
F128	B1
F129	B1
F130	B1
F131	B1
F132	B1
F133	E1
F134	F1
F135	E1
F136	F1
F137	F1
F138	F1
F139	F1
I110	G8
I111	G8
I113	G10
I114	G10
I115	G10
I124	E11
I125	E11
I126	F11

CHN
SETNAME
CLASS_NO
DRIVER 6LED LITEON
2K9
2008-08-08 2
3
8204 000 8857
1 2008-06-10
2 2008-08-08
3 ??
NAME Peter Van Hove
SUPERS.
3
130 - 1
A2
CHECK
DATE 2008-06-02

3104 313 6314.3

18310_650_090508.eps
090507

8 LED Low-Pow: Microcontroller Block Liteon


AL2
MICROCONTROLLER BLOCK LITEON
INPUT BUFFER
+3V3
3213 10K
3210 10K
7212 PDTC144EU
7209 PDTC144EU
7210 PDTC144EU
F202
2209 33p
EEPROM-CS
EEPROM-CS-LOCAL
SPI-CS
2214 100n
3203 10K
F203
3205 10K RES
7214
VCC
(64K)
D
C
S
W
Q
HOLD
M95010-WDW6
GND
3204 10K
SPI-DATA-IN
SPI-DATA-RETURN
SPI-CLOCK-BUF
PWM-CLOCK
SPI-CLOCK
BLANK
9208 RES
7201-1 74HCT125PW
3207 1K0
F205
RES
9209
2201 33p
EN
3219 100R
2217 100p
PWM-CLOCK-BUF
9210 RES
7201-4 74HCT125PW
3209 1K0
F206
9211
2202 33p
3220 27R
2218 100p
SPI-CLOCK-BUF
9212 RES
7201-2 74HCT125PW
3211 1K0
F207
9213
2203 33p
3223 100R
2219 100p
BLANK-BUF
9214 RES
7201-3 74HCT125PW
SPI-DATA-OUT-FIL
3121 100R
2220 RES 100p
F208
3212 100R
DATA-RETURN-SWITCH
2216 1u0
2215 100n
7215 TLC5946PWP
LED DRIVER PWM CONTROL
PWM-CLOCK-BUF
BLANK-BUF
2210 33p
PROG
3217 100R
3218 RES
3215 1K2
1K2
F204
SPI-LATCH
SPI-CLOCK-BUF
SPI-DATA-IN
SPI-DATA-OUT
SPI-DATA-OUT-FIL
3216 100R
3214 10K
2211 33p
GSCLK
BLANK
MODE
IREF
XLAT
SCLK
SIN
SOUT
XHALF
GND GND_HS
VIA
XERR
OUT
3222 470R
6216 SML-310
F210
F211
F212
F213
F214
F215
PWM-B1
PWM-G1
PWM-R1
PWM-R2
PWM-G2
PWM-B2
EEPROM-CS-LOCAL
DATA-RETURN-SWITCH
F209
3224 3K3
3221 3K3

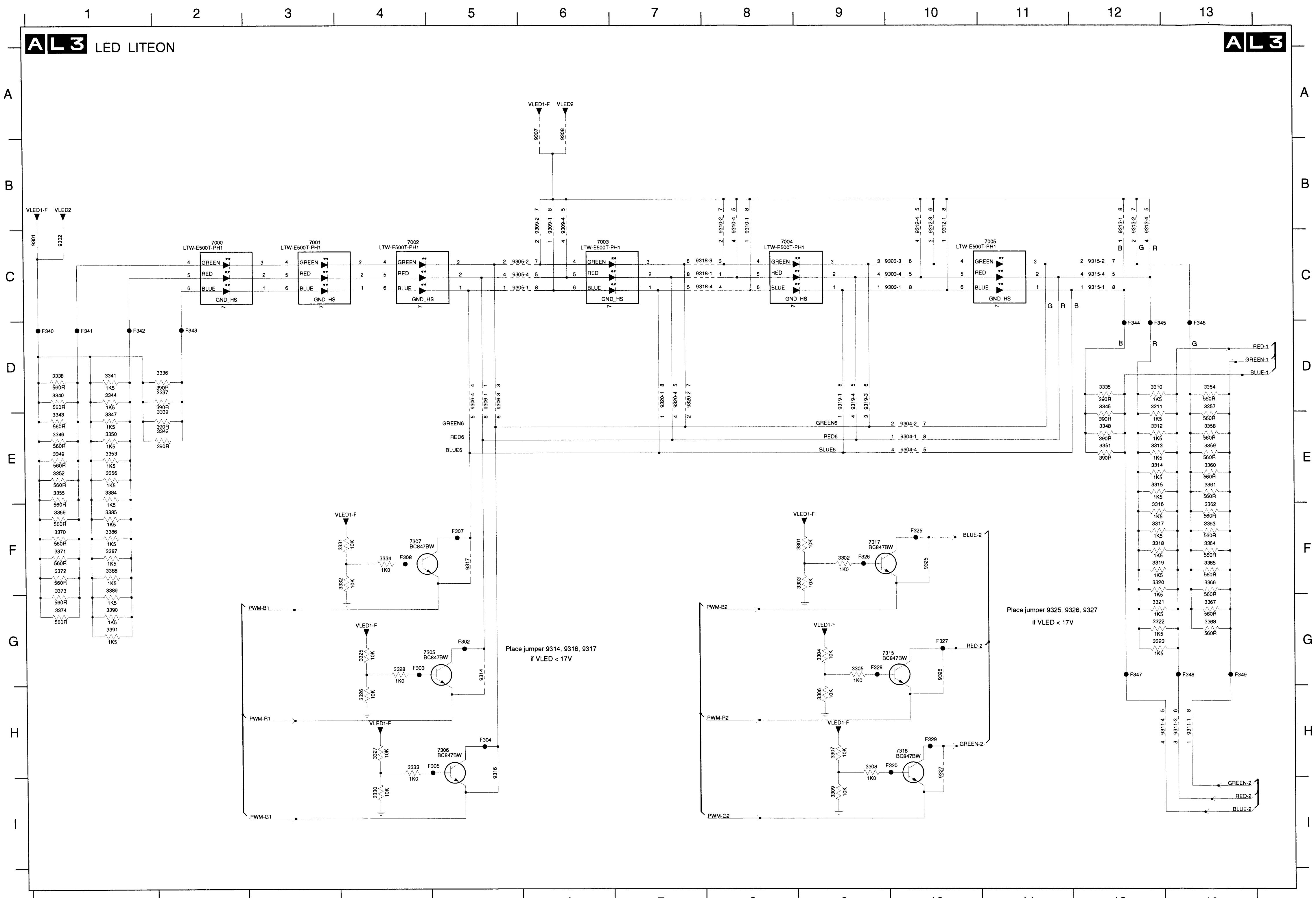
2201	B8
2202	C8
2203	D8
2209	B2
2210	G6
2211	I6
2214	A6
2215	F7
2216	F7
2217	B12
2218	C12
2219	D12
2220	E9
3121	D9
3203	B5
3204	B7
3205	C5
3207	B9
3209	C9
3210	B3
3211	C9
3212	D11
3213	B3
3214	H6
3215	H6
3216	H6
3217	H6
3218	H6
3219	B11
3220	C11
3221	H11
3222	I8
3223	C11
3224	H11
6216	I8
7201-1	A10
7201-2	C10
7201-3	D10
7201-4	B10
7209	B2
7210	C2
7212	B3
7214	B6
7215	G7
9208	A10
9209	B9
9210	B10
9211	C9
9212	C10
9213	D9
9214	D10
F202	B3
F203	C5
F204	H6
F205	B10
F206	C10
F207	C10
F208	D10
F209	H11
F210	G9
F211	G9
F212	G9
F213	H9
F214	H9
F215	H9

3104 313 6314.3

CHN
SETNAME
CLASS_NO
2008-08-08 2
3
DRIVER 6LED LITEON
2K9
8204 000 8857
1 2008-06-10
2 2008-08-08
3 ??
NAME Peter Van Hove
SUPERS. 3
130 - 2
A2
CHECK
DATE 2008-06-02

18310_651_090508.eps
090508

8 LED Low-Pow: LED Liteon


AL3
LED LITEON
VLED1-F
VLED2
7000 LTW-E500T-PH1
7001 LTW-E500T-PH1
7002 LTW-E500T-PH1
7003 LTW-E500T-PH1
7004 LTW-E500T-PH1
7005 LTW-E500T-PH1
GREEN
RED
BLUE
GND_HS
GREEN6
RED6
BLUE6
7307 BC847BW
7305 BC847BW
7306 BC847BW
7317 BC847BW
7315 BC847BW
7316 BC847BW
PWM-B1
PWM-R1
PWM-G1
PWM-B2
PWM-R2
PWM-G2
BLUE-2
RED-2
GREEN-2
RED-1
GREEN-1
BLUE-1

Place jumper 9314, 9316, 9317 if VLED < 17V

Place jumper 9325, 9326, 9327 if VLED < 17V

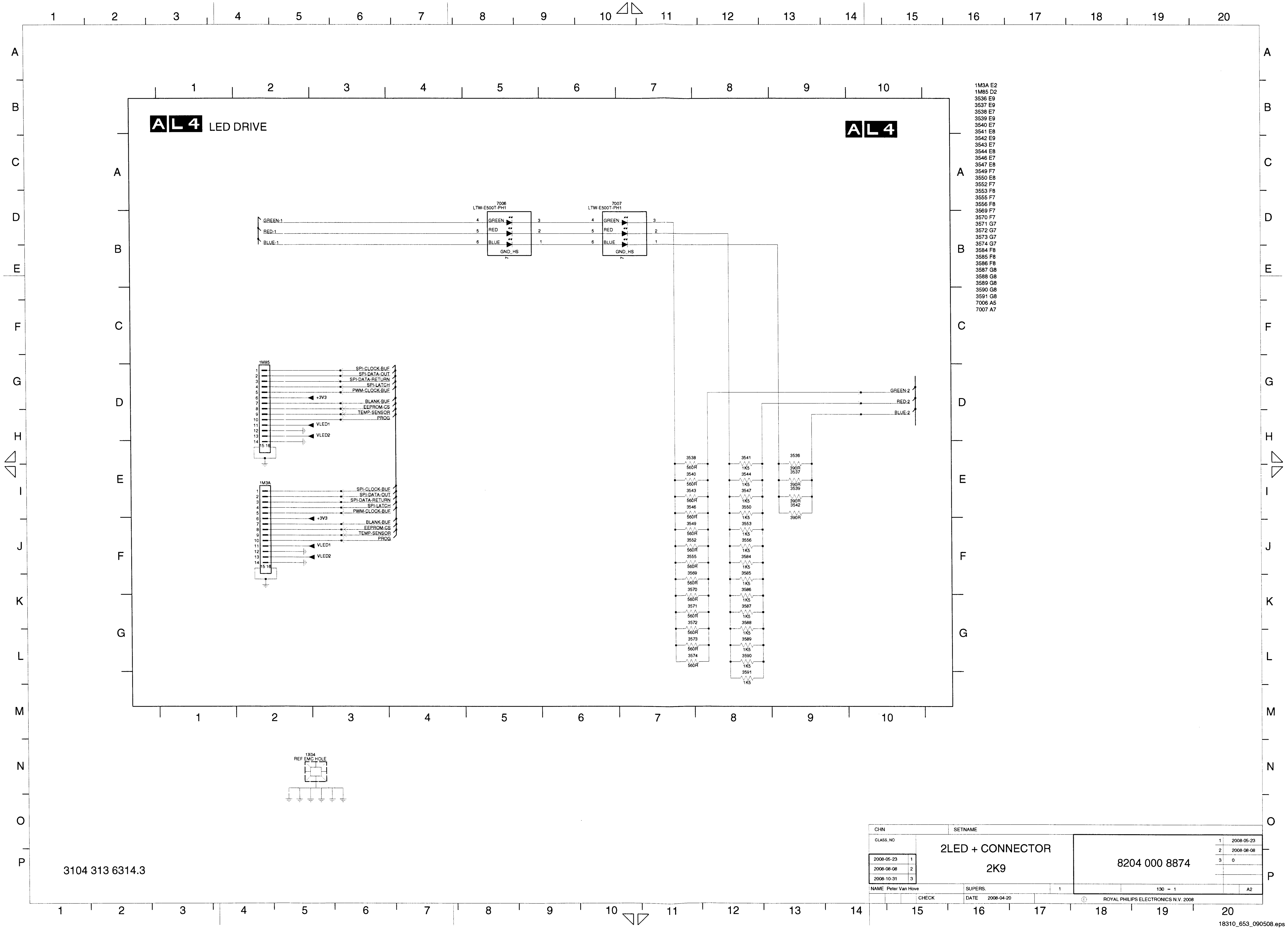
3301	F9
3302	F9
3303	F9
3304	G9
3305	G9
3306	H9
3307	H9
3308	H9
3309	I9
3310	D12
3311	D12
3312	E12
3313	E12
3314	E12
3315	E12
3316	E12
3317	F12
3318	F12
3319	F12
3320	F12
3321	G12
3322	G12
3323	G12
3325	G4
3326	H4
3327	H4
3328	G4
3330	I4
3331	F4
3332	F4
3333	H4
3334	F4
3335	D12
3336	D2
3337	D2
3338	D1
3339	D2
3340	D1
3341	D1
3342	E2
3343	D1
3344	D1
3345	D12
3346	E1
3347	D1
3348	E12
3349	E1
3350	E1
3351	E12
3352	E1
3353	E1
3354	D13
3355	E1
3356	E1
3357	D13
3358	E13
3359	E13
3360	E13
3361	E13
3362	E13
3363	F13
3364	F13
3365	F13
3366	F13
3367	G13
3368	G13
3369	F1
3370	F1
3371	F1
3372	F1
3373	F1
3374	G1
3384	E1
3385	F1
3386	F1
3387	F1
3388	F1
3389	F1
3390	G1
3391	G1
7000	C2
7001	C3
7002	C4
7003	C6
7004	C8
7005	C11
7305	G4
7306	H5
7307	F4
7315	G9
7316	H10
7317	F9
9301	C1
9302	C1
9303-1	C10
9303-3	C10
9303-4	C10
9304-1	E10
9304-2	E10
9304-4	E10
9305-1	C6
9305-2	C6
9305-4	C6
9306-1	D5
9306-3	D5
9306-4	D5
9307	A6
9308	A6
9309-1	B6
9309-2	B6
9309-4	B6
9310-1	B8
9310-2	B8
9310-4	B8
9311-1	H13
9311-3	H13
9311-4	H12
9312-1	B10
9312-3	B10
9312-4	B10
9313-1	B12
9313-2	B12
9313-4	B12
9314	G5
9315-1	C12
9315-2	C12
9315-4	C12
9316	H5
9317	F5
9318-1	C8
9318-3	C8
9318-4	C8
9319-1	D9
9319-3	D9
9319-4	D9
9320-1	D7
9320-2	D7
9320-4	D7
9325	F10
9326	G10
9327	H10
F302	G5
F303	G4
F304	H5
F305	H5
F307	F5
F308	F4
F325	F10
F326	F9
F327	G10
F328	G9
F329	H10
F330	H10
F340	D1
F341	D1
F342	D1
F343	D2
F344	D12
F345	D12
F346	D13
F347	G12
F348	G13
F349	G13

3104 313 6314.3

CHN
SETNAME
CLASS_NO
2008-08-08 2
3
DRIVER 6LED LITEON
2K9
8204 000 8857
1 2008-06-10
2 2008-08-08
3 ??
NAME Peter Van Hove
SUPERS.
3
130 – 3
A2
CHECK
DATE 2008-06-02

18310_652_090508.eps
090508

8 LED Low-Pow: LED Drive Liteon


AL4 LED DRIVE
AL4
7006
LTW-E500T-PH1
7007
LTW-E500T-PH1
GREEN-1
RED-1
BLUE-1
GREEN
RED
BLUE
GND_HS
GREEN-2
RED-2
BLUE-2
1M85
1M3A
SPI-CLOCK-BUF
SPI-DATA-OUT
SPI-DATA-RETURN
SPI-LATCH
PWM-CLOCK-BUF
+3V3
BLANK-BUF
EEPROM-CS
TEMP-SENSOR
PROG
VLED1
VLED2
3538 560R
3540 560R
3543 560R
3546 560R
3549 560R
3552 560R
3555 560R
3569 560R
3570 560R
3571 560R
3572 560R
3573 560R
3574 560R
3541 1K5
3544 1K5
3547 1K5
3550 1K5
3553 1K5
3556 1K5
3584 1K5
3585 1K5
3586 1K5
3587 1K5
3588 1K5
3589 1K5
3590 1K5
3591 1K5
3536 390R
3537 390R
3539 390R
3542 390R
1X04
REF EMC HOLE
1M3A E2
1M85 D2
3536 E9
3537 E9
3538 E7
3539 E9
3540 E7
3541 E8
3542 E9
3543 E7
3544 E8
3546 E7
3547 E8
3549 F7
3550 E8
3552 F7
3553 F8
3555 F7
3556 F8
3569 F7
3570 F7
3571 G7
3572 G7
3573 G7
3574 G7
3584 F8
3585 F8
3586 F8
3587 G8
3588 G8
3589 G8
3590 G8
3591 G8
7006 A5
7007 A7
3104 313 6314.3
CHN
SETNAME
CLASS_NO
2LED + CONNECTOR
2K9
8204 000 8874
2008-05-23 1
2008-08-08 2
2008-10-31 3
1 2008-05-23
2 2008-08-08
3 0
NAME Peter Van Hove
SUPERS.
1
130 - 1
A2
CHECK
DATE 2008-04-20
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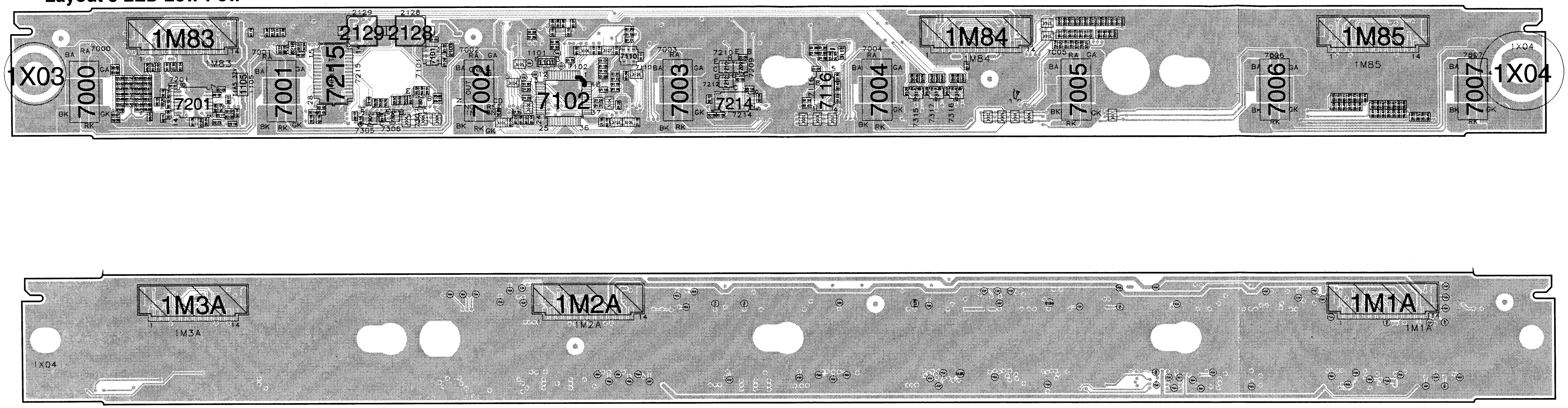
18310_653_090508.eps
090508

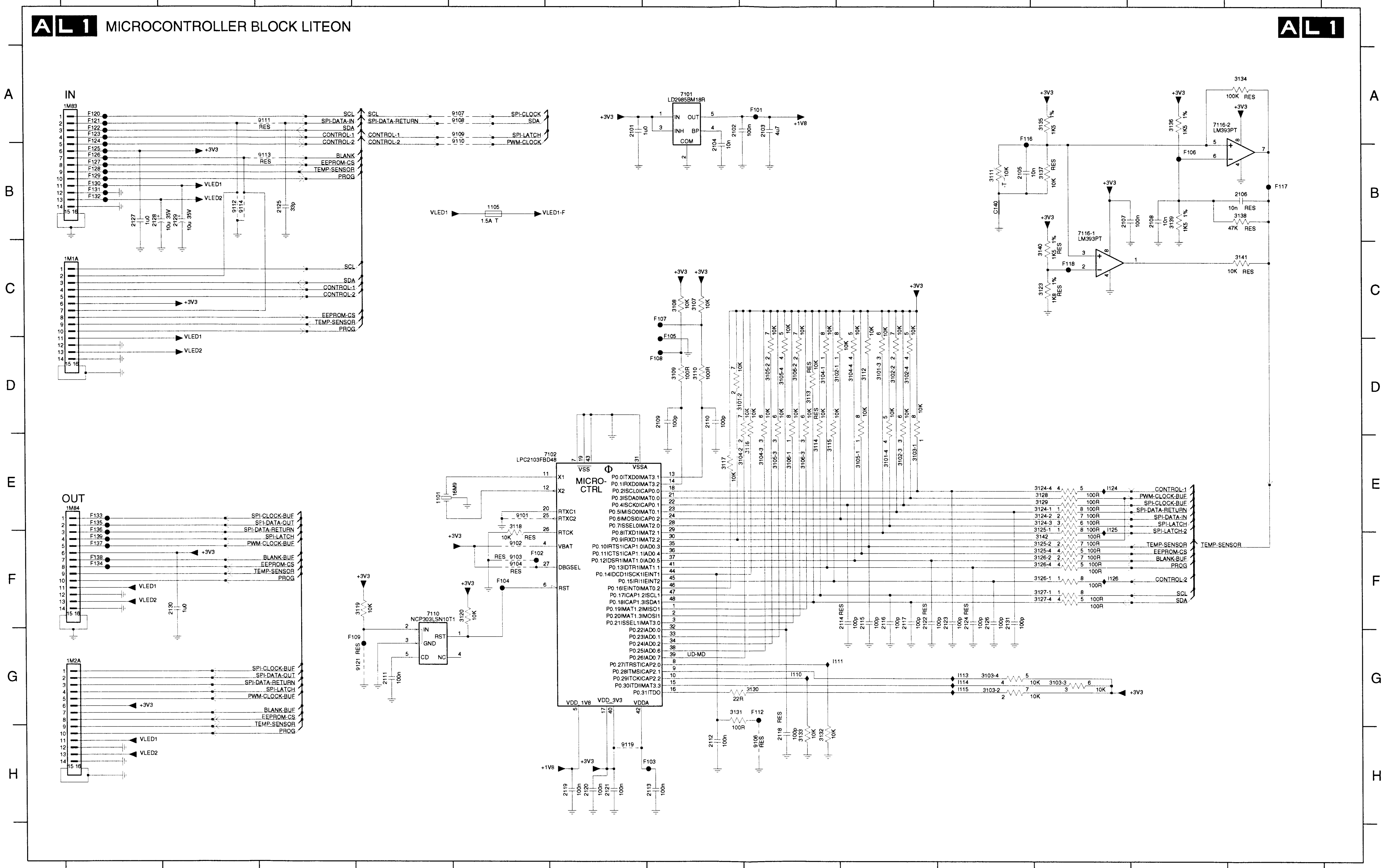
Layout 8 LED Low-Pow

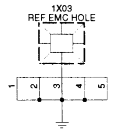

1M83
2129
2128
1X03
7000
7201
7001
7215
7002
7102
7003
7214
7116
7004
1M84
7005
1M85
7006
7007
1X04
1M3A
1M2A
1M1A

31043136314.3

18490_550_090326.eps
090326

10 LED Low-Pow: Microcontroller Block Liteon


AL 1
MICROCONTROLLER BLOCK LITEON
AL 1
IN
1M83
OUT
1M84
1M1A
1M2A
SCL
SDA
SPI-DATA-IN
SPI-DATA-RETURN
CONTROL-1
CONTROL-2
SPI-CLOCK
SPI-LATCH
PWM-CLOCK
BLANK
EEPROM-CS
TEMP-SENSOR
PROG
VLED1
VLED2
VLED1-F
SPI-CLOCK-BUF
SPI-DATA-OUT
PWM-CLOCK-BUF
BLANK-BUF
+3V3
+1V8
7101
LD2985BM18R
7102
LPC2103FBD48
MICRO-CTRL
7110
NCP303LSN10T1
7116-1
LM393PT
7116-2
LM393PT
1105
1.5A T
X1
X2
RTXC1
RTXC2
RTCK
VBAT
DBGSEL
RST
VSS
VSSA
VDD_1V8
VDD_3V3
VDDA
UD-MD

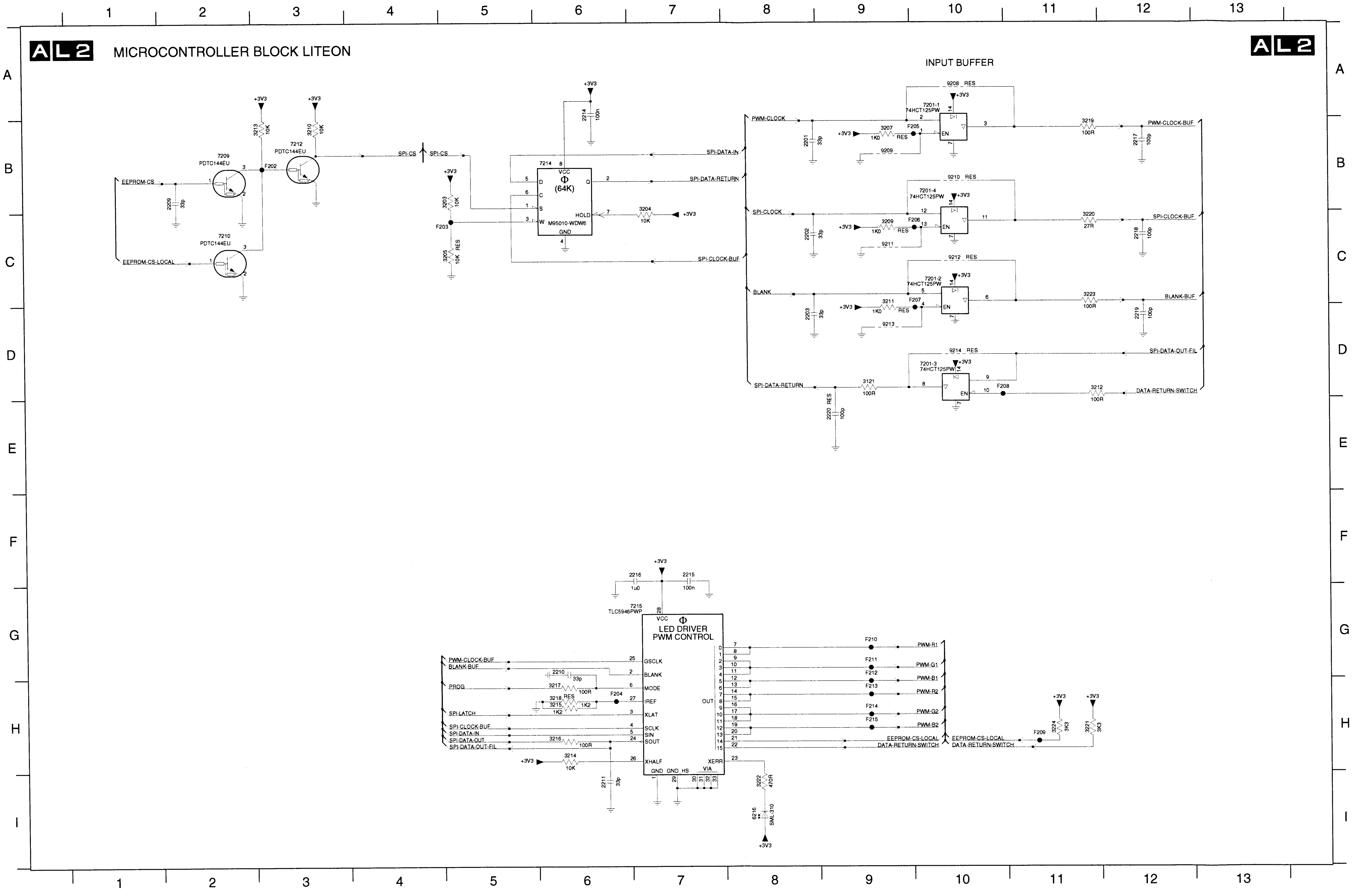

1X03
REF EMC HOLE
1
2
3
4
5

1101	E4
1105	B5
1M1A	C1
1M2A	G1
1M83	A1
1M84	E1
2101	A6
2102	A7
2103	A8
2104	B7
2105	B10
2106	B13
2107	B11
2108	B12
2109	D7
2110	D7
2111	G4
2112	H7
2113	H7
2114	F9
2115	F9
2116	F9
2117	F9
2118	H8
2119	H6
2120	H6
2121	H6
2122	F9
2123	F10
2124	F10
2125	B3
2126	F10
2127	B1
2128	B1
2129	B2
2130	F2
2131	F10
3101-2	D7
3101-3	D9
3101-4	E9
3102-1	D9
3102-2	D9
3102-3	E9
3102-4	D9
3103-1	E9
3103-2	G10
3103-3	G11
3103-4	G10
3104-1	D8
3104-2	E8
3104-3	E8
3104-4	D9
3105-1	E9
3105-2	D8
3105-3	E8
3105-4	D8
3106-1	E8
3106-2	D8
3106-3	E8
3107	C7
3108	C7
3109	D7
3110	D7
3111	B10
3112	D9
3113	D8
3114	E8
3115	E8
3116	E8
3117	E7
3118	E5
3119	F4
3120	F5
3123	C11
3124-1	E11
3124-2	E11
3124-3	E11
3124-4	E11
3125-1	F11
3125-2	F11
3125-4	F11
3126-1	F11
3126-2	F11
3126-4	F11
3127-1	F11
3127-4	F11
3128	E11
3129	E11
3130	G8
3131	G7
3132	H8
3133	H8
3134	A13
3135	A11
3136	A12
3137	B11
3138	B13
3139	B12
3140	C11
3141	C13
3142	F11
7101	A7
7102	E6
7110	F4
7116-1	B11
7116-2	A12
9101	E5
9102	F5
9103	F5
9104	F5
9106	H8
9107	A5
9108	A5
9109	A5
9110	B5
9111	A3
9112	B2
9113	B3
9114	B2
9119	H6
9121	G4
C140	B10
F101	A8
F102	F5
F103	H7
F104	F5
F105	D7
F106	B12
F107	C7
F108	D7
F109	G3
F112	G8
F116	A10
F117	B13
F118	C11
F120	A1
F121	A1
F122	A1
F123	A1
F124	B1
F125	B1
F126	B1
F127	B1
F128	B1
F129	B1
F130	B1
F131	B1
F132	B1
F133	E1
F134	F1
F135	E1
F136	F1
F137	F1
F138	F1
F139	F1
I110	G8
I111	G8
I113	G10
I114	G10
I115	G10
I124	E11
I125	E11
I126	F11

CHN	SETNAME				
CLASS_NO	DRIVER 6LED LITEON 2K9	8204 000 8857		1	2008-06-10
				2	2008-08-08
2008-08-08 2				3	??
3					
NAME Peter Van Hove	SUPERS.	3	130 - 1		A2
CHECK	DATE 2008-06-02	© ROYAL PHILIPS ELECTRONICS N.V. 2008			

18310_630_090306.eps
090306

10 LED Low-Pow: Microcontroller Block Liteon


AL2
MICROCONTROLLER BLOCK LITEON
INPUT BUFFER
EEPROM-CS
EEPROM-CS-LOCAL
7209 PDTC144EU
7210 PDTC144EU
7212 PDTC144EU
2209 33p
3213 10K
3210 10K
F202
+3V3
SPI-CS
3203 10K
F203
3205 10K RES
7214
VCC
(64K)
D
C
S
W
Q
HOLD
M95010-WDW6
GND
2214 100n
3204 10K
SPI-DATA-IN
SPI-DATA-RETURN
SPI-CLOCK-BUF
PWM-CLOCK
SPI-CLOCK
BLANK
9208 RES
7201-1 74HCT125PW
3207 1K0 RES
F205
9209
2201 33p
3219 100R
2217 100p
PWM-CLOCK-BUF
9210 RES
7201-4 74HCT125PW
3209 1K0 RES
F206
9211
2202 33p
3220 27R
2218 100p
9212 RES
7201-2 74HCT125PW
3211 1K0 RES
F207
9213
2203 33p
3223 100R
2219 100p
BLANK-BUF
9214 RES
7201-3 74HCT125PW
SPI-DATA-OUT-FIL
3121 100R
2220 RES 100p
F208
3212 100R
DATA-RETURN-SWITCH
EN
2216 1u0
2215 100n
7215 TLC5946PWP
LED DRIVER
PWM CONTROL
GSCLK
BLANK
MODE
IREF
XLAT
SCLK
SIN
SOUT
XHALF
GND GND_HS VIA
XERR
OUT
PROG
SPI-LATCH
SPI-DATA-OUT
2210 33p
3217 100R
3218 RES
3215 1K2
1K2
F204
3216 100R
3214 10K
2211 33p
3222 470R
6216 SML-310
F210
F211
F212
F213
F214
F215
PWM-R1
PWM-G1
PWM-B1
PWM-R2
PWM-G2
PWM-B2
F209
3224 3K3
3221 3K3

2201	B8
2202	C8
2203	D8
2209	B2
2210	G6
2211	I6
2214	A6
2215	F7
2216	F7
2217	B12
2218	C12
2219	D12
2220	E9
3121	D9
3203	B5
3204	B7
3205	C5
3207	B9
3209	C9
3210	B3
3211	C9
3212	D11
3213	B3
3214	H6
3215	H6
3216	H6
3217	H6
3218	H6
3219	B11
3220	C11
3221	H11
3222	I8
3223	C11
3224	H11
6216	I8
7201-1	A10
7201-2	C10
7201-3	D10
7201-4	B10
7209	B2
7210	C2
7212	B3
7214	B6
7215	G7
9208	A10
9209	B9
9210	B10
9211	C9
9212	C10
9213	D9
9214	D10
F202	B3
F203	C5
F204	H6
F205	B10
F206	C10
F207	C10
F208	D10
F209	H11
F210	G9
F211	G9
F212	G9
F213	H9
F214	H9
F215	H9

CHN
SETNAME
CLASS_NO
DRIVER 6LED LITEON
2K9
8204 000 8857

1	2008-06-10
2	2008-08-08
3	??

2008-08-08	2
	3

NAME Peter Van Hove
SUPERS. 3
130 - 2
A2
CHECK
DATE 2008-06-02

18310_631_090306.eps
090306

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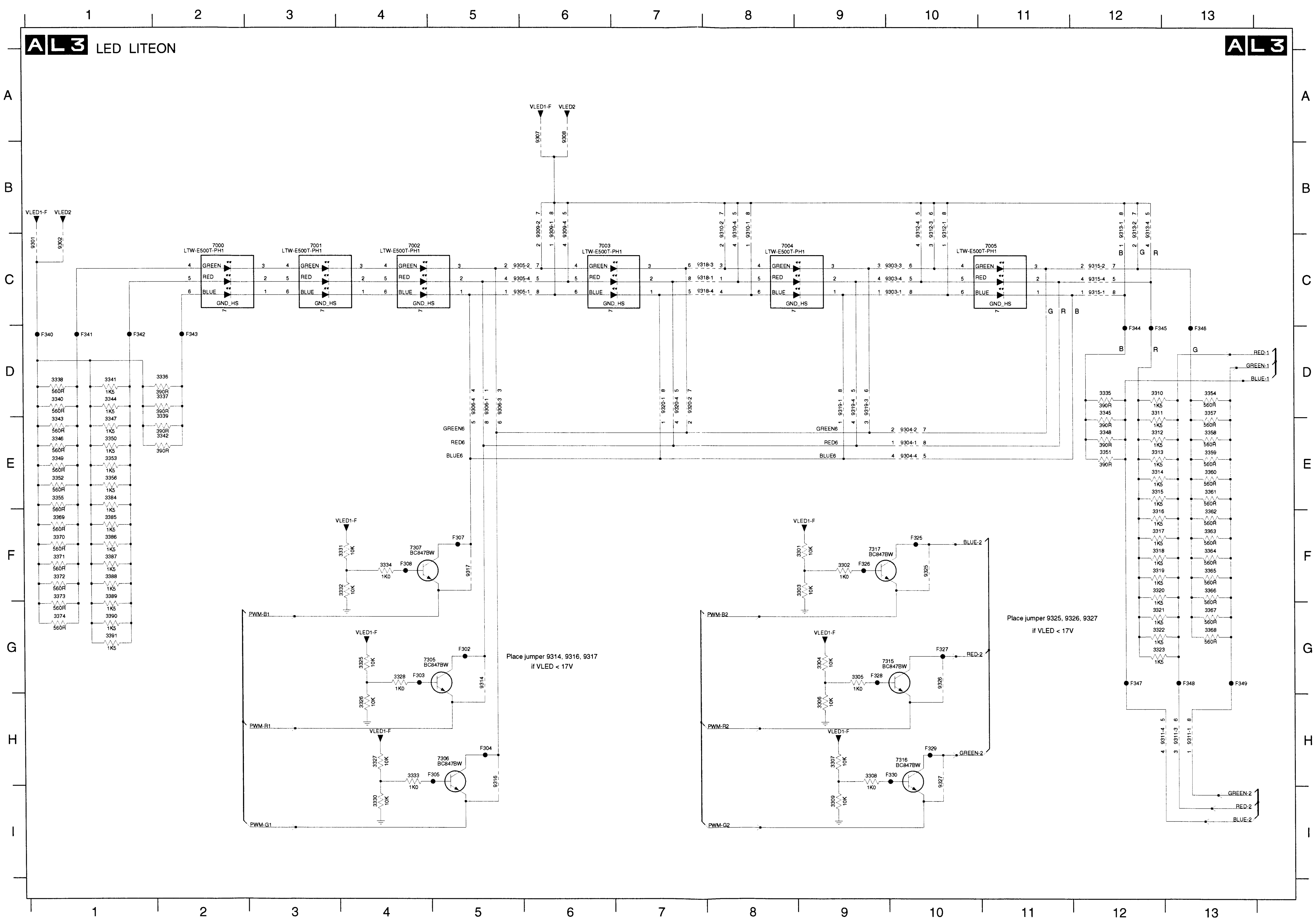
10 LED Low-Pow: LED Liteon


AL3
LED LITEON
VLED1-F
VLED2
9307
9308
9301
9302
7000 LTW-E500T-PH1
7001 LTW-E500T-PH1
7002 LTW-E500T-PH1
7003 LTW-E500T-PH1
7004 LTW-E500T-PH1
7005 LTW-E500T-PH1
GREEN
RED
BLUE
GND_HS
F340
F341
F342
F343
F344
F345
F346
F347
F348
F349
GREEN6
RED6
BLUE6
RED-1
GREEN-1
BLUE-1
BLUE-2
RED-2
GREEN-2
PWM-B1
PWM-R1
PWM-G1
PWM-B2
PWM-R2
PWM-G2
7307 BC847BW
7305 BC847BW
7306 BC847BW
7317 BC847BW
7315 BC847BW
7316 BC847BW
560R
1K5
390R
10K
1K0

Place jumper 9314, 9316, 9317
if VLED < 17V

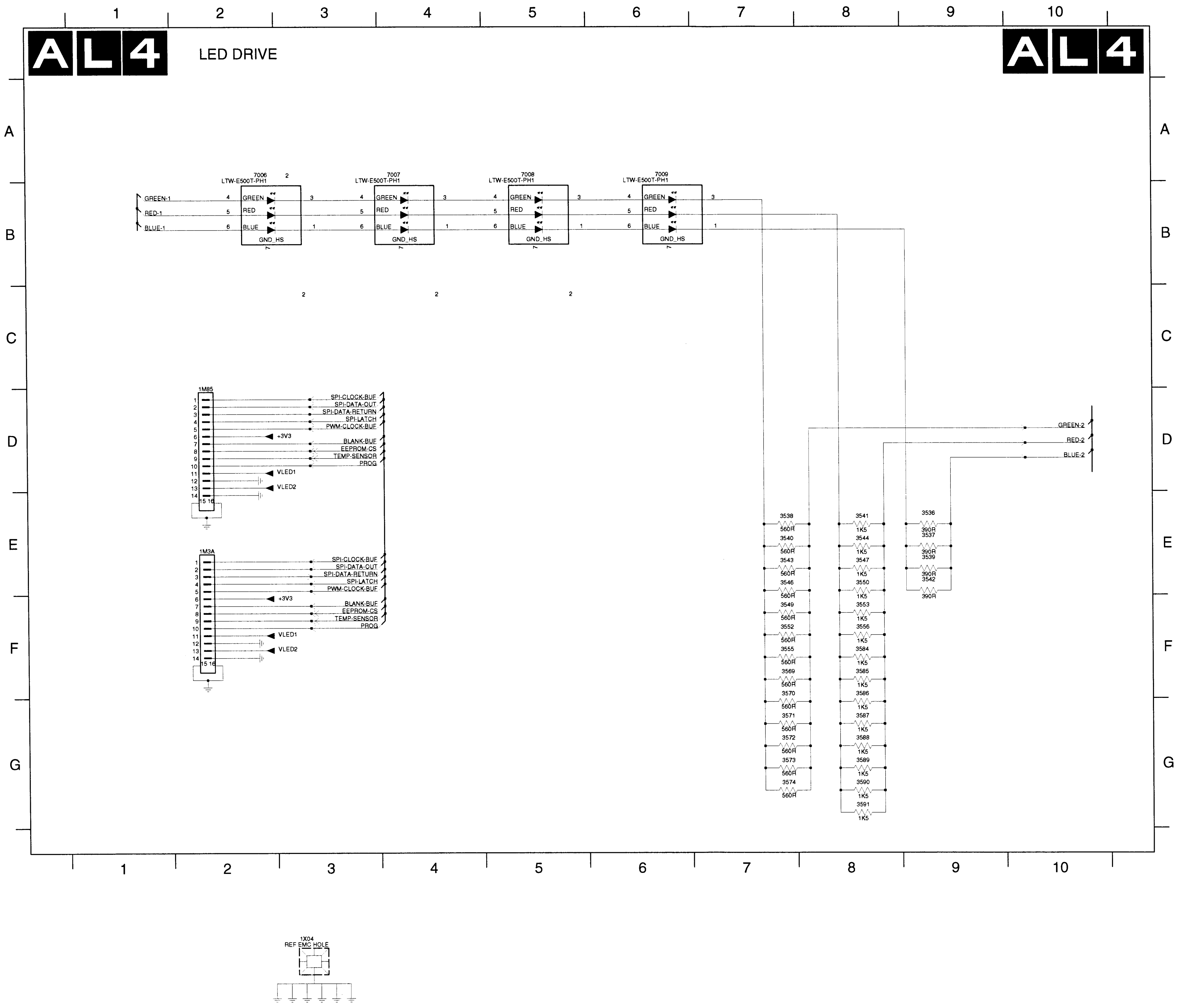
Place jumper 9325, 9326, 9327
if VLED < 17V

3301	F9
3302	F9
3303	F9
3304	G9
3305	G9
3306	H9
3307	H9
3308	H9
3309	I9
3310	D12
3311	D12
3312	E12
3313	E12
3314	E12
3315	E12
3316	E12
3317	F12
3318	F12
3319	F12
3320	F12
3321	G12
3322	G12
3323	G12
3325	G4
3326	H4
3327	H4
3328	G4
3330	I4
3331	F4
3332	F4
3333	H4
3334	F4
3335	D12
3336	D2
3337	D2
3338	D1
3339	D2
3340	D1
3341	D1
3342	E2
3343	D1
3344	D1
3345	D12
3346	E1
3347	D1
3348	E12
3349	E1
3350	E1
3351	E12
3352	E1
3353	E1
3354	D13
3355	E1
3356	E1
3357	D13
3358	E13
3359	E13
3360	E13
3361	E13
3362	E13
3363	F13
3364	F13
3365	F13
3366	F13
3367	G13
3368	G13
3369	F1
3370	F1
3371	F1
3372	F1
3373	F1
3374	G1
3384	E1
3385	F1
3386	F1
3387	F1
3388	F1
3389	F1
3390	G1
3391	G1
7000	C2
7001	C3
7002	C4
7003	C6
7004	C8
7005	C11
7305	G4
7306	H5
7307	F4
7315	G9
7316	H10
7317	F9
9301	C1
9302	C1
9303-1	C10
9303-3	C10
9303-4	C10
9304-1	E10
9304-2	E10
9304-4	E10
9305-1	C6
9305-2	C6
9305-4	C6
9306-1	D5
9306-3	D5
9306-4	D5
9307	A6
9308	A6
9309-1	B6
9309-2	B6
9309-4	B6
9310-1	B8
9310-2	B8
9310-4	B8
9311-1	H13
9311-3	H13
9311-4	H12
9312-1	B10
9312-3	B10
9312-4	B10
9313-1	B12
9313-2	B12
9313-4	B12
9314	G5
9315-1	C12
9315-2	C12
9315-4	C12
9316	H5
9317	F5
9318-1	C8
9318-3	C8
9318-4	C8
9319-1	D9
9319-3	D9
9319-4	D9
9320-1	D7
9320-2	D7
9320-4	D7
9325	F10
9326	G10
9327	H10
F302	G5
F303	G4
F304	H5
F305	H5
F307	F5
F308	F4
F325	F10
F326	F9
F327	G10
F328	G9
F329	H10
F330	H10
F340	D1
F341	D1
F342	D1
F343	D2
F344	D12
F345	D12
F346	D13
F347	G12
F348	G13
F349	G13

CHN
SETNAME
CLASS_NO
DRIVER 6LED LITEON
2K9
2008-08-08 2
3
8204 000 8857
1 2008-06-10
2 2008-08-08
3 ??
NAME Peter Van Hove
SUPERS. 3
130 – 3
A2
CHECK
DATE 2008-06-02

18310_632_090306.eps
090306

10 LED Low-Pow: LED Drive Liteon


AL4
LED DRIVE
AL4
7006
LTW-E500T-PH1
7007
LTW-E500T-PH1
7008
LTW-E500T-PH1
7009
LTW-E500T-PH1
GREEN-1
RED-1
BLUE-1
GREEN
RED
BLUE
GND_HS
1M85
1M3A
SPI-CLOCK-BUF
SPI-DATA-OUT
SPI-DATA-RETURN
SPI-LATCH
PWM-CLOCK-BUF
+3V3
BLANK-BUF
EEPROM-CS
TEMP-SENSOR
PROG
VLED1
VLED2
GREEN-2
RED-2
BLUE-2
3538 560R
3540 560R
3543 560R
3546 560R
3549 560R
3552 560R
3555 560R
3569 560R
3570 560R
3571 560R
3572 560R
3573 560R
3574 560R
3541 1K5
3544 1K5
3547 1K5
3550 1K5
3553 1K5
3556 1K5
3584 1K5
3585 1K5
3586 1K5
3587 1K5
3588 1K5
3589 1K5
3590 1K5
3591 1K5
3536 390R
3537 390R
3539 390R
3542 390R
1X04
REF EMC HOLE

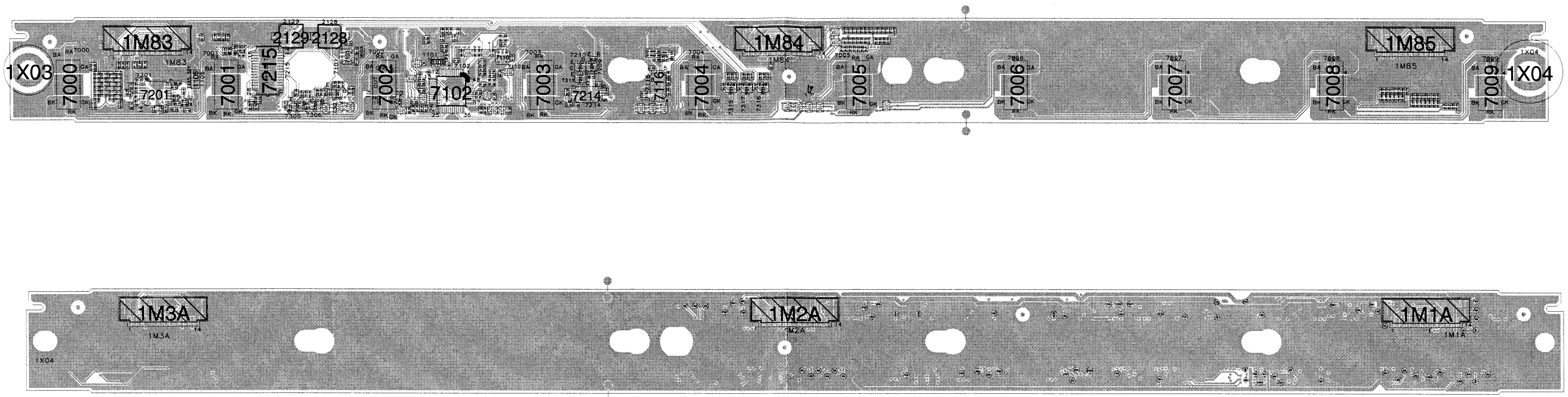
1M3A	E2
1M85	D2
3536	E9
3537	E9
3538	E7
3539	E9
3540	E7
3541	E8
3542	E9
3543	E7
3544	E8
3546	E7
3547	E8
3549	F7
3550	E8
3552	F7
3553	F8
3555	F7
3556	F8
3569	F7
3570	F7
3571	G7
3572	G7
3573	G7
3574	G7
3584	F8
3585	F8
3586	F8
3587	G8
3588	G8
3589	G8
3590	G8
3591	G8
7006	A2
7007	A4
7008	A5
7009	A6

PHILIPS

CHN	SETNAME			
CLASS_NO	4 LED + CONNECTOR LITEON 2K9	8204 000 8897	1	2008-08-14
2008-08-14 2			2	2008-10-24
2008-10-31 3			3	2008-10-31
NAME Peter Van Hove	SUPERS. 1	130 – 1		A2
CHECK	DATE 2008-07-29			

18310_633_090306.eps
090306

Layout 10 LED Low-Pow

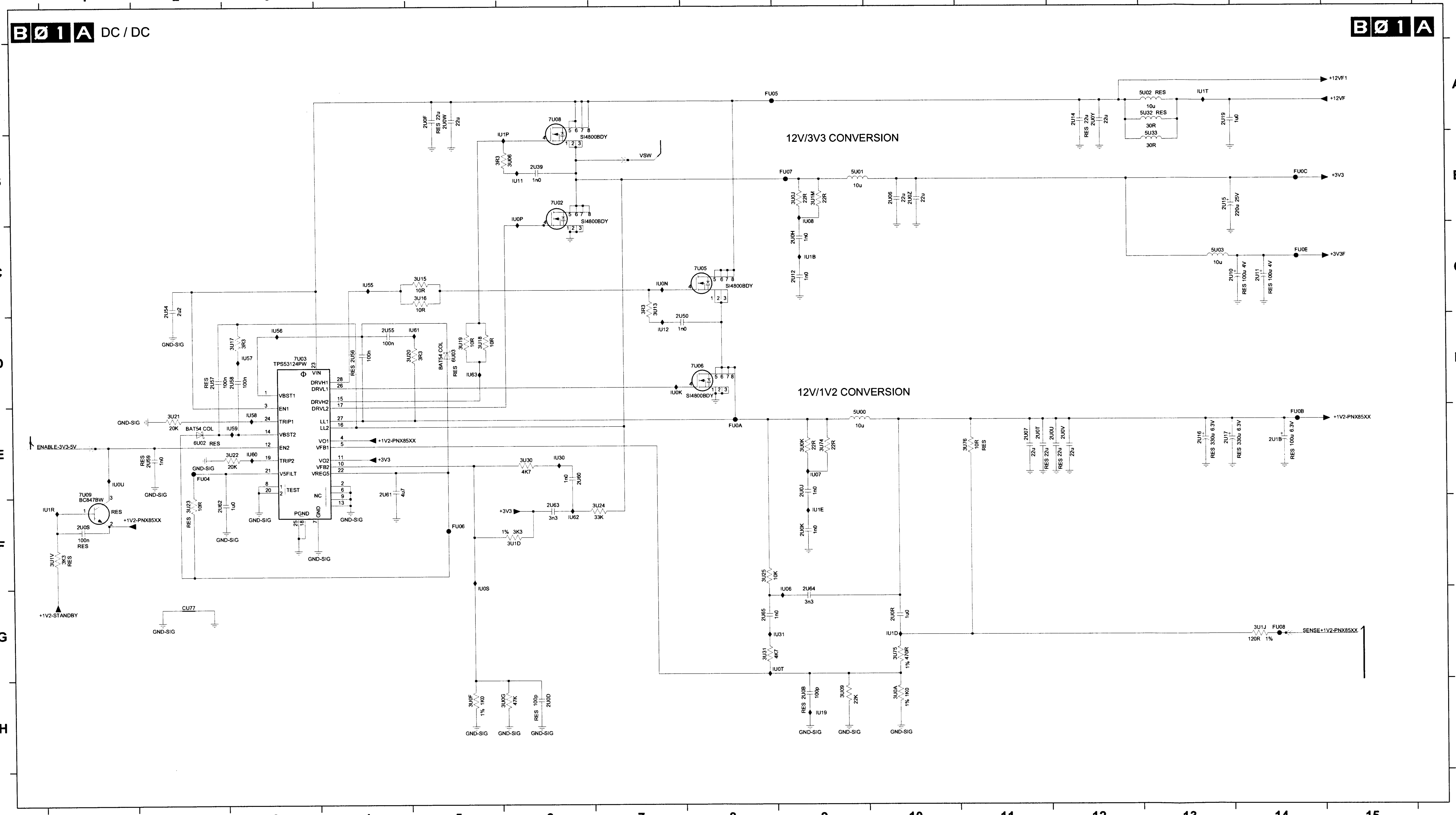

1M83
2129
2128
1X03
7000
7201
7001
7215
7002
7102
7003
7214
7116
7004
1M84
7005
7006
7007
7008
1M85
7009
1X04
1M3A
1M2A
1M1A

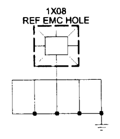
3104 313 6315.2

18310_553_090309
090309

SSB: DC/DC

2U06	B10
2U07	E11
2U0B	H9
2U0D	H6
2U0F	A5
2U0H	C9
2U0J	E9
2U0K	F9
2U0R	G10
2U0S	F1
2U0T	E11
2U0U	E12
2U0V	E12
2U0W	A5
2U0Y	A12
2U0Z	B10
2U10	C14
2U11	C14
2U12	C9
2U14	A12
2U15	B13
2U16	E13
2U17	E13
2U19	A13
2U1B	E14
2U39	B6
2U50	D7
2U54	C2
2U55	D4
2U56	D4
2U57	D2
2U58	D3
2U59	E2
2U60	E6
2U61	E4
2U62	F2
2U63	F6
2U64	G9
2U65	G8
3U06	B6
3U09	H9
3U0A	H10
3U0F	H5
3U0G	H6
3U0J	B9
3U0K	E9
3U13	C7
3U15	C5
3U16	C5
3U17	D3
3U18	D5
3U19	D5
3U1D	F6
3U1J	G14
3U1M	B9
3U1V	F1
3U20	D5
3U21	E2
3U22	E3
3U23	F2
3U24	F7
3U25	F8
3U30	E6
3U31	G8
3U74	E9
3U75	G10
3U76	E11
5U00	E9
5U01	B9
5U02	A13
5U03	C13
5U32	A13
5U33	B13
6U02	E2
6U03	D5
7U02	B6
7U03	D3
7U05	C8
7U06	D8
7U08	A6
7U09	E1
CU77	G2
FU04	E2
FU05	A8
FU06	F5
FU07	B9
FU08	G14
FU0A	E8
FU0B	E14
FU0C	B14
FU0E	C14
IU06	G9
IU07	E9
IU08	B9
IU0K	D7
IU0N	C7
IU0P	B6
IU0S	G5
IU0T	G9
IU0U	E1
IU11	B6
IU12	D7
IU19	H9
IU1B	C9
IU1D	G10
IU1E	F9
IU1P	B6
IU1R	F1
IU1T	A13
IU30	E6
IU31	G9
IU55	C4
IU56	D3
IU57	D3
IU58	E3
IU59	E3
IU60	E3
IU61	D5
IU62	F6
IU63	D5


B01A DC / DC
B01A
12V/3V3 CONVERSION
12V/1V2 CONVERSION
+12VF1
+12VF
+3V3
+3V3F
+1V2-PNX85XX
SENSE+1V2-PNX85XX
ENABLE-3V3-5V
+1V2-STANDBY
VSW
7U03
TPS53124PW
VIN
DRVH1
DRVL1
DRVH2
DRVL2
LL1
LL2
VBST1
EN1
TRIP1
VBST2
EN2
TRIP2
V5FILT
TEST
VO1
VFB1
VO2
VFB2
VREG5
NC
PGND
GND
7U08
7U02
7U05
7U06
SI4800BDY
7U09
BC847BW
BAT54 COL
6U02
6U03
5U00
5U01
5U02
5U03
5U32
5U33
CU77
GND-SIG
FU04
FU05
FU06
FU07
FU08
FU0A
FU0B
FU0C
FU0E


1X08
REF EMC HOLE

CHN	SETNAME		
CLASS_NO	DC/DC TV543 R2 LDIPNX	8204 000 8932	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 3	130 - 1	A2
CHECK	DATE 2007-11-20	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

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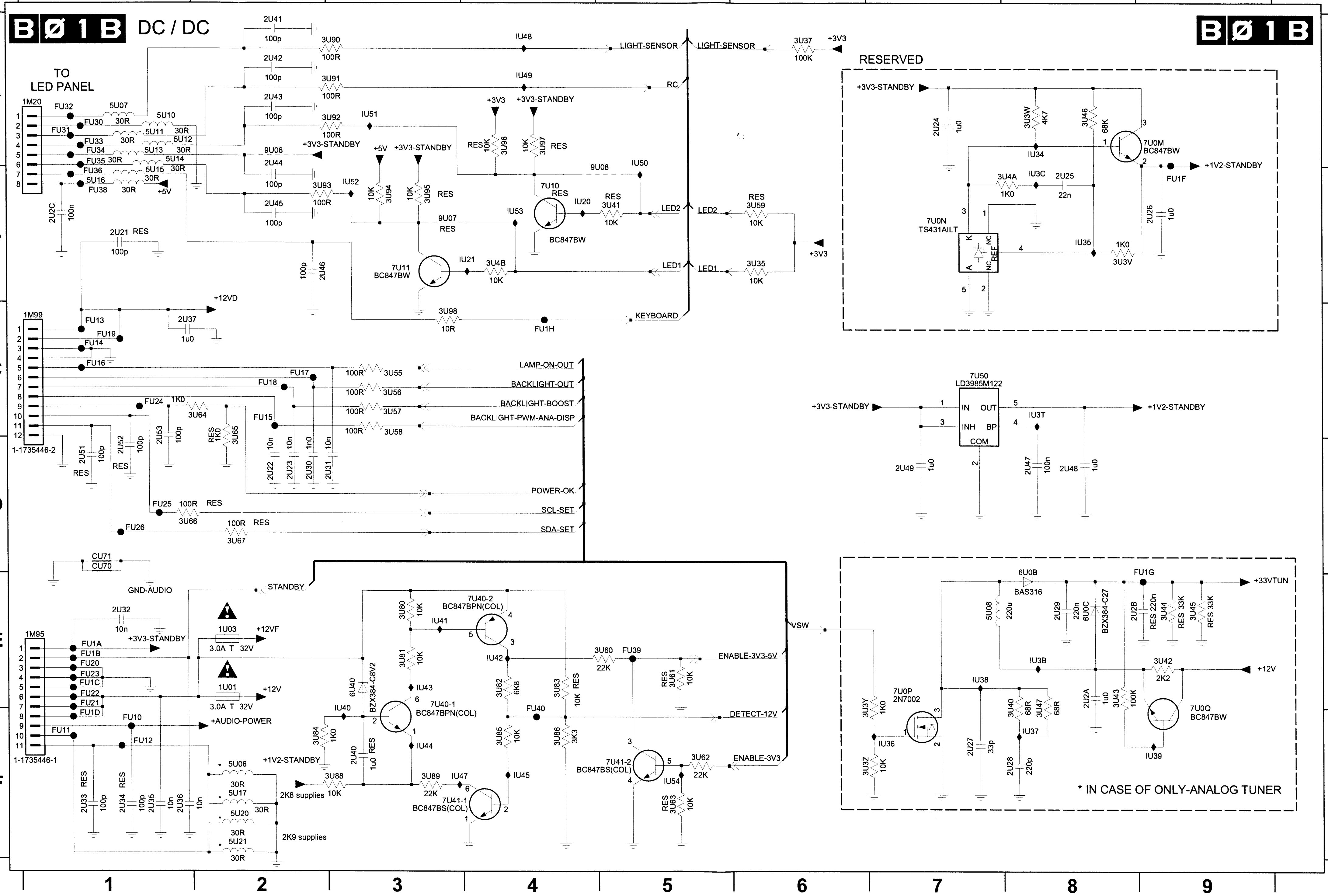
090302

SSB: DC/DC


B01B DC / DC
TO LED PANEL
1M20
1M99
1M95
1-1735446-2
1-1735446-1
LIGHT-SENSOR
RC
LED2
LED1
KEYBOARD
+3V3
+3V3-STANDBY
+5V
+12VD
LAMP-ON-OUT
BACKLIGHT-OUT
BACKLIGHT-BOOST
BACKLIGHT-PWM-ANA-DISP
POWER-OK
SCL-SET
SDA-SET
GND-AUDIO
STANDBY
+12VF
+12V
+AUDIO-POWER
+1V2-STANDBY
2K8 supplies
2K9 supplies
3.0A T 32V
ENABLE-3V3-5V
DETECT-12V
ENABLE-3V3
VSW
7U10 BC847BW
7U11 BC847BW
7U40-1 BC847BPN(COL)
7U40-2 BC847BPN(COL)
7U41-1 BC847BS(COL)
7U41-2 BC847BS(COL)
BZX384-C8V2
RESERVED
7U0M BC847BW
7U0N TS431AILT
+1V2-STANDBY
7U50 LD3985M122
IN OUT INH BP COM
6U0B BAS316
+33VTUN
7U0P 2N7002
7U0Q BC847BW
BZX384-C27
* IN CASE OF ONLY-ANALOG TUNER

1M20	A1	5U13	A1
1M95	E1	5U14	A1
1M99	C1	5U15	B1
1U01	E2	5U16	B1
1U03	E2	5U17	F2
2U21	B1	5U20	F2
2U22	D2	5U21	F2
2U23	D2	6U0B	E8
2U24	A7	6U0C	E8
2U25	B8	6U40	E3
2U26	B9	7U0M	A9
2U27	F7	7U0N	B7
2U28	F8	7U0P	E7
2U29	E8	7U0Q	E9
2U2A	E8	7U10	B4
2U2B	E8	7U11	B3
2U2C	B1	7U40-1	E3
2U30	D2	7U40-2	E4
2U31	D3	7U41-1	F4
2U32	E1	7U41-2	F5
2U33	F1	7U50	C7
2U34	F1	9U06	A2
2U35	F1	9U07	B3
2U36	F1	9U08	B5
2U37	C1	CU70	D1
2U40	F3	CU71	D1
2U41	A2	FU10	F1
2U42	A2	FU11	F1
2U43	A2	FU12	F1
2U44	A2	FU13	C1
2U45	B2	FU14	C1
2U46	B2	FU15	C2
2U47	D8	FU16	C1
2U48	D8	FU17	C2
2U49	D7	FU18	C2
2U51	D1	FU19	C1
2U52	D1	FU1A	E1
2U53	C1	FU1B	E1
3U35	B6	FU1C	E1
3U37	A6	FU1D	F1
3U3V	B8	FU1F	B9
3U3W	A8	FU1G	E9
3U3Y	E6	FU1H	C4
3U3Z	F6	FU20	E1
3U40	E8	FU21	E1
3U41	B5	FU22	E1
3U42	E9	FU23	E1
3U43	E8	FU24	C1
3U44	E9	FU25	D1
3U45	E9	FU26	D1
3U46	A8	FU30	A1
3U47	E8	FU31	A1
3U4A	B8	FU32	A1
3U4B	B4	FU33	A1
3U55	C3	FU34	A1
3U56	C3	FU35	A1
3U57	C3	FU36	B1
3U58	C3	FU38	B1
3U59	B6	FU39	E5
3U60	E5	FU40	F4
3U61	E5	IU20	B4
3U62	F5	IU21	B4
3U63	F5	IU34	A8
3U64	C2	IU35	B8
3U65	C2	IU36	F7
3U66	D1	IU37	F8
3U67	D2	IU38	E7
3U80	E3	IU39	F9
3U81	E3	IU3B	E8
3U82	E4	IU3C	B8
3U83	E4	IU3T	C8
3U84	F2	IU40	E3
3U85	F4	IU41	E3
3U86	F4	IU42	E4
3U88	F3	IU43	E3
3U89	F3	IU44	F3
3U90	A3	IU45	F4
3U91	A3	IU47	F3
3U92	A3	IU48	A4
3U93	B2	IU49	A4
3U94	B3	IU50	A5
3U95	B3	IU51	A3
3U96	A4	IU52	B3
3U97	A4	IU53	B4
3U98	C3	IU54	F5
5U06	F2		
5U07	A1		
5U08	E7		
5U10	A1		
5U11	A1		
5U12	A1		

CHN	SETNAME		
CLASS_NO	DC/DC TV543 R2 LDIPNX	8204 000 8932	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS.	3	130 - 2 A3
CHECK	DATE 2007-11-20	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

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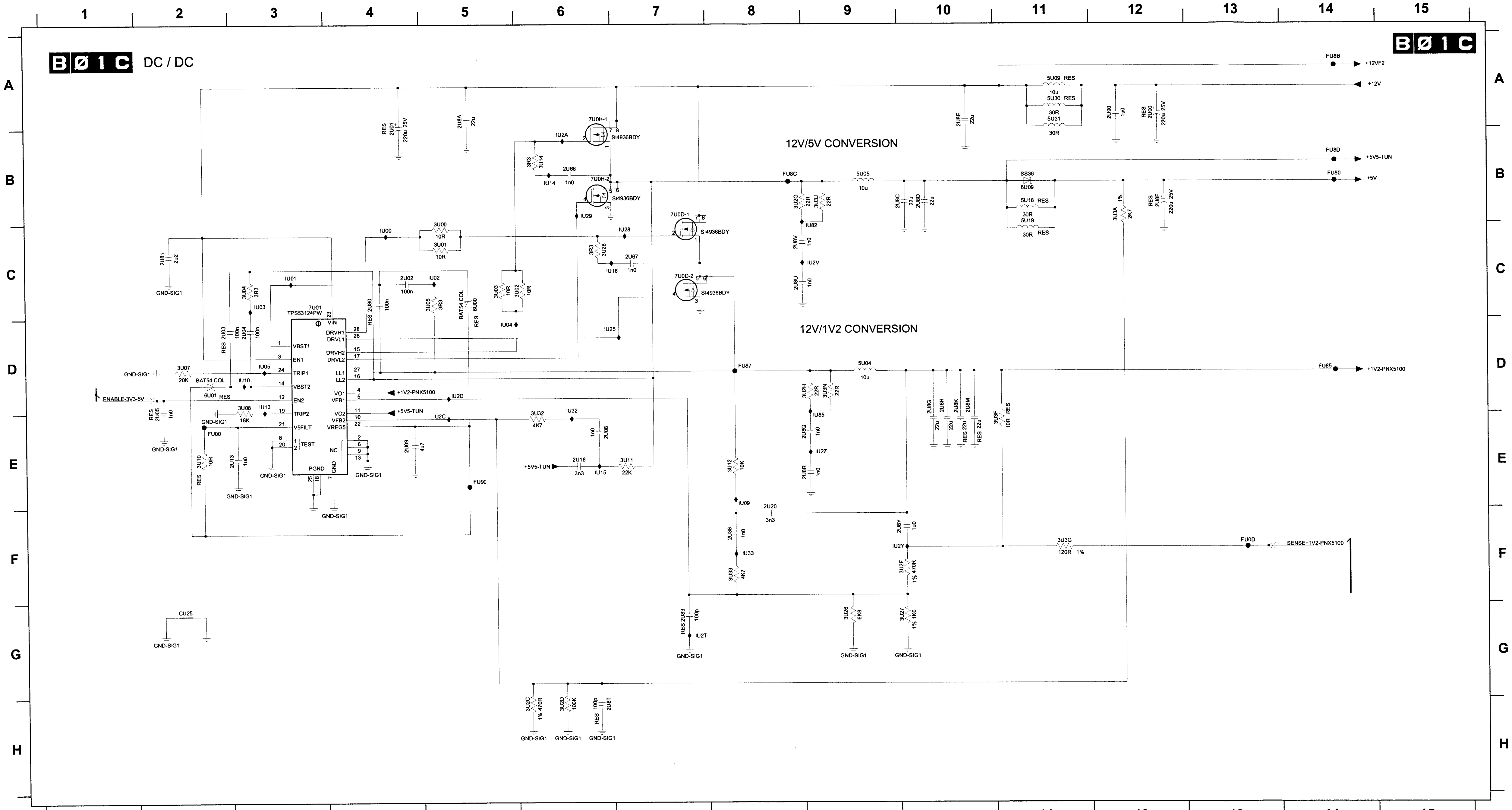
090302

SSB: DC/DC

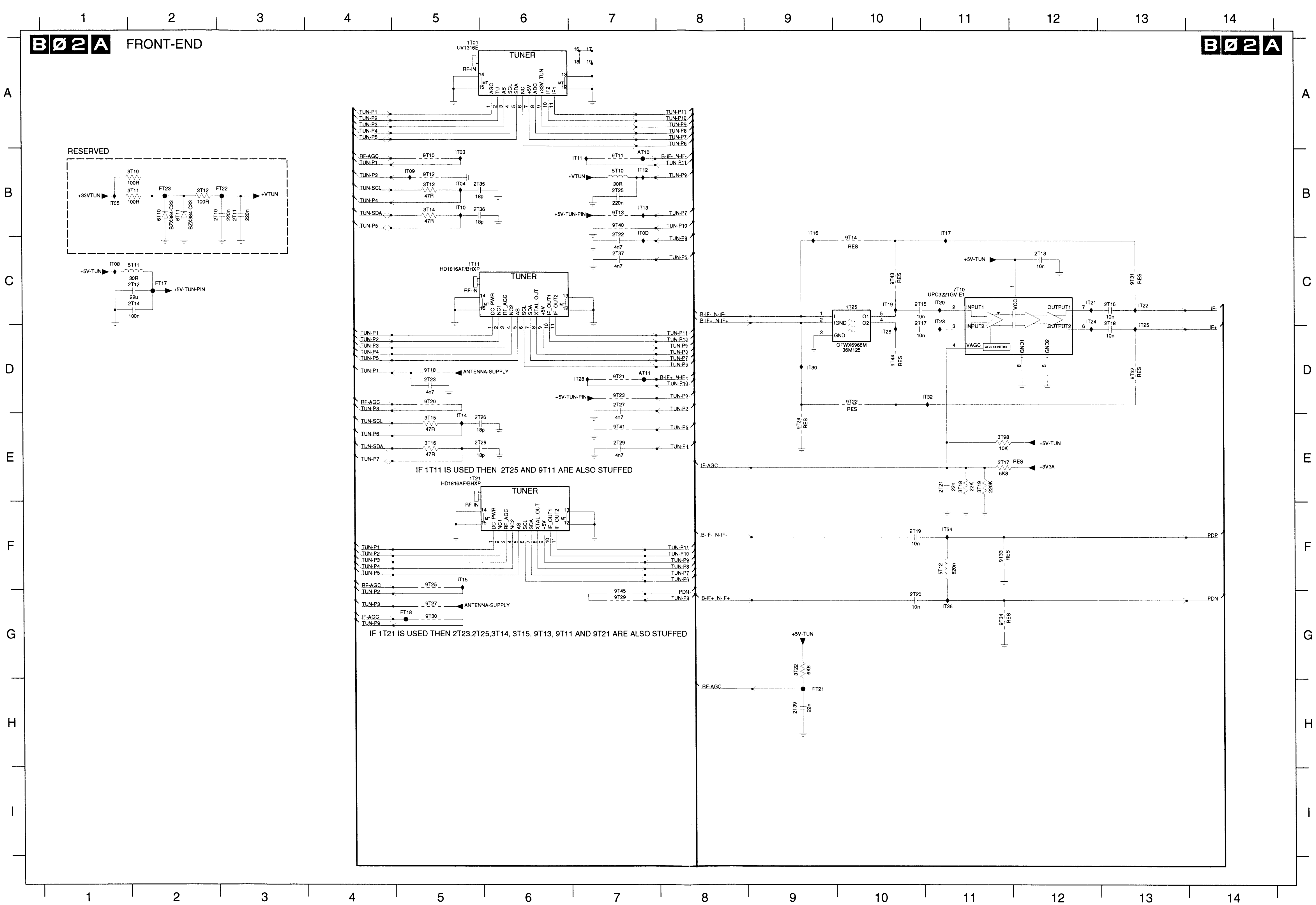
2U00 A12
2U01 A4
2U02 C4
2U03 D2
2U04 D3
2U05 D2
2U08 E6
2U09 E4
2U13 E3
2U18 E6
2U20 F8
2U38 F8
2U66 B6
2U67 C7
2U80 C4
2U81 C2
2U83 G7
2U8A A5
2U8C B10
2U8D B10
2U8E A10
2U8F B12
2U8G D10
2U8H D10
2U8K D10
2U8M D10
2U8Q E9
2U8R E9
2U8T H6
2U8U C8
2U8V C8
2U8Y F9
2U90 A12
3U00 C5
3U01 C5
3U02 C6
3U03 C5
3U04 C3
3U05 C5
3U07 D2
3U08 D3
3U10 E2
3U11 E7
3U12 E8
3U14 B6
3U26 G9
3U27 G10
3U28 C6
3U2C H6
3U2D H6
3U2F F10
3U2G B8
3U2H D9
3U32 E6
3U33 F8
3U3A B12
3U3F E11
3U3G F11
3U3J B9
3U3N D9
5U04 D9
5U05 B9
5U09 A11
5U18 B11
5U19 C11
5U30 A11
5U31 A11
6U00 C5
6U01 D2
6U09 B11
7U01 C3
7U0D-1 B7
7U0D-2 C7
7U0H-1 A6
7U0H-2 B6
CU25 G2
FU00 E2
FU0D F13
FU80 B14
FU85 D14
FU87 D8
FU8B A14
FU8C B8
FU8D B14
FU90 E5
IU00 C4
IU01 C3
IU02 C5
IU03 C3
IU04 D5
IU05 D3
IU09 E8
IU10 D3
IU13 D3
IU14 B6
IU15 E6
IU16 C7
IU25 D6
IU28 C7
IU29 B6
IU2A B6
IU2C E5
IU2D D5
IU2T G7
IU2V C9
IU2Y F9
IU2Z E9
IU32 D6
IU33 F8
IU82 C9
IU85 E9


B01C
DC / DC
12V/5V CONVERSION
12V/1V2 CONVERSION
7U01 TPS53124PW
7U0H-1 SI4936BDY
7U0H-2 SI4936BDY
7U0D-1 SI4936BDY
7U0D-2 SI4936BDY
VIN
VBST1
EN1
TRIP1
VBST2
EN2
TRIP2
V5FILT
TEST
PGND
GND
DRVH1
DRVL1
DRVH2
DRVL2
LL1
LL2
VO1
VFB1
VO2
VFB2
VREG5
NC
+12VF2
+12V
+5V5-TUN
+5V
+1V2-PNX5100
SENSE+1V2-PNX5100
ENABLE-3V3-5V
GND-SIG1
BAT54 COL
5U09 RES
5U30 RES
5U31
5U05 10u
5U04 10u
5U18 RES
5U19
SS36
3U3G 120R 1%
FU8B
FU8D
FU80
FU85
FU87
FU8C
FU0D
FU00
FU90
CU25

CHN
SETNAME
CLASS_NO
2008-10-10 3
DC/DC
TV543 R2 LDIPNX
8204 000 8932
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 3
130 – 3
A2
CHECK
DATE 2007-11-20

18310_502_090302.eps
090302

SSB: Front End

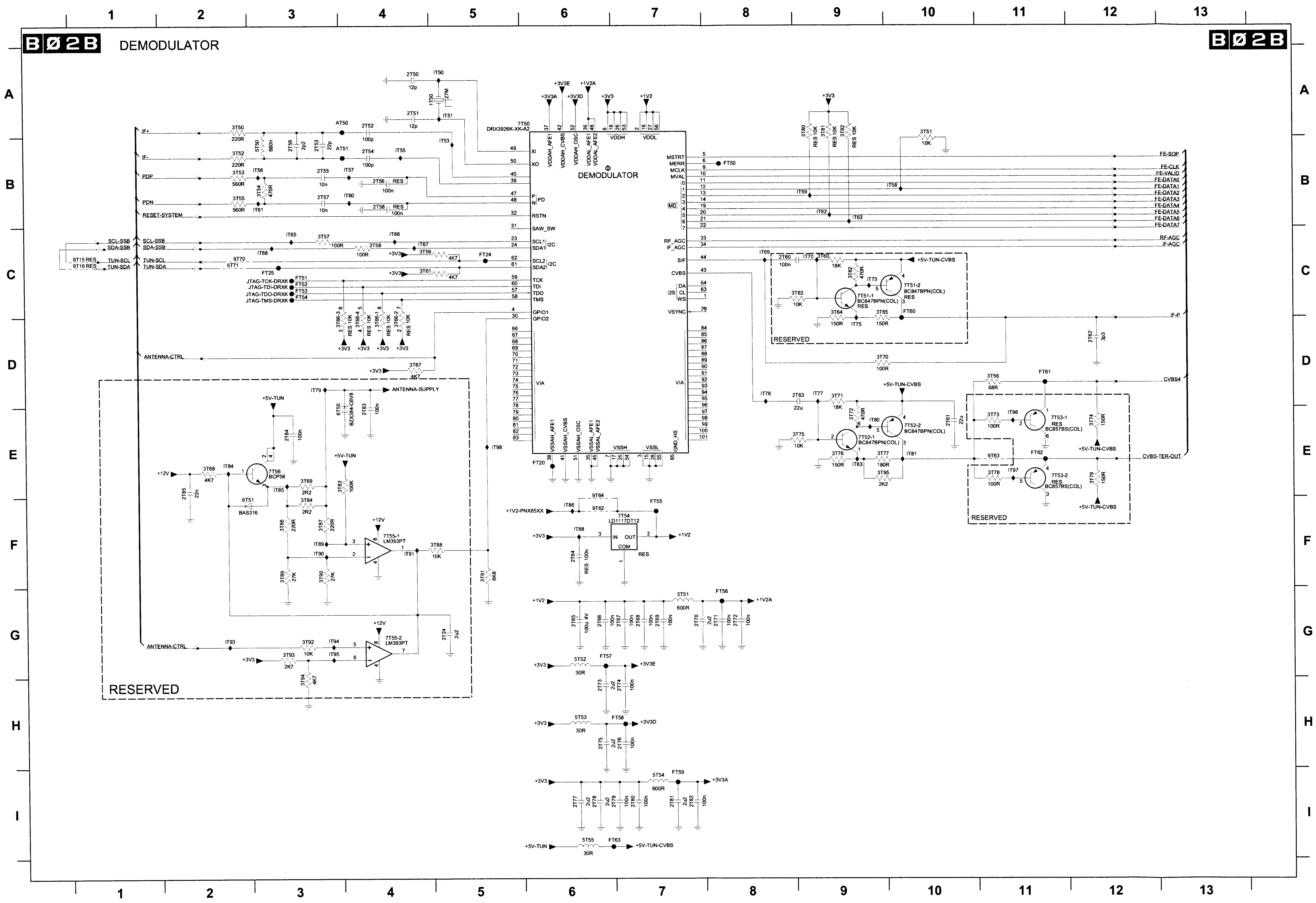

B02A FRONT-END
B02A
RESERVED
TUNER
1T01
UV1316E
1T11
HD1816AF/BHXP
1T21
HD1816AF/BHXP
RF-IN
+33VTUN
+VTUN
+5V-TUN
+5V-TUN-PIN
ANTENNA-SUPPLY
RF-AGC
IF-AGC
TUN-SCL
TUN-SDA
B-IF- N-IF-
B-IF+ N-IF+
7T10
UPC3221GV-E1
1T25
OFWX6966M
36M125
INPUT1
INPUT2
OUTPUT1
OUTPUT2
VAGC
AGC CONTROL
VCC
GND1
GND2
IF-
IF+
PDP
PDN
+3V3A
IF 1T11 IS USED THEN 2T25 AND 9T11 ARE ALSO STUFFED
IF 1T21 IS USED THEN 2T23,2T25,3T14, 3T15, 9T13, 9T11 AND 9T21 ARE ALSO STUFFED

1T01	A5
1T11	C5
1T21	E5
1T25	C10
2T10	B3
2T11	B3
2T12	C2
2T13	C12
2T14	C2
2T15	C10
2T16	C13
2T17	C10
2T18	C13
2T19	F10
2T20	G10
2T21	E11
2T22	B7
2T23	D5
2T25	B7
2T26	E5
2T27	D7
2T28	E5
2T29	E7
2T35	B5
2T36	B5
2T37	C7
2T39	H9
3T10	B2
3T11	B2
3T12	B2
3T13	B5
3T14	B5
3T15	E5
3T16	E5
3T17	E11
3T18	E11
3T19	E11
3T22	G9
3T98	E11
5T10	B7
5T11	C2
5T12	F11
6T10	B2
6T11	B2
7T10	C11
9T10	B5
9T11	B7
9T12	B5
9T13	B7
9T14	C10
9T18	D5
9T20	D5
9T21	D7
9T22	D10
9T23	D7
9T24	E9
9T25	F5
9T27	G5
9T29	G7
9T30	G5
9T31	C13
9T32	D13
9T33	F11
9T34	G11
9T40	B7
9T41	E7
9T43	C10
9T44	D10
9T45	G7
AT10	B7
AT11	D7
FT17	C2
FT18	G5
FT21	H9
FT22	B3
FT23	B2
IT03	B5
IT04	B5
IT05	B1
IT08	C1
IT09	B5
IT0D	B7
IT10	B5
IT11	B7
IT12	B7
IT13	B7
IT14	E5
IT15	F5
IT16	B9
IT17	B11
IT19	C10
IT20	C11
IT21	C12
IT22	C13
IT23	C11
IT24	C12
IT25	C13
IT26	D10
IT28	D7
IT30	D9
IT32	D11
IT34	F11
IT36	G11

CHN
SETNAME
CLASS_NO
FRONT-END
TV543 R2 LDIPNX
8204 000 8929
2 2008-11-21
2008-10-10 3
NAME Randal De Keyzer
SUPERS. 3
130 - 1
A2
CHECK
DATE 2008-06-03

18310_503_090302.eps
090302

SSB: Demodulator


B02B
DEMODULATOR
7T50
DRX3926K-XK-A2
DEMODULATOR
IF+
IF-
PDP
PDN
RESET-SYSTEM
SCL-SSB
SDA-SSB
TUN-SCL
TUN-SDA
9T15 RES
9T16 RES
9T70
9T71
JTAG-TCK-DRXK
JTAG-TDI-DRXK
JTAG-TDO-DRXK
JTAG-TMS-DRXK
ANTENNA-CTRL
ANTENNA-SUPPLY
XI
XO
RSTN
SAW_SW
SCL1
SDA1
SCL2
SDA2
I2C
TCK
TDI
TDO
TMS
GPIO1
GPIO2
VIA
VDDAH_AFE1
VDDAH_CVBS
VDDAH_OSC
VDDAL_AFE1
VDDAL_AFE2
VDDH
VDDL
VSSH
VSSL
MSTRT
MERR
MCLK
MVAL
MD
RF_AGC
IF_AGC
SIF
CVBS
I2S
DA
CL
WS
VSYNC
FE-SOP
FE-CLK
FE-VALID
FE-DATA0
FE-DATA1
FE-DATA2
FE-DATA3
FE-DATA4
FE-DATA5
FE-DATA6
FE-DATA7
RF-AGC
IF-AGC
IF-P
CVBS4
CVBS-TER-OUT
+5V-TUN-CVBS
7T51-1 BC847BPN(COL) RES
7T51-2 BC847BPN(COL) RES
7T52-1 BC847BPN(COL)
7T52-2 BC847BPN(COL)
7T53-1 RES BC857BS(COL)
7T53-2 RES BC857BS(COL)
7T56 BCP56
6T50 BZX384-C6V8
6T51 BAS316
7T55-1 LM393PT
7T55-2 LM393PT
7T54 LD1117DT12
IN OUT COM
+1V2-PNX85XX
+1V2
+1V2A
+3V3
+3V3A
+3V3D
+3V3E
+5V-TUN
+12V
RESERVED

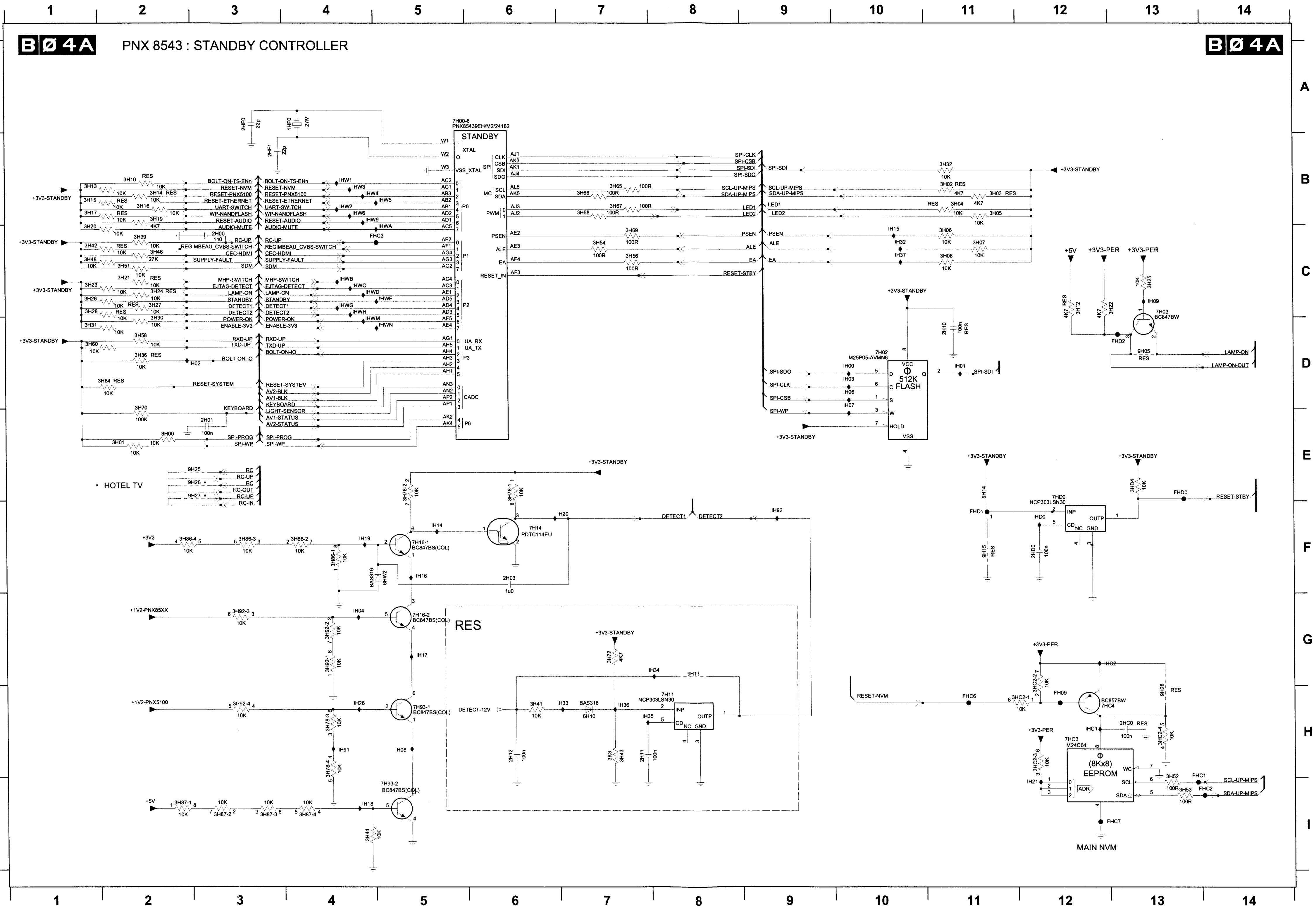
1T50 A5	AT50 A4
2T24 G5	AT51 B4
2T50 A4	FT20 E6
2T51 A4	FT24 C5
2T52 A4	FT25 C3
2T53 B3	FT50 B8
2T54 B4	FT51 C3
2T55 B3	FT52 C3
2T56 B4	FT53 C3
2T57 B3	FT54 C3
2T58 B4	FT55 F7
2T59 B3	FT56 G8
2T60 C8	FT57 G6
2T61 E10	FT58 H7
2T62 D12	FT59 I7
2T63 D9	FT60 C10
2T64 F6	FT61 D11
2T65 G6	FT62 E11
2T66 G6	FT63 I6
2T67 G7	IT50 A5
2T68 G7	IT51 A5
2T69 G7	IT53 B5
2T70 G7	IT55 B4
2T71 G8	IT56 B3
2T72 G8	IT57 B4
2T73 H6	IT58 B10
2T74 H7	IT59 B9
2T75 H6	IT60 B4
2T76 H7	IT61 B3
2T77 I6	IT62 B9
2T78 I6	IT63 B9
2T79 I6	IT65 C3
2T80 I7	IT66 C4
2T81 I7	IT67 C4
2T82 I7	IT68 C3
2T83 E4	IT69 C8
2T84 E3	IT70 C9
2T85 E2	IT73 C9
3T50 A2	IT75 D9
3T51 A10	IT76 D8
3T52 B2	IT77 D9
3T53 B2	IT79 D3
3T54 B3	IT80 E9
3T55 B2	IT81 E10
3T56 D11	IT83 E9
3T57 C3	IT84 E2
3T58 C4	IT85 E3
3T59 C4	IT86 F6
3T60 C9	IT88 F6
3T61 C4	IT89 F3
3T62 C9	IT90 F3
3T63 C9	IT91 F4
3T64 C9	IT93 G2
3T65 C9	IT94 G3
3T66-1 D4	IT95 G3
3T66-2 D4	IT96 E11
3T66-3 D3	IT97 E11
3T66-4 D4	IT98 E5
3T67 D4	
3T68 E2	
3T69 E3	
3T70 D9	
3T71 D9	
3T72 E9	
3T73 E11	
3T74 E12	
3T75 E9	
3T76 E9	
3T77 E9	
3T78 E11	
3T79 E12	
3T80 A9	
3T81 A9	
3T82 A9	
3T83 E3	
3T84 F3	
3T86 F3	
3T87 F3	
3T88 F5	
3T89 F3	
3T90 F3	
3T91 F5	
3T92 G3	
3T93 G3	
3T94 H3	
3T95 E9	
5T50 B3	
5T51 G7	
5T52 G6	
5T53 H6	
5T54 I7	
5T55 I6	
6T50 E3	
6T51 F2	
7T50 A6	
7T51-1 C9	
7T51-2 C10	
7T52-1 E9	
7T52-2 E10	
7T53-1 E11	
7T53-2 E11	
7T54 F7	
7T55-1 F4	
7T55-2 G4	
7T56 E3	
9T15 C1	
9T16 C1	
9T62 F6	
9T63 E11	
9T64 F6	
9T70 C2	
9T71 C2	

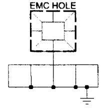
PHILIPS

	SETNAME		
CLASS_NO	FRONT-END TV543 R2 LDIPNX	8204 000 8929	2 2008-11-21
2008-10-10 3			
NAME Randal De Keyzer	SUPERS. 3	130 - 2	A2
CHECK	DATE 2008-06-03		

18310_504_090302.eps
090302

SSB: PNX8543 - Stand-by Controller


B04A
PNX 8543 : STANDBY CONTROLLER
7H00-6
PNX85439EH/M2/24182
STANDBY
XTAL
VSS_XTAL
SPI
MC
PWM
P0
P1
P2
P3
CADC
P6
RESET_IN
BOLT-ON-TS-ENn
RESET-NVM
RESET-PNX5100
RESET-ETHERNET
UART-SWITCH
WP-NANDFLASH
RESET-AUDIO
AUDIO-MUTE
RC-UP
REGIMBEAU_CVBS-SWITCH
CEC-HDMI
SUPPLY-FAULT
SDM
MHP-SWITCH
EJTAG-DETECT
LAMP-ON
STANDBY
DETECT1
DETECT2
POWER-OK
ENABLE-3V3
RXD-UP
TXD-UP
BOLT-ON-IO
RESET-SYSTEM
AV2-BLK
AV1-BLK
KEYBOARD
LIGHT-SENSOR
AV1-STATUS
AV2-STATUS
SPI-PROG
SPI-WP
SPI-CLK
SPI-CSB
SPI-SDI
SPI-SDO
SCL-UP-MIPS
SDA-UP-MIPS
LED1
LED2
PSEN
ALE
EA
RESET-STBY
+3V3-STANDBY
7H02
M25P05-AVMN6
512K
FLASH
HOLD
VSS
+5V
+3V3-PER
7H03
BC847BW
LAMP-ON
LAMP-ON-OUT
• HOTEL TV
RC
RC-UP
I²C-OUT
RC-IN
+3V3
+1V2-PNX85XX
+1V2-PNX5100
7H14
PDTC114EU
7H16-1
BC847BS(COL)
7H16-2
BC847BS(COL)
7H93-1
BC847BS(COL)
7H93-2
BC847BS(COL)
DETECT1
DETECT2
RES
DETECT-12V
7H11
NCP303LSN30
INP
OUTP
CD
NC GND
7HD0
NCP303LSN30
RESET-STBY
RESET-NVM
7HC4
BC857BW
7HC3
M24C64
(8Kx8)
EEPROM
WC
SCL
SDA
ADR
SCL-UP-MIPS
SDA-UP-MIPS
MAIN NVM

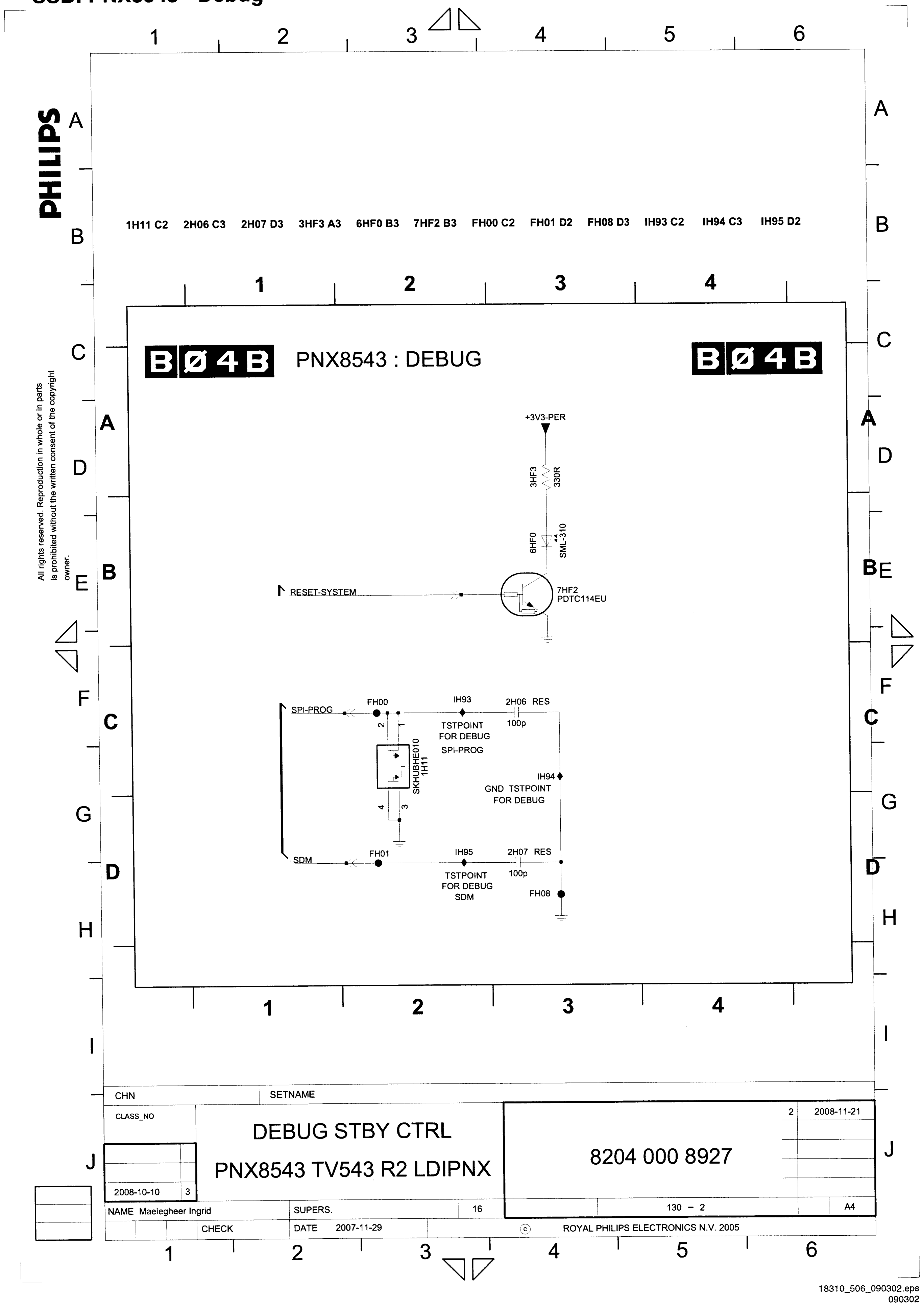

1X03
EMC HOLE

1HF0	A4
2H00	C3
2H01	E3
2H03	F6
2H10	D11
2H11	H7
2H12	H6
2HC0	H13
2HD0	F12
2HF0	A3
2HF1	B3
3H00	E2
3H01	E2
3H02	B11
3H03	B11
3H04	B11
3H05	B11
3H06	C11
3H07	C11
3H08	C11
3H10	B2
3H12	C12
3H13	B1
3H14	B2
3H15	B1
3H16	B2
3H17	B1
3H19	B2
3H20	C1
3H21	C2
3H22	C13
3H23	C1
3H24	C2
3H25	C13
3H26	C1
3H27	C2
3H28	C1
3H30	D2
3H31	D1
3H32	B11
3H36	D2
3H39	C2
3H41	H6
3H42	C1
3H43	H7
3H44	I4
3H46	C2
3H48	C1
3H51	C2
3H52	I13
3H53	I13
3H54	C7
3H56	C7
3H58	D2
3H60	D1
3H64	D2
3H65	B7
3H66	B7
3H67	B7
3H68	B7
3H69	C7
3H70	E2
3H72	G7
3H78-1	E6
3H78-2	E5
3H78-3	H4
3H78-4	H4
3H86-1	F4
3H86-2	F4
3H86-3	F3
3H86-4	F2
3H87-1	I2
3H87-2	I3
3H87-3	I3
3H87-4	I4
3H92-1	G4
3H92-2	G4
3H92-3	G3
3H92-4	H3
3HC2-1	H12
3HC2-2	G12
3HC2-3	H12
3HC2-4	H13
3HD4	E13
6H10	H7
6HW2	F5
7H00-6	A5
7H02	D10
7H03	C13
7H11	H8
7H14	F6
7H16-1	F5
7H16-2	G5
7H93-1	H5
7H93-2	I5
7HC3	H12
7HC4	H12
7HD0	E12
9H05	D13
9H13	G8
9H14	E11
9H15	F11
9H25	E3
9H26	E3
9H27	E3
9H28	H13
FH09	H12
FHC1	H13
FHC2	I14
FHC3	C5
FHC6	H11
FHC7	I13
FHD0	E13
FHD1	F11
FHD2	D13
IH00	D10
IH01	D11
IH02	D3
IH03	D10
IH04	G4
IH06	D10
IH07	D10
IH08	H5
IH09	C13
IH14	F5
IH15	C10
IH16	F5
IH17	G5
IH18	I4
IH19	F4
IH20	F7
IH21	I12
IH26	H4
IH32	C10
IH33	H7
IH34	G8
IH35	H7
IH36	H7
IH37	C10
IH91	H4
IH92	F9
IHC1	H12
IHC2	G12
IHD0	F12
IHW1	B4
IHW2	B4
IHW3	B4
IHW4	B4
IHW5	B5
IHW6	B4
IHW9	B4
IHWA	C5
IHWB	C4
IHWC	C4
IHWD	C4
IHWF	C5
IHWG	C4
IHWH	C4
IHWM	D4
IHWN	D5

CHN
SETNAME
CLASS_NO
2008-10-10 3
STANDBY CONTROLLER
PNX8543 TV543 R2 LDIPNX
8204 000 8927
2 2008-11-21
NAME Randal De Keyzer
SUPERS.
16
130 - 1
A2
CHECK
DATE 2007-11-29

18310_505_090302.eps
090302

SSB: PNX8543 - Debug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1H11 C2
2H06 C3
2H07 D3
3HF3 A3
6HF0 B3
7HF2 B3
FH00 C2
FH01 D2
FH08 D3
IH93 C2
IH94 C3
IH95 D2
B04B
PNX8543 : DEBUG
+3V3-PER
3HF3
330R
6HF0
SML-310
RESET-SYSTEM
7HF2
PDTC114EU
SPI-PROG
FH00
IH93
2H06 RES
100p
TSTPOINT
FOR DEBUG
SPI-PROG
SKHUBHE010
1H11
IH94
GND TSTPOINT
FOR DEBUG
SDM
FH01
IH95
2H07 RES
100p
TSTPOINT
FOR DEBUG
SDM
FH08
CHN
SETNAME
CLASS_NO
DEBUG STBY CTRL
PNX8543 TV543 R2 LDIPNX
8204 000 8927
2
2008-11-21
2008-10-10
3
NAME Maelegheer Ingrid
SUPERS.
16
130 - 2
A4
CHECK
DATE 2007-11-29
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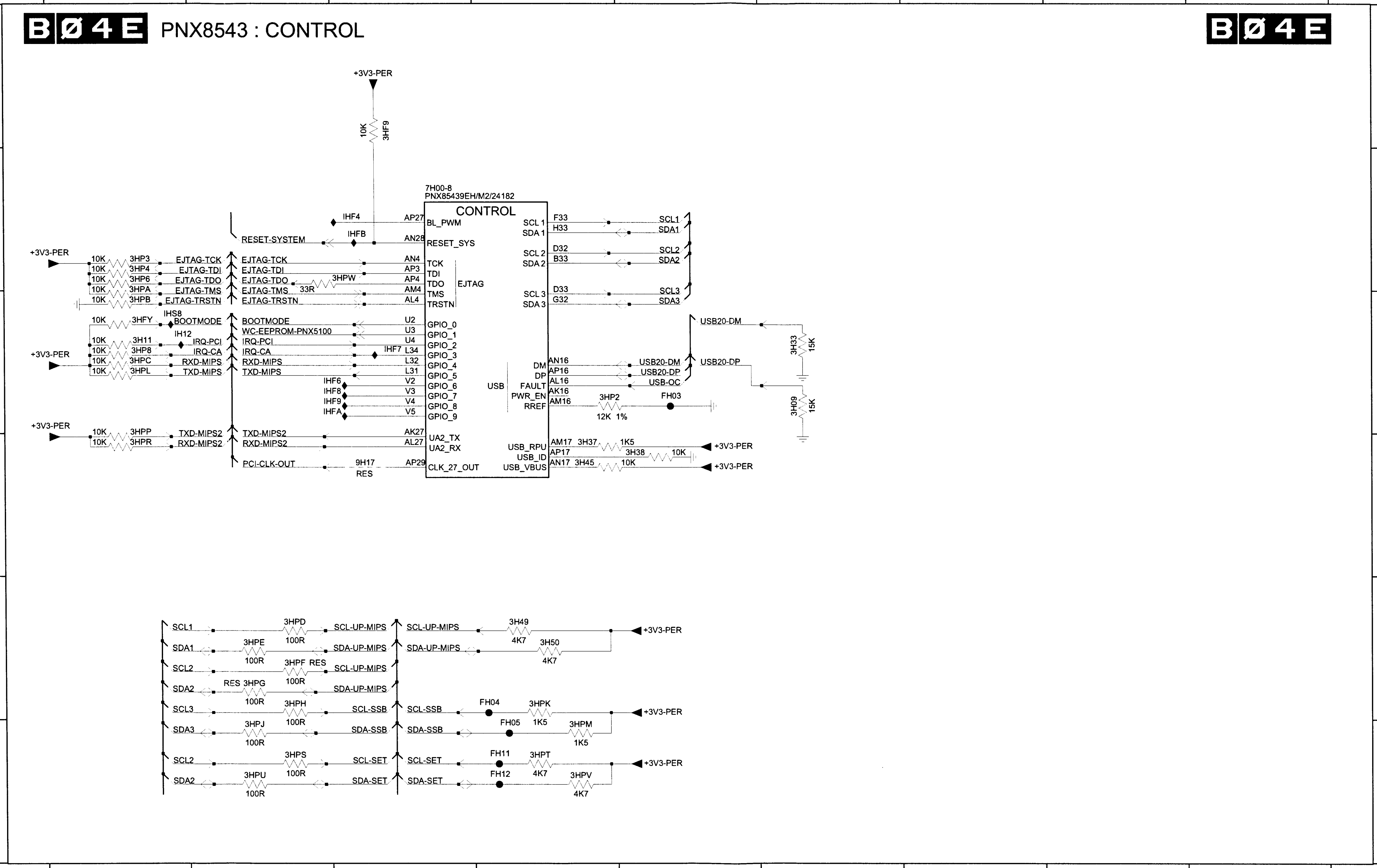
18310_506_090302.eps
090302

Personal Notes:

10000_012_090121.eps
090121

SSB: PNX8543 - Control

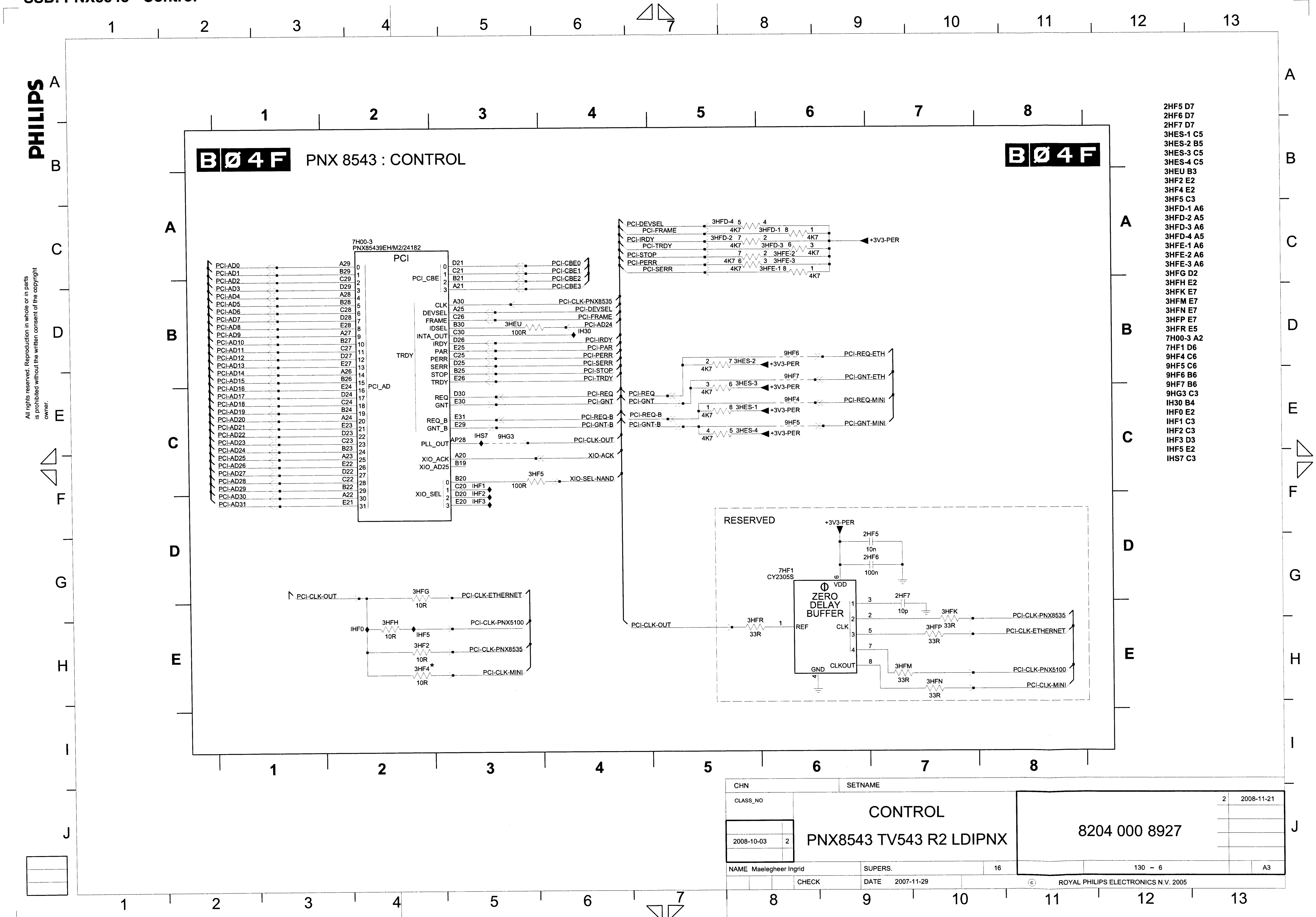

B04E
PNX8543 : CONTROL
B04E
+3V3-PER
10K
3HF9
7H00-8
PNX85439EH/M2/24182
CONTROL
IHF4
AP27
BL_PWM
RESET-SYSTEM
IHFB
AN28
RESET_SYS
+3V3-PER
10K 3HP3 EJTAG-TCK
10K 3HP4 EJTAG-TDI
10K 3HP6 EJTAG-TDO
10K 3HPA EJTAG-TMS
10K 3HPB EJTAG-TRSTN
EJTAG-TCK
EJTAG-TDI
EJTAG-TDO
3HPW
33R
EJTAG-TMS
EJTAG-TRSTN
AN4 TCK
AP3 TDI
AP4 TDO
AM4 TMS
AL4 TRSTN
EJTAG
IHS8
10K 3HFY BOOTMODE
IH12
10K 3H11 IRQ-PCI
+3V3-PER
10K 3HP8 IRQ-CA
10K 3HPC RXD-MIPS
10K 3HPL TXD-MIPS
BOOTMODE
WC-EEPROM-PNX5100
IRQ-PCI
IRQ-CA
RXD-MIPS
TXD-MIPS
IHF7
U2 GPIO_0
U3 GPIO_1
U4 GPIO_2
L34 GPIO_3
L32 GPIO_4
L31 GPIO_5
IHF6 V2 GPIO_6
IHF8 V3 GPIO_7
IHF9 V4 GPIO_8
IHFA V5 GPIO_9
+3V3-PER
10K 3HPP TXD-MIPS2
10K 3HPR RXD-MIPS2
TXD-MIPS2
RXD-MIPS2
AK27 UA2_TX
AL27 UA2_RX
PCI-CLK-OUT
9H17
RES
AP29 CLK_27_OUT
SCL 1 F33 SCL1
SDA 1 H33 SDA1
SCL 2 D32 SCL2
SDA 2 B33 SDA2
SCL 3 D33 SCL3
SDA 3 G32 SDA3
USB
DM AN16 USB20-DM
DP AP16 USB20-DP
FAULT AL16 USB-OC
PWR_EN AK16
RREF AM16
3HP2
12K 1%
FH03
USB20-DM
USB20-DP
3H33
15K
3H09
15K
USB_RPU AM17 3H37 1K5
USB_ID AP17 3H38 10K
USB_VBUS AN17 3H45 10K
+3V3-PER
+3V3-PER
SCL1 3HPD 100R SCL-UP-MIPS
SDA1 3HPE 100R SDA-UP-MIPS
SCL2 3HPF RES 100R SCL-UP-MIPS
SDA2 RES 3HPG 100R SDA-UP-MIPS
SCL3 3HPH 100R SCL-SSB
SDA3 3HPJ 100R SDA-SSB
SCL2 3HPS 100R SCL-SET
SDA2 3HPU 100R SDA-SET
SCL-UP-MIPS 3H49 4K7
SDA-UP-MIPS 3H50 4K7
+3V3-PER
SCL-SSB FH04 3HPK 1K5
SDA-SSB FH05 3HPM 1K5
+3V3-PER
SCL-SET FH11 3HPT 4K7
SDA-SET FH12 3HPV 4K7
+3V3-PER

3H09	C6
3H11	C1
3H33	C6
3H37	D4
3H38	D5
3H45	D4
3H49	E4
3H50	E4
3HF9	A3
3HFY	C1
3HP2	C4
3HP3	B1
3HP4	B1
3HP6	B1
3HP8	C1
3HPA	C1
3HPB	C1
3HPC	C1
3HPD	E2
3HPE	E2
3HPF	E2
3HPG	E2
3HPH	E2
3HPJ	F2
3HPK	E4
3HPL	C1
3HPM	F4
3HPP	D1
3HPR	D1
3HPS	F2
3HPT	F4
3HPU	F2
3HPV	F4
3HPW	B3
7H00-8	B3
9H17	D3
FH03	C5
FH04	E4
FH05	F4
FH11	F4
FH12	F4
IH12	C1
IHF4	B3
IHF6	C3
IHF7	C3
IHF8	C3
IHF9	C3
IHFA	C3
IHFB	B3
IHS8	C1

CHN
SETNAME
CLASS_NO
2008-10-10 3
MIPS , I2C & EJTAG
PNX8543 TV543 R2 LDIPNX
8204 000 8927
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 16
130 - 5
A3
CHECK
DATE 2007-11-29

18310_507_090302.eps
090302

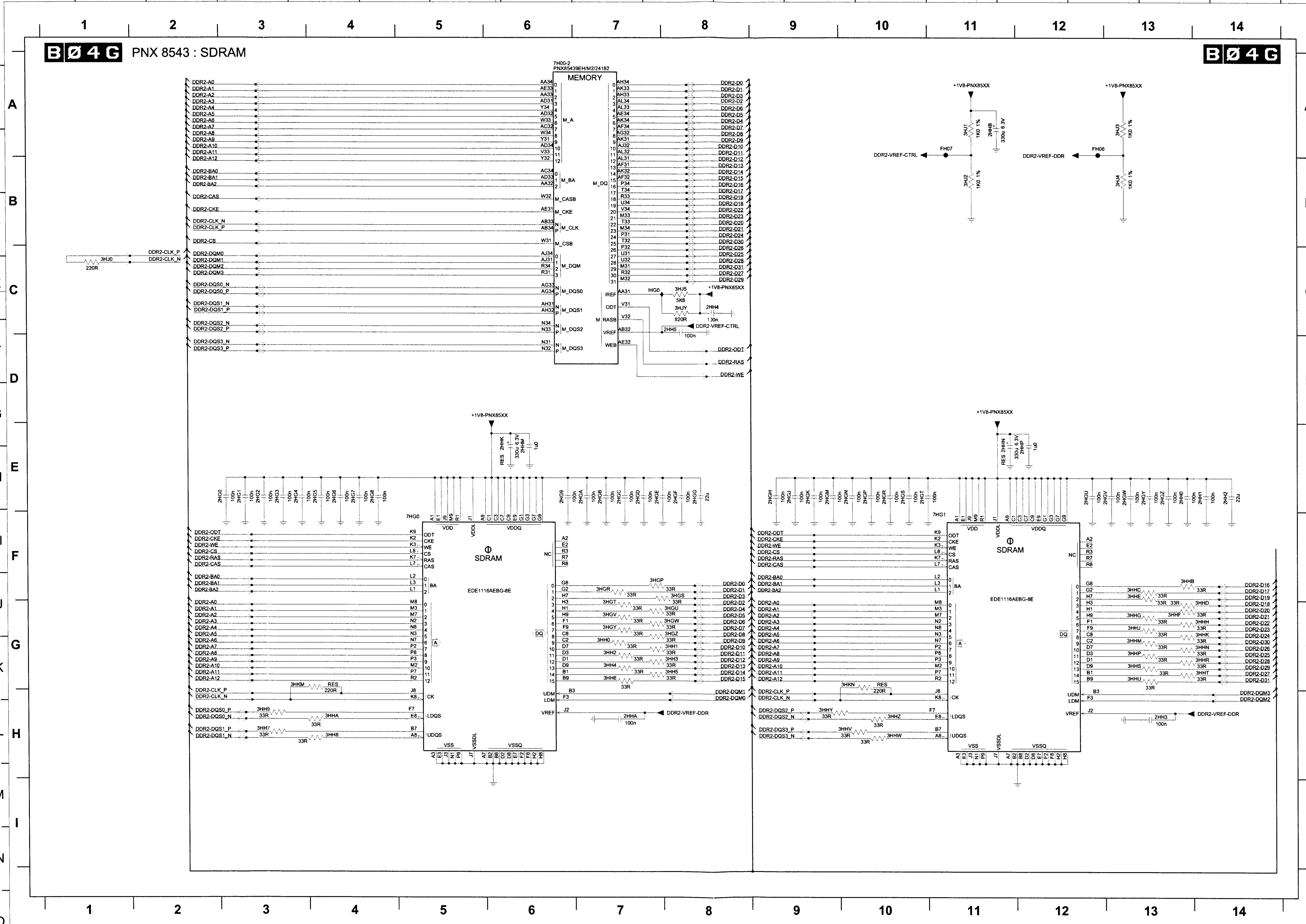
SSB: PNX8543 - Control


PHILIPS
B04F PNX 8543 : CONTROL
B04F
7H00-3
PNX85439EH/M2/24182
PCI
PCI_AD
PCI_CBE
CLK
DEVSEL
FRAME
IDSEL
INTA_OUT
IRDY
PAR
PERR
SERR
STOP
TRDY
REQ
GNT
REQ_B
GNT_B
PLL_OUT
XIO_ACK
XIO_AD25
XIO_SEL
PCI-AD0 … PCI-AD31
PCI-CBE0
PCI-CBE1
PCI-CBE2
PCI-CBE3
PCI-CLK-PNX8535
PCI-DEVSEL
PCI-FRAME
3HEU
100R
PCI-AD24
IH30
PCI-IRDY
PCI-PAR
PCI-PERR
PCI-SERR
PCI-STOP
PCI-TRDY
PCI-REQ
PCI-GNT
PCI-REQ-B
PCI-GNT-B
IHS7
9HG3
PCI-CLK-OUT
XIO-ACK
3HF5
100R
XIO-SEL-NAND
IHF1
IHF2
IHF3
3HFD-4
3HFD-1
3HFD-2
3HFD-3
3HFE-1
3HFE-2
3HFE-3
4K7
+3V3-PER
9HF6
PCI-REQ-ETH
3HES-2
9HF7
PCI-GNT-ETH
3HES-3
9HF4
PCI-REQ-MINI
3HES-1
9HF5
PCI-GNT-MINI
3HES-4
PCI-CLK-OUT
3HFG
10R
PCI-CLK-ETHERNET
3HFH
IHF0
IHF5
PCI-CLK-PNX5100
3HF2
PCI-CLK-PNX8535
3HF4*
PCI-CLK-MINI
RESERVED
2HF5
10n
2HF6
100n
7HF1
CY2305S
VDD
ZERO DELAY BUFFER
REF
CLK
GND
CLKOUT
3HFR
33R
2HF7
10p
3HFK
3HFP
3HFM
3HFN

2HF5	D7
2HF6	D7
2HF7	D7
3HES-1	C5
3HES-2	B5
3HES-3	C5
3HES-4	C5
3HEU	B3
3HF2	E2
3HF4	E2
3HF5	C3
3HFD-1	A6
3HFD-2	A5
3HFD-3	A6
3HFD-4	A5
3HFE-1	A6
3HFE-2	A6
3HFE-3	A6
3HFG	D2
3HFH	E2
3HFK	E7
3HFM	E7
3HFN	E7
3HFP	E7
3HFR	E5
7H00-3	A2
7HF1	D6
9HF4	C6
9HF5	C6
9HF6	B6
9HF7	B6
9HG3	C3
IH30	B4
IHF0	E2
IHF1	C3
IHF2	C3
IHF3	D3
IHF5	E2
IHS7	C3

CHN SETNAME
CLASS_NO
CONTROL
PNX8543 TV543 R2 LDIPNX
2008-10-03 2
2 2008-11-21
8204 000 8927
NAME Maelegheer Ingrid SUPERS. 16
CHECK DATE 2007-11-29
130 - 6 A3

SSB: PNX8543 - SDRAM


B04G
PNX 8543 : SDRAM
7H00-2
PNX85439EH/M2/24182
MEMORY
M_A
M_BA
M_DQ
M_CASB
M_CKE
M_CLK
M_CSB
M_DQM
M_DQS0
M_DQS1
M_DQS2
M_DQS3
IREF
ODT
M_RASB
VREF
WEB
+1V8-PNX85XX
DDR2-VREF-CTRL
DDR2-VREF-DDR
FH07
FH06
DDR2-ODT
DDR2-RAS
DDR2-WE
7HG0
7HG1
SDRAM
EDE1116AEBG-8E
VDD
VDDL
VDDQ
VSS
VSSDL
VSSQ
LDQS
UDQS
UDM
LDM
CK
BA
DQ
NC

2HG0	E3
2HG1	E3
2HG2	E3
2HG3	E3
2HG4	E3
2HG5	E4
2HG6	E4
2HG7	E4
2HG8	E4
2HG9	E6
2HGA	E7
2HGB	E7
2HGC	E7
2HGD	E7
2HGE	E7
2HGF	E8
2HGG	E8
2HGH	E9
2HGJ	E9
2HGK	E9
2HGM	E9
2HGN	E10
2HGP	E10
2HGR	E10
2HGS	E10
2HGT	E10
2HGU	E12
2HGV	E13
2HGW	E13
2HGY	E13
2HGZ	E13
2HH0	E13
2HH1	E14
2HH2	E14
2HH3	H13
2HH4	C8
2HH5	C8
2HHA	H7
2HHB	A11
2HHK	E6
2HHM	E6
2HHN	E11
2HHP	E12
3HGP	F7
3HGR	F7
3HGS	F8
3HGT	G7
3HGU	G8
3HGV	G7
3HGW	G8
3HGY	G7
3HGZ	G8
3HH0	G7
3HH1	G8
3HH2	G7
3HH3	G8
3HH4	G7
3HH5	G8
3HH6	G7
3HH7	H3
3HH8	H4
3HH9	H3
3HHA	H4
3HHB	F13
3HHC	F13
3HHD	G14
3HHE	F13
3HHF	G13
3HHG	G13
3HHH	G14
3HHJ	G13
3HHK	G14
3HHM	G13
3HHN	G14
3HHP	G13
3HHR	G14
3HHS	G13
3HHT	G14
3HHU	G13
3HHV	H10
3HHW	H10
3HHY	H9
3HHZ	H10
3HJ0	C1
3HJ1	A11
3HJ2	B11
3HJ3	A13
3HJ4	B13
3HJ5	C8
3HJY	C8
3HKM	G3
3HKN	G10
7H00-2	A7
7HG0	F5
7HG1	F11
FH06	A12
FH07	A11
IHG0	C7

CHN	SETNAME		
CLASS_NO	DDR2 INTERFACE	2	2008-11-21
2008-10-10 3	PNX8543 TV543 R2 LDIPNX	8204 000 8927	
NAME Maelegheer Ingrid	SUPERS. 16	130 – 7	A2
CHECK	DATE 2007-11-29		

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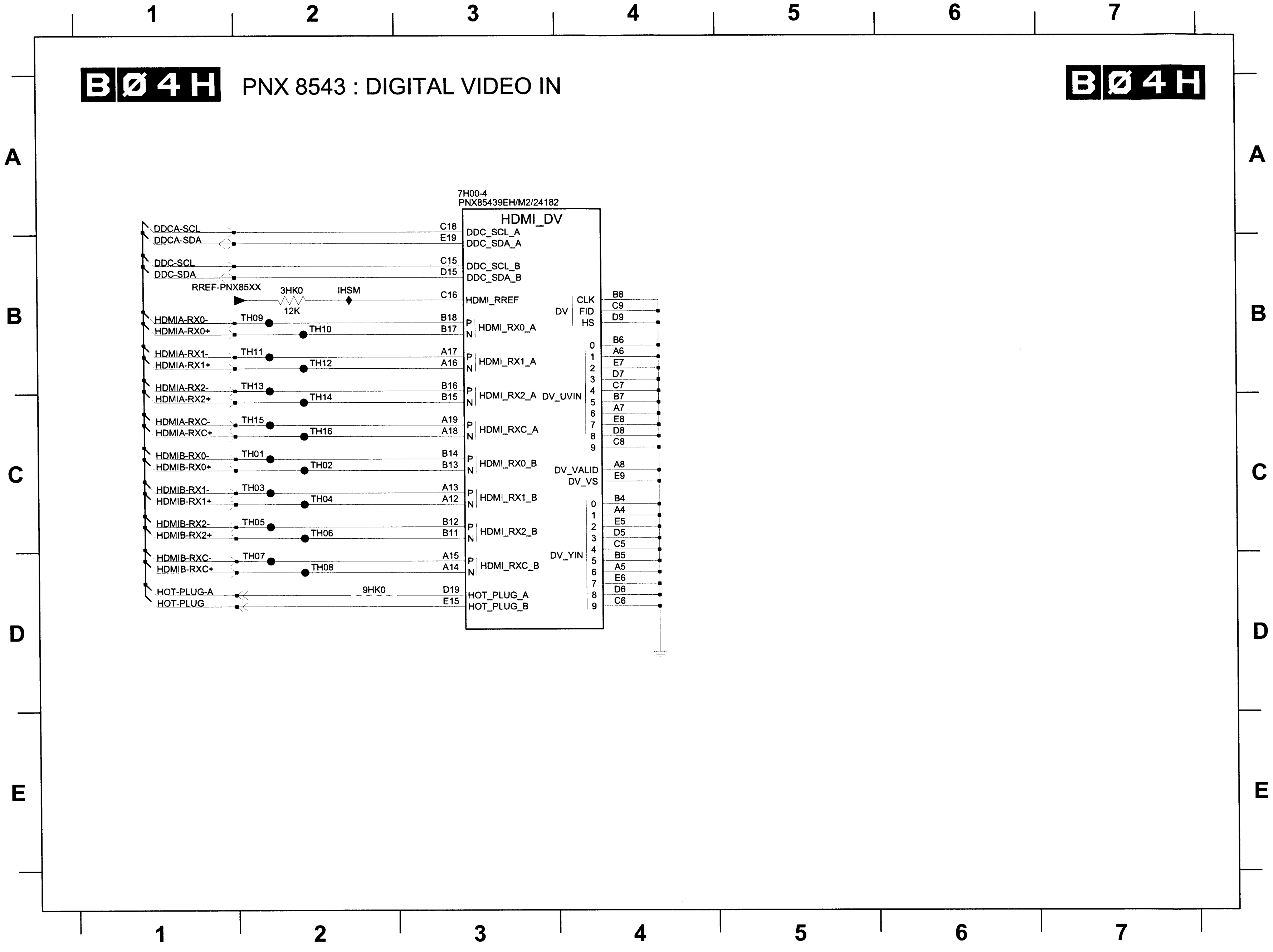
090302

SSB: PNX8543 - Digital Video In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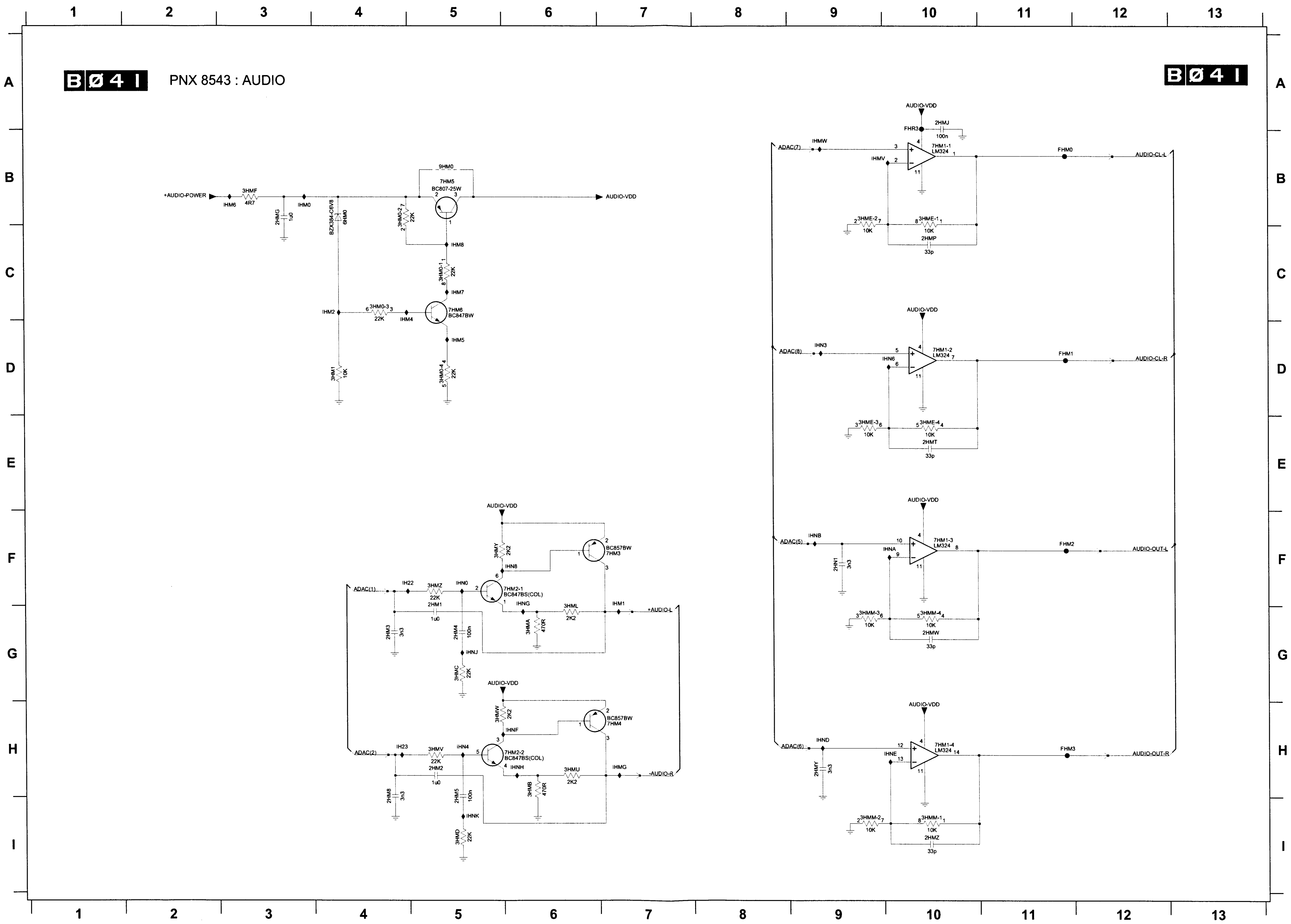
PNX 8543 : DIGITAL VIDEO IN
B04H
7H00-4
PNX85439EH/M2/24182
HDMI_DV
DDCA-SCL
DDCA-SDA
DDC-SCL
DDC-SDA
RREF-PNX85XX
3HK0
12K
IHSM
HDMIA-RX0-
HDMIA-RX0+
HDMIA-RX1-
HDMIA-RX1+
HDMIA-RX2-
HDMIA-RX2+
HDMIA-RXC-
HDMIA-RXC+
HDMIB-RX0-
HDMIB-RX0+
HDMIB-RX1-
HDMIB-RX1+
HDMIB-RX2-
HDMIB-RX2+
HDMIB-RXC-
HDMIB-RXC+
HOT-PLUG-A
HOT-PLUG
TH09
TH10
TH11
TH12
TH13
TH14
TH15
TH16
TH01
TH02
TH03
TH04
TH05
TH06
TH07
TH08
9HK0
C18
E19
C15
D15
C16
B18
B17
A17
A16
B16
B15
A19
A18
B14
B13
A13
A12
B12
B11
A15
A14
D19
E15
DDC_SCL_A
DDC_SDA_A
DDC_SCL_B
DDC_SDA_B
HDMI_RREF
P
N
HDMI_RX0_A
HDMI_RX1_A
HDMI_RX2_A
HDMI_RXC_A
HDMI_RX0_B
HDMI_RX1_B
HDMI_RX2_B
HDMI_RXC_B
HOT_PLUG_A
HOT_PLUG_B
DV
CLK
FID
HS
DV_UVIN
DV_VALID
DV_VS
DV_YIN
0
1
2
3
4
5
6
7
8
9
B8
C9
D9
B6
A6
E7
D7
C7
B7
A7
E8
D8
C8
A8
E9
B4
A4
E5
D5
C5
B5
A5
E6
D6
C6
1
2
3
4
5
6
7
A
B
C
D
E

3HK0	B2
7H00-4	A3
9HK0	D2
IHSM	B2
TH01	C2
TH02	C2
TH03	C2
TH04	C2
TH05	C2
TH06	C2
TH07	D2
TH08	D2
TH09	B2
TH10	B2
TH11	B2
TH12	B2
TH13	B2
TH14	C2
TH15	C2
TH16	C2

CHN
SETNAME
CLASS_NO
VIDEO IN
PNX8543 TV543 R2 LDIPNX
8204 000 8927
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid
SUPERS.
16
130 – 8
A3
CHECK
DATE 2007-11-29

18310_510_090302.eps
090302

SSB: PNX8543 - Audio


B041
PNX 8543 : AUDIO
+AUDIO-POWER
3HMF 4R7
IHM6
2HMG 1u0
IHM0
BZX384-C6V8 6HM0
9HM0
7HM5 BC807-25W
3HM0-2 22K
AUDIO-VDD
IHM8
3HM0-1 22K
IHM7
IHM2
3HM0-3 22K
IHM4
7HM6 BC847BW
IHM5
3HM1 10K
3HM0-4 22K
ADAC(1)
IH22
3HMZ 22K
2HM1 1u0
IHN0
7HM2-1 BC847BS(COL)
3HMY 2K2
IHN8
BC857BW 7HM3
IHNG
3HML 2K2
IHM1
+AUDIO-L
2HM3 3n3
2HM4 100n
3HMA 470K
IHNJ
3HMC 22K
ADAC(2)
IH23
3HMV 22K
2HM2 1u0
IHN4
7HM2-2 BC847BS(COL)
3HMW 2K2
IHNF
BC857BW 7HM4
IHNH
3HMU 2K2
IHMG
-AUDIO-R
2HM8 3n3
2HM5 100n
3HMB 470K
IHNK
3HMD 22K
ADAC(7)
IHMW
IHMV
FHR3
2HMJ 100n
7HM1-1 LM324
FHM0
AUDIO-CL-L
3HME-2 10K
3HME-1 10K
2HMP 33p
ADAC(8)
IHN3
IHN6
7HM1-2 LM324
FHM1
AUDIO-CL-R
3HME-3 10K
3HME-4 10K
2HMT 33p
ADAC(5)
IHNB
IHNA
7HM1-3 LM324
FHM2
AUDIO-OUT-L
2HN1 3n3
3HMM-3 10K
3HMM-4 10K
2HMW 33p
ADAC(6)
IHND
IHNE
7HM1-4 LM324
FHM3
AUDIO-OUT-R
2HMY 3n3
3HMM-2 10K
3HMM-1 10K
2HMZ 33p

2HM1	G5
2HM2	H5
2HM3	G4
2HM4	G5
2HM5	H5
2HM8	H4
2HMG	B3
2HMJ	A10
2HMP	C10
2HMT	E10
2HMW	G10
2HMY	H9
2HMZ	I10
2HN1	F9
3HM0-1	C5
3HM0-2	B4
3HM0-3	C4
3HM0-4	D5
3HM1	D4
3HMA	G6
3HMB	H6
3HMC	G5
3HMD	I5
3HME-1	B10
3HME-2	B9
3HME-3	E9
3HME-4	E10
3HMF	B3
3HML	G6
3HMM-1	I10
3HMM-2	I9
3HMM-3	G9
3HMM-4	G10
3HMU	H6
3HMV	H5
3HMW	H5
3HMY	F5
3HMZ	F5
6HM0	B4
7HM1-1	B10
7HM1-2	D10
7HM1-3	F10
7HM1-4	H10
7HM2-1	F5
7HM2-2	H5
7HM3	F7
7HM4	H7
7HM5	B5
7HM6	C5
9HM0	B5
FHM0	B11
FHM1	D11
FHM2	F11
FHM3	H11
FHR3	A10
IH22	F4
IH23	H4
IHM0	B3
IHM1	F7
IHM2	C4
IHM4	C4
IHM5	D5
IHM6	B3
IHM7	C5
IHM8	C5
IHMG	H7
IHMV	B9
IHMW	B9
IHN0	F5
IHN3	D9
IHN4	H5
IHN6	D10
IHN8	F6
IHNA	F10
IHNB	F9
IHND	H9
IHNE	H10
IHNF	H6
IHNG	F6
IHNH	H6
IHNJ	G5
IHNK	I5

CHN	SETNAME			
CLASS_NO	AUDIO PNX8543 TV543 R2 LDIPNX	8204 000 8927	2	2008-11-21
2008-10-10	3			
NAME Maelegheer Ingrid	SUPERS.	16	130 – 9	A2
CHECK	DATE 2007-11-29			

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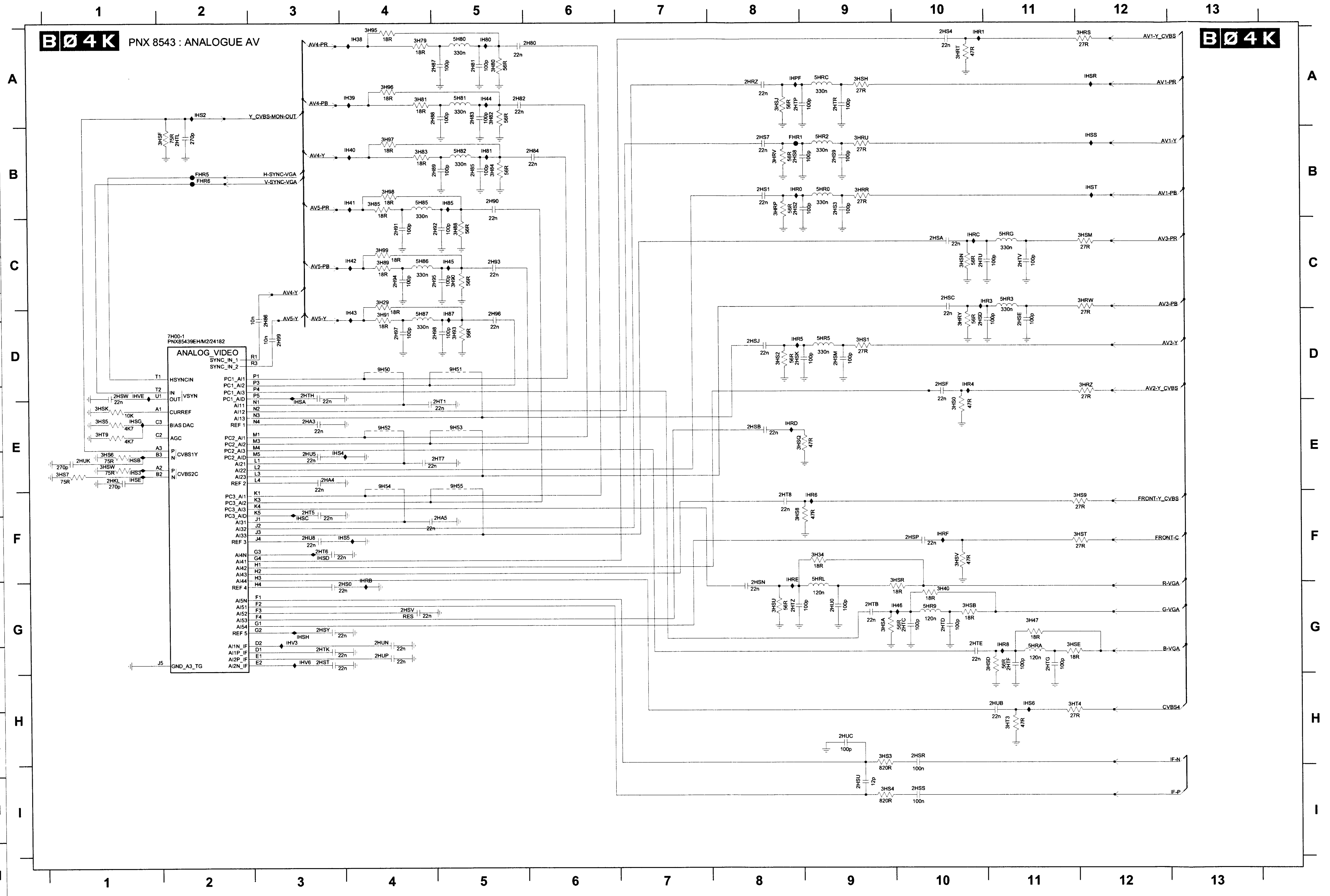
090302

SSB: PNX8543 - Analogue AV

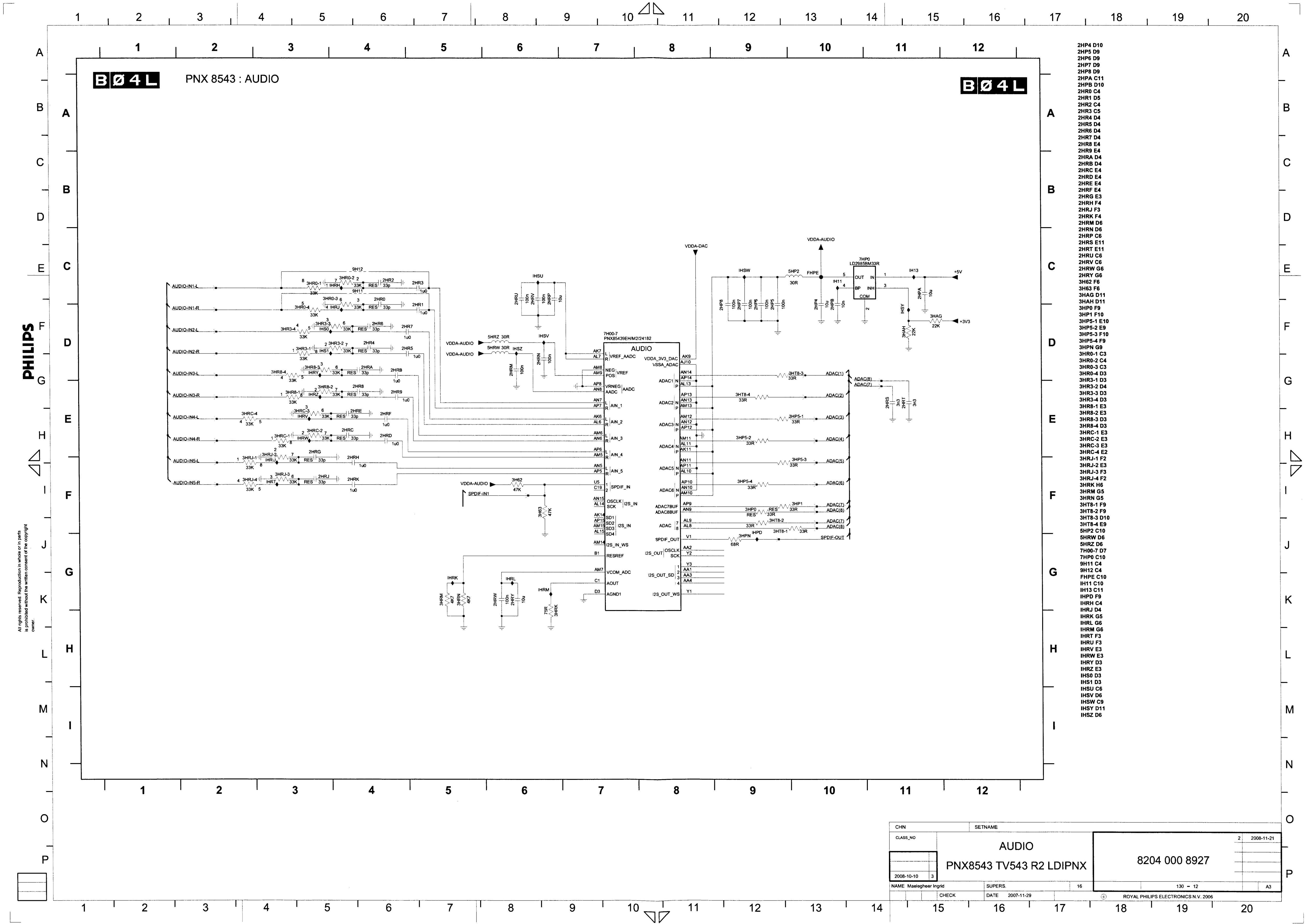

B04K
PNX 8543 : ANALOGUE AV
7H00-1
PNX85439EH/M2/24182
ANALOG_VIDEO
SYNC_IN_1
SYNC_IN_2
HSYNCIN
VSYN
CURREF
BIAS DAC
AGC
CVBS1Y
CVBS2C
GND_A3_TG
AV4-PR
AV4-PB
AV4-Y
AV5-PR
AV5-PB
AV5-Y
Y_CVBS-MON-OUT
H-SYNC-VGA
V-SYNC-VGA
AV1-Y_CVBS
AV1-PR
AV1-Y
AV1-PB
AV3-PR
AV3-PB
AV3-Y
AV2-Y_CVBS
FRONT-Y_CVBS
FRONT-C
R-VGA
G-VGA
B-VGA
CVBS4
IF-N
IF-P
PC1_AI1
PC1_AI2
PC1_AI3
PC1_AID
PC2_AI1
PC2_AI2
PC2_AI3
PC2_AID
PC3_AI1
PC3_AI2
PC3_AI3
PC3_AID
AI1N_IF
AI1P_IF
AI2P_IF
AI2N_IF
REF 1
REF 2
REF 3
REF 4
REF 5
1
2
3
4
5
6
7
8
9
10
11
12
13
A
B
C
D
E
F
G
H
I

2H80	A6
2H81	A5
2H82	A5
2H83	A5
2H84	B6
2H85	B5
2H86	D3
2H87	A5
2H88	A4
2H89	B4
2H90	B5
2H91	C4
2H92	C5
2H93	C5
2H94	C4
2H95	C4
2H96	D5
2H97	D4
2H98	D4
2H99	D3
2HA3	E3
2HA4	E3
2HA5	F5
2HKL	E1
2HRZ	A8
2HS0	G4
2HS1	B8
2HS2	B8
2HS3	B9
2HS4	A10
2HS7	B8
2HS8	B8
2HS9	B9
2HSA	C10
2HSB	E8
2HSC	C10
2HSD	D10
2HSE	D11
2HSF	D10
2HSJ	D8
2HSK	D8
2HSM	D9
2HSN	G8
2HSP	F10
2HSR	H10
2HSS	I10
2HST	G3
2HSU	I9
2HSV	G4
2HSW	D1
2HSY	G3
2HT1	E5
2HT5	F3
2HT6	F3
2HT7	E5
2HT8	F8
2HTB	G9
2HTC	G10
2HTD	G10
2HTE	G10
2HTF	G11
2HTG	G11
2HTH	D3
2HTK	G3
2HTL	B2
2HTP	A8
2HTR	A9
2HTU	C10
2HTV	C11
2HTZ	G8
2HU0	G9
2HU5	E3
2HU8	F3
2HUB	H11
2HUC	H9
2HUK	E1
2HUN	G4
2HUP	G4
3H29	C4
3H34	F9
3H40	G10
3H47	G11
3H79	A4
3H80	A5
3H81	A4
3H82	A5
3H83	B4
3H84	B5
3H85	B4
3H88	C5
3H89	C4
3H90	C5
3H91	D4
3H93	D5
3H95	A4
3H96	A4
3H97	B4
3H98	B4
3H99	C4
3HRP	B8
3HRR	B9
3HRS	A12
3HRT	A10
3HRU	B9
3HRV	B8
3HRW	C12
3HRY	D10
3HRZ	D12
3HS0	E10
3HS1	D9
3HS2	D8
3HS3	H9
3HS4	I9
3HS5	E1
3HS6	E1
3HS7	E1
3HS8	F8
3HS9	F12
3HSA	G9
3HSB	G10
3HSD	G10
3HSE	G11
3HSF	B2
3HSH	A9
3HSJ	A8
3HSK	E1
3HSM	C12
3HSN	C10
3HSQ	E8
3HSR	G10
3HST	F12
3HSU	G8
3HSV	F10
3HSW	E1
3HT3	H11
3HT4	H11
3HT9	E1
5H80	A5
5H81	A5
5H82	B5
5H85	B4
5H86	C4
5H87	D4
5HR0	B9
5HR2	B9
5HR3	C11
5HR5	D9
5HR9	G10
5HRA	G11
5HRC	A9
5HRG	C11
5HRL	F9
7H00-1	D2
9H50	D4
9H51	D5
9H52	E4
9H53	E5
9H54	E4
9H55	E5
FHR1	B8
FHR5	B2
FHR6	B2
IH38	A4
IH39	A4
IH40	B4
IH41	B4
IH42	C4
IH43	D4
IH44	A5
IH45	C5
IH46	G10
IH80	A5
IH81	B5
IH85	B5
IH87	D5
IHPF	A8
IHR0	B8
IHR1	A10
IHR3	C11
IHR4	D10
IHR5	D8
IHR6	F9
IHR8	G11
IHRB	F4
IHRC	C10
IHRD	E8
IHRE	F8
IHRF	F10
IHS2	A2
IHS3	E1
IHS4	E3
IHS5	F4
IHS6	H11
IHSA	E3
IHSB	E1
IHSC	F3
IHSD	F3
IHSE	E1
IHSG	E1
IHSH	G3
IHSR	A12
IHSS	B12
IHST	B12
IHV3	G3
IHV6	G3
IHVE	D1

CHN	SETNAME		
CLASS_NO	ANALOG AV PNX8543 TV543 R2 LDIPNX	8204 000 8927	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 16	130 - 11	A2
CHECK	DATE 2007-11-29	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

PHILIPS

SSB: PNX8543 - Audio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PNX 8543 : AUDIO
B04L
AUDIO-IN1-L
AUDIO-IN1-R
AUDIO-IN2-L
AUDIO-IN2-R
AUDIO-IN3-L
AUDIO-IN3-R
AUDIO-IN4-L
AUDIO-IN4-R
AUDIO-IN5-L
AUDIO-IN5-R
VDDA-AUDIO
VDDA-AUDIO
5HRZ 30R
5HRW 30R
IHSZ
IHSV
IHSU
VDDA-AUDIO
3H62
47K
SPDIF-IN1
3H63
47K
7H00-7
PNX85439EH/M2/24182
AUDIO
VREF_AADC
VREF
AADC
AIN_1
AIN_2
AIN_3
AIN_4
AIN_5
SPDIF_IN
I2S_IN
I2S_IN_WS
RESREF
VCOM_ADC
AOUT
AGND1
VDDA_3V3_DAC
VSSA_ADAC
ADAC1
ADAC2
ADAC3
ADAC4
ADAC5
ADAC6
ADAC7BUF
ADAC8BUF
ADAC
SPDIF_OUT
I2S_OUT
OSCLK
SCK
I2S_OUT_SD
I2S_OUT_WS
VDDA-DAC
IHSW
5HP2
30R
FHPE
VDDA-AUDIO
7HP0
LD2985BM33R
OUT
IN
BP
INH
COM
IH11
IH13
+5V
IHSY
3HAG
22K
3HAH
27K
+3V3
ADAC(1)
ADAC(2)
ADAC(3)
ADAC(4)
ADAC(5)
ADAC(6)
ADAC(7)
ADAC(8)
SPDIF-OUT
IHRK
IHRL
IHRM
3HRM
3HRN
2HRW
2HRY
3HRK
75R

2HP4	D10
2HP5	D9
2HP6	D9
2HP7	D9
2HP8	D9
2HPA	C11
2HPB	D10
2HR0	C4
2HR1	D5
2HR2	C4
2HR3	C5
2HR4	D4
2HR5	D4
2HR6	D4
2HR7	D4
2HR8	E4
2HR9	E4
2HRA	D4
2HRB	D4
2HRC	E4
2HRD	E4
2HRE	E4
2HRF	E4
2HRG	E3
2HRH	F4
2HRJ	F3
2HRK	F4
2HRM	D6
2HRN	D6
2HRP	C6
2HRS	E11
2HRT	E11
2HRU	C6
2HRV	C6
2HRW	G6
2HRY	G6
3H62	F6
3H63	F6
3HAG	D11
3HAH	D11
3HP0	F9
3HP1	F10
3HP5-1	E10
3HP5-2	E9
3HP5-3	F10
3HP5-4	F9
3HPN	G9
3HR0-1	C3
3HR0-2	C4
3HR0-3	C3
3HR0-4	D3
3HR3-1	D3
3HR3-2	D4
3HR3-3	D3
3HR3-4	D3
3HR8-1	E3
3HR8-2	E3
3HR8-3	D3
3HR8-4	D3
3HRC-1	E3
3HRC-2	E3
3HRC-3	E3
3HRC-4	E2
3HRJ-1	F2
3HRJ-2	E3
3HRJ-3	F3
3HRJ-4	F2
3HRK	H6
3HRM	G5
3HRN	G5
3HT8-1	F9
3HT8-2	F9
3HT8-3	D10
3HT8-4	E9
5HP2	C10
5HRW	D6
5HRZ	D6
7H00-7	D7
7HP0	C10
9H11	C4
9H12	C4
FHPE	C10
IH11	C10
IH13	C11
IHPD	F9
IHRH	C4
IHRJ	D4
IHRK	G5
IHRL	G6
IHRM	G6
IHRT	F3
IHRU	F3
IHRV	E3
IHRW	E3
IHRY	D3
IHRZ	E3
IHS0	D3
IHS1	D3
IHSU	C6
IHSV	D6
IHSW	C9
IHSY	D11
IHSZ	D6

CHN	SETNAME			
CLASS_NO	AUDIO PNX8543 TV543 R2 LDIPNX	8204 000 8927	2	2008-11-21
2008-10-10 3				
NAME Maelegheer Ingrid	SUPERS.	16	130 - 12	A3
CHECK	DATE 2007-11-29			

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090302

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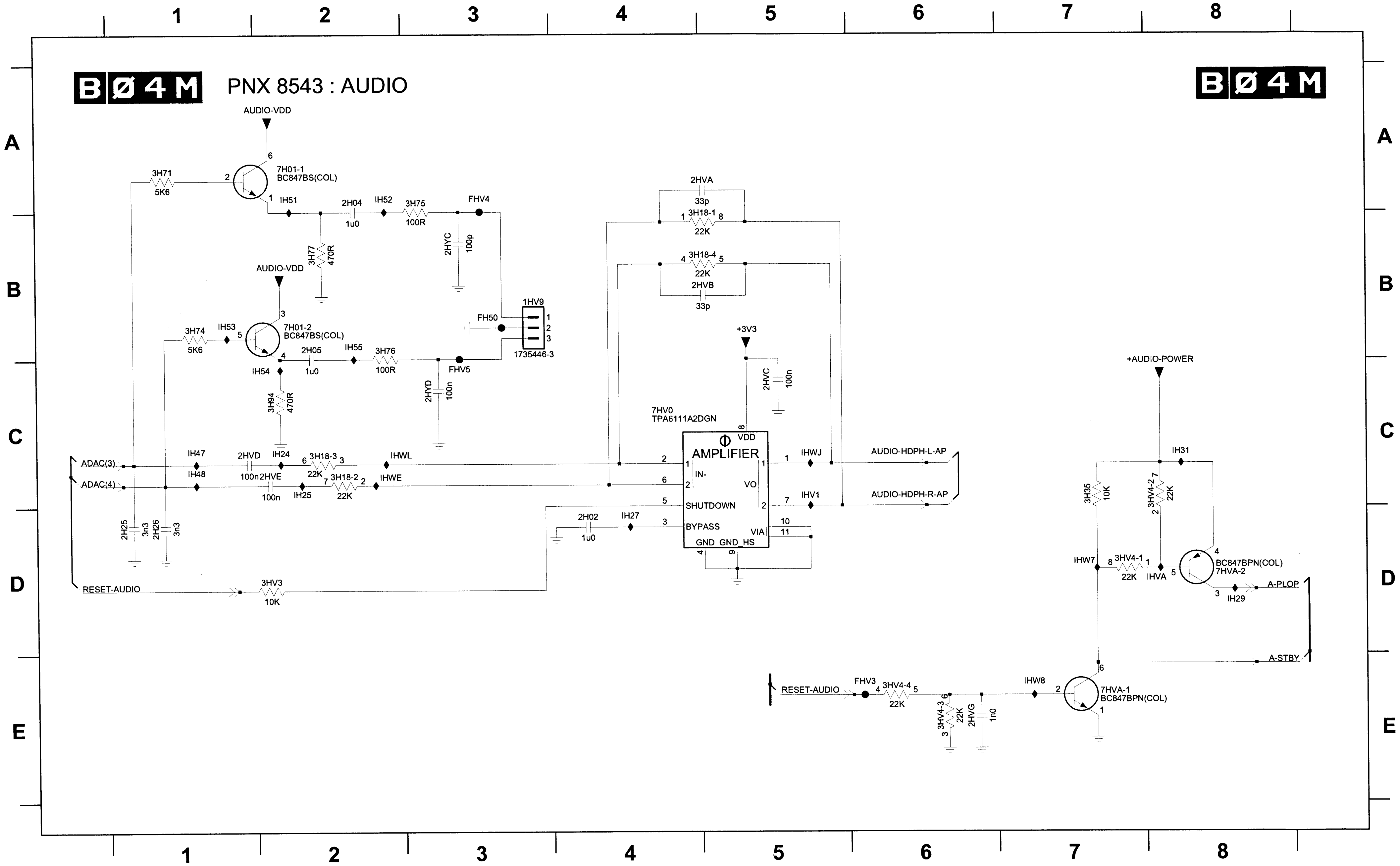
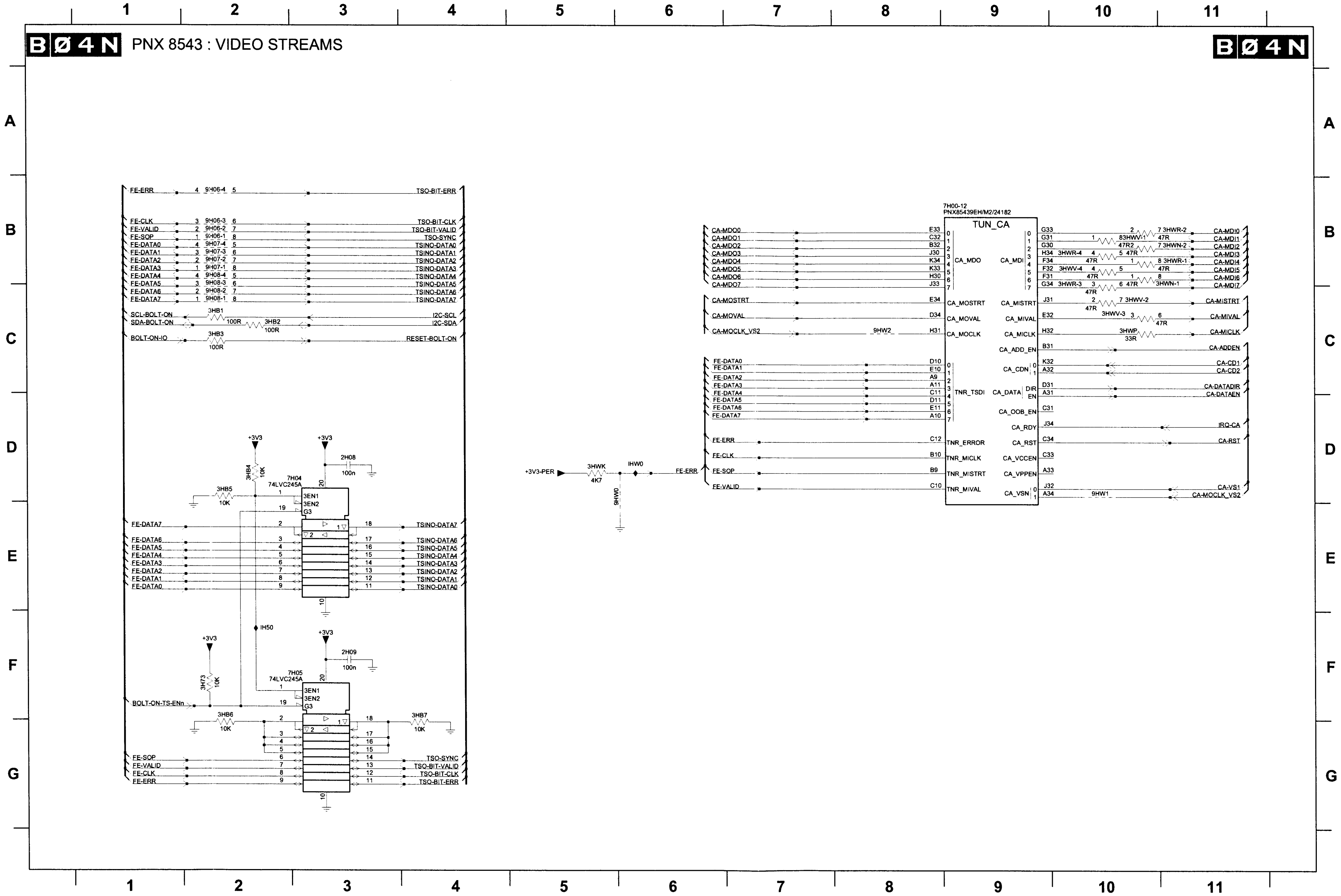

B04M
PNX 8543 : AUDIO
B04M
AUDIO-VDD
3H71
5K6
7H01-1
BC847BS(COL)
IH51
2H04
1u0
IH52
3H75
100R
FHV4
2HYC
100p
3H77
470R
AUDIO-VDD
1HV9
FH50
1735446-3
3H74
5K6
IH53
7H01-2
BC847BS(COL)
2H05
1u0
IH54
IH55
3H76
100R
FHV5
2HYD
100n
3H94
470R
2HVA
33p
3H18-1
22K
3H18-4
22K
2HVB
33p
+3V3
2HVC
100n
7HV0
TPA6111A2DGN
VDD
AMPLIFIER
IN-
VO
SHUTDOWN
BYPASS
VIA
GND GND_HS
IHWJ
IHV1
AUDIO-HDPH-L-AP
AUDIO-HDPH-R-AP
ADAC(3)
ADAC(4)
IH47
IH48
2HVD
100n
2HVE
100n
IH24
IH25
3H18-3
22K
3H18-2
22K
IHWL
IHWE
2H25
3n3
2H26
3n3
2H02
1u0
IH27
RESET-AUDIO
3HV3
10K
+AUDIO-POWER
IH31
3H35
10K
3HV4-2
22K
IHW7
3HV4-1
22K
IHVA
BC847BPN(COL)
7HVA-2
A-PLOP
IH29
A-STBY
RESET-AUDIO
FHV3
3HV4-4
22K
3HV4-3
22K
2HVG
1n0
IHW8
7HVA-1
BC847BPN(COL)
A
B
C
D
E
1
2
3
4
5
6
7
8

1HV9	B3
2H02	D4
2H04	A2
2H05	B2
2H25	D1
2H26	D1
2HVA	A5
2HVB	B5
2HVC	C5
2HVD	C1
2HVE	C2
2HVG	E6
2HYC	B3
2HYD	C3
3H18-1	B5
3H18-2	C2
3H18-3	C2
3H18-4	B5
3H35	C7
3H71	A1
3H74	B1
3H75	A3
3H76	B2
3H77	B2
3H94	C2
3HV3	D2
3HV4-1	D7
3HV4-2	C8
3HV4-3	E6
3HV4-4	E6
7H01-1	A2
7H01-2	B2
7HV0	C4
7HVA-1	E7
7HVA-2	D8
FH50	B3
FHV3	E6
FHV4	A3
FHV5	C3
IH24	C2
IH25	C2
IH27	D4
IH29	D8
IH31	C8
IH47	C1
IH48	C1
IH51	A2
IH52	A2
IH53	B1
IH54	C2
IH55	B2
IHV1	C5
IHVA	D8
IHW7	D7
IHW8	E7
IHWE	C2
IHWJ	C5
IHWL	C2

CHN	SETNAME		
CLASS_NO	AUDIO PNX8543 TV543 R2 LDIPNX	8204 000 8927	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 16	130 - 13	A3
CHECK	DATE 2007-11-29		

18310_514_090302.eps
090302

SSB: PNX8543 - Video Streams

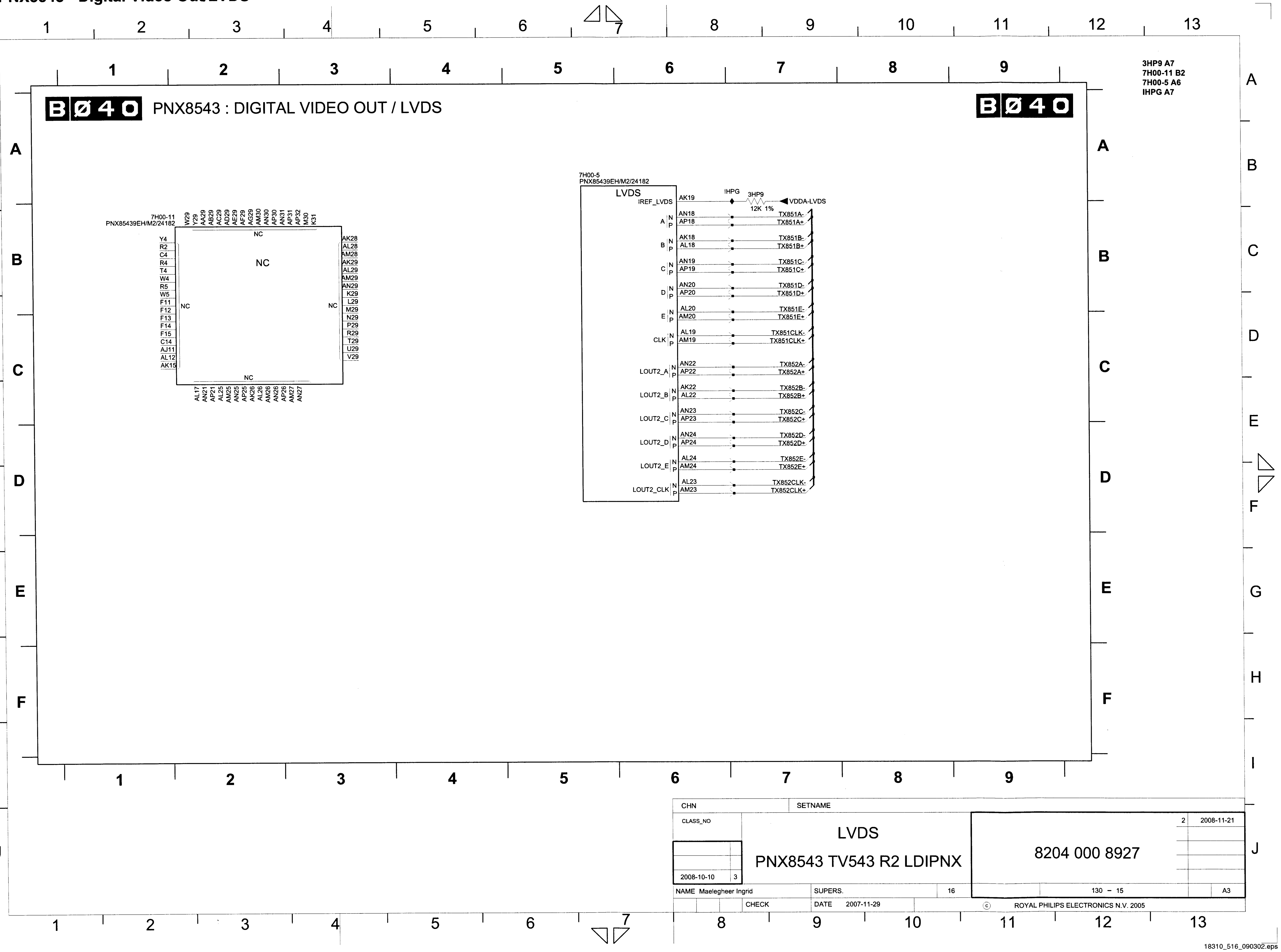

B04N
PNX 8543 : VIDEO STREAMS
B04N
FE-ERR
9H06-4
TSO-BIT-ERR
FE-CLK
FE-VALID
FE-SOP
FE-DATA0
FE-DATA1
FE-DATA2
FE-DATA3
FE-DATA4
FE-DATA5
FE-DATA6
FE-DATA7
9H06-3
9H06-2
9H06-1
9H07-4
9H07-3
9H07-2
9H07-1
9H08-4
9H08-3
9H08-2
9H08-1
TSO-BIT-CLK
TSO-BIT-VALID
TSO-SYNC
TSINO-DATA0
TSINO-DATA1
TSINO-DATA2
TSINO-DATA3
TSINO-DATA4
TSINO-DATA5
TSINO-DATA6
TSINO-DATA7
SCL-BOLT-ON
SDA-BOLT-ON
3HB1
100R
3HB2
100R
I2C-SCL
I2C-SDA
BOLT-ON-IO
3HB3
100R
RESET-BOLT-ON
+3V3
3HB4
10K
2H08
100n
7H04
74LVC245A
3HB5
10K
3EN1
3EN2
G3
IH50
2H09
100n
3H73
10K
7H05
74LVC245A
BOLT-ON-TS-ENn
3HB6
10K
3HB7
10K
+3V3-PER
3HWK
4K7
IHW0
9HW0
7H00-12
PNX85439EH/M2/24182
TUN_CA
CA-MDO0
CA-MDO1
CA-MDO2
CA-MDO3
CA-MDO4
CA-MDO5
CA-MDO6
CA-MDO7
CA_MDO
CA_MDI
CA-MDI0
CA-MDI1
CA-MDI2
CA-MDI3
CA-MDI4
CA-MDI5
CA-MDI6
CA-MDI7
3HWR-2
3HWV-1
3HWN-2
3HWR-4
3HWR-1
3HWV-4
3HWR-3
3HWN-1
47R
CA-MOSTRT
CA_MOSTRT
CA_MISTRT
3HWV-2
CA-MISTRT
CA-MOVAL
CA_MOVAL
CA_MIVAL
3HWV-3
CA-MIVAL
CA-MOCLK_VS2
9HW2
CA_MOCLK
CA_MICLK
3HWP
33R
CA-MICLK
CA_ADD_EN
CA-ADDEN
TNR_TSDI
CA_CDN
CA-CD1
CA-CD2
CA_DATA
DIR
EN
CA-DATADIR
CA-DATAEN
CA_OOB_EN
CA_RDY
IRQ-CA
TNR_ERROR
CA_RST
CA-RST
TNR_MICLK
CA_VCCEN
TNR_MISTRT
CA_VPPEN
TNR_MIVAL
CA_VSN
9HW1
CA-VS1
CA-MOCLK_VS2

2H08	D3
2H09	F3
3H73	F2
3HB1	C2
3HB2	C2
3HB3	C2
3HB4	D2
3HB5	D2
3HB6	F2
3HB7	F4
3HWK	D5
3HWN-1	B11
3HWN-2	B11
3HWP	C10
3HWR-1	B11
3HWR-2	B11
3HWR-3	C10
3HWR-4	B10
3HWV-1	B10
3HWV-2	C10
3HWV-3	C10
3HWV-4	B10
7H00-12	B9
7H04	D3
7H05	F3
9H06-1	B2
9H06-2	B2
9H06-3	B2
9H06-4	B2
9H07-1	B2
9H07-2	B2
9H07-3	B2
9H07-4	B2
9H08-1	C2
9H08-2	C2
9H08-3	C2
9H08-4	B2
9HW0	D6
9HW1	D10
9HW2	C8
IH50	F2
IHW0	D6

CHN	SETNAME				
CLASS_NO	CONDITIONAL ACCESS PNX8543 TV543 R2 LDIPNX		8204 000 8927	2	2008-11-21
2008-10-10	3				
NAME Maelegheer Ingrid	SUPERS.	16	130 - 14		A2
CHECK	DATE 2008-06-05				

18310_515_090302.eps
090302

SSB: PNX8543 - Digital Video Out/LVDS


B040
PNX8543 : DIGITAL VIDEO OUT / LVDS
B040
3HP9 A7
7H00-11 B2
7H00-5 A6
IHPG A7
7H00-11
PNX85439EH/M2/24182
W29
Y29
AA29
AB29
AC29
AD29
AE29
AF29
AG29
AM30
AN30
AP30
AN31
AP31
AP32
M30
K31
NC
Y4
R2
C4
R4
T4
W4
R5
W5
F11
F12
F13
F14
F15
C14
AJ11
AL12
AK15
AK28
AL28
AM28
AK29
AL29
AM29
AN29
K29
L29
M29
N29
P29
R29
T29
U29
V29
AL17
AN21
AP21
AL25
AM25
AN25
AP25
AK26
AL26
AM26
AN26
AP26
AM27
AN27
7H00-5
PNX85439EH/M2/24182
LVDS
IREF_LVDS
AK19
IHPG
3HP9
12K 1%
VDDA-LVDS
A N P AN18 AP18 TX851A- TX851A+
B N P AK18 AL18 TX851B- TX851B+
C N P AN19 AP19 TX851C- TX851C+
D N P AN20 AP20 TX851D- TX851D+
E N P AL20 AM20 TX851E- TX851E+
CLK N P AL19 AM19 TX851CLK- TX851CLK+
LOUT2_A N P AN22 AP22 TX852A- TX852A+
LOUT2_B N P AK22 AL22 TX852B- TX852B+
LOUT2_C N P AN23 AP23 TX852C- TX852C+
LOUT2_D N P AN24 AP24 TX852D- TX852D+
LOUT2_E N P AL24 AM24 TX852E- TX852E+
LOUT2_CLK N P AL23 AM23 TX852CLK- TX852CLK+
CHN
SETNAME
CLASS_NO
LVDS
PNX8543 TV543 R2 LDIPNX
2008-10-10 3
8204 000 8927
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS.
16
130 - 15
A3
CHECK
DATE 2007-11-29
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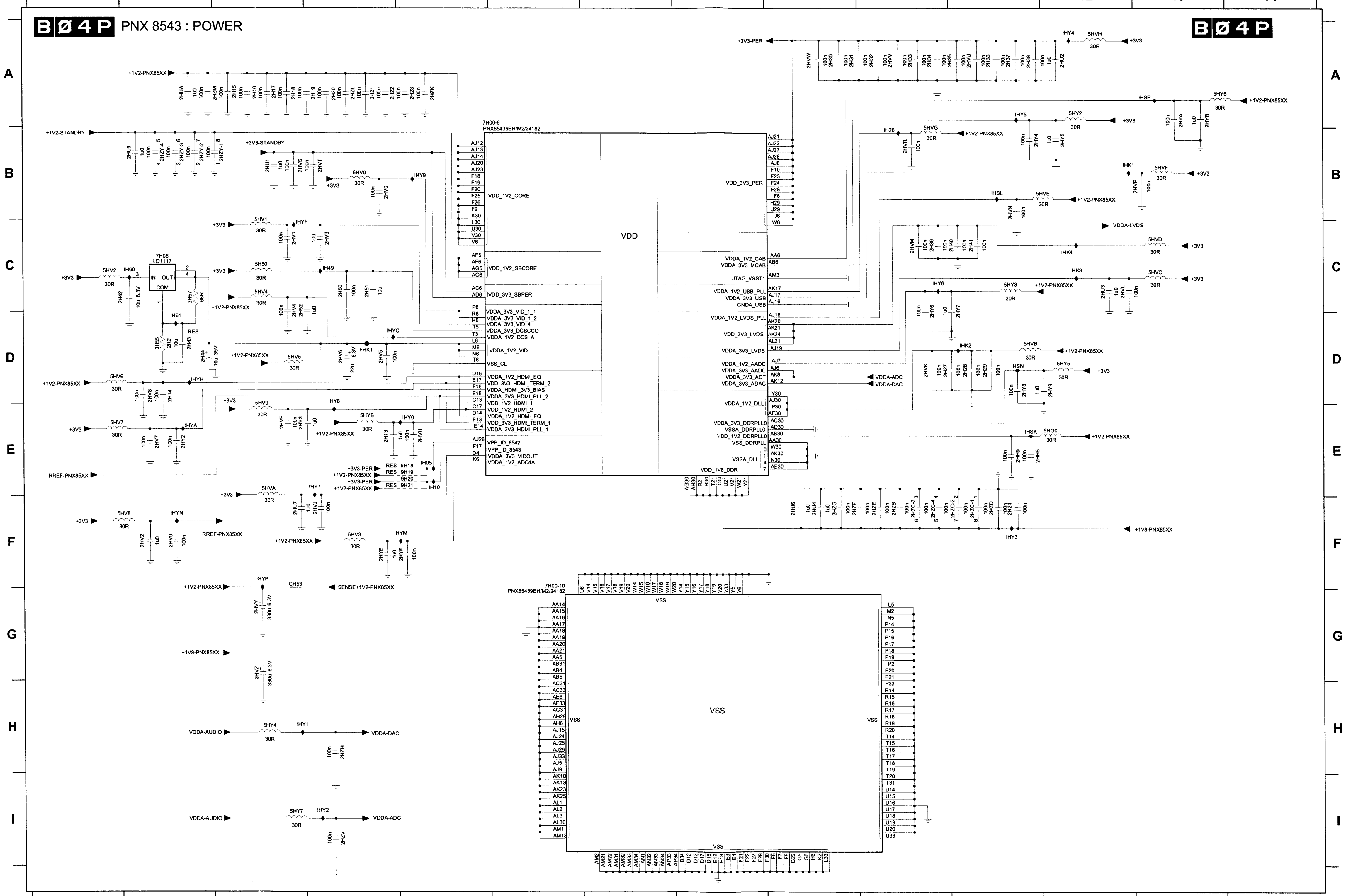
090302

SSB: PNX8543 - Power

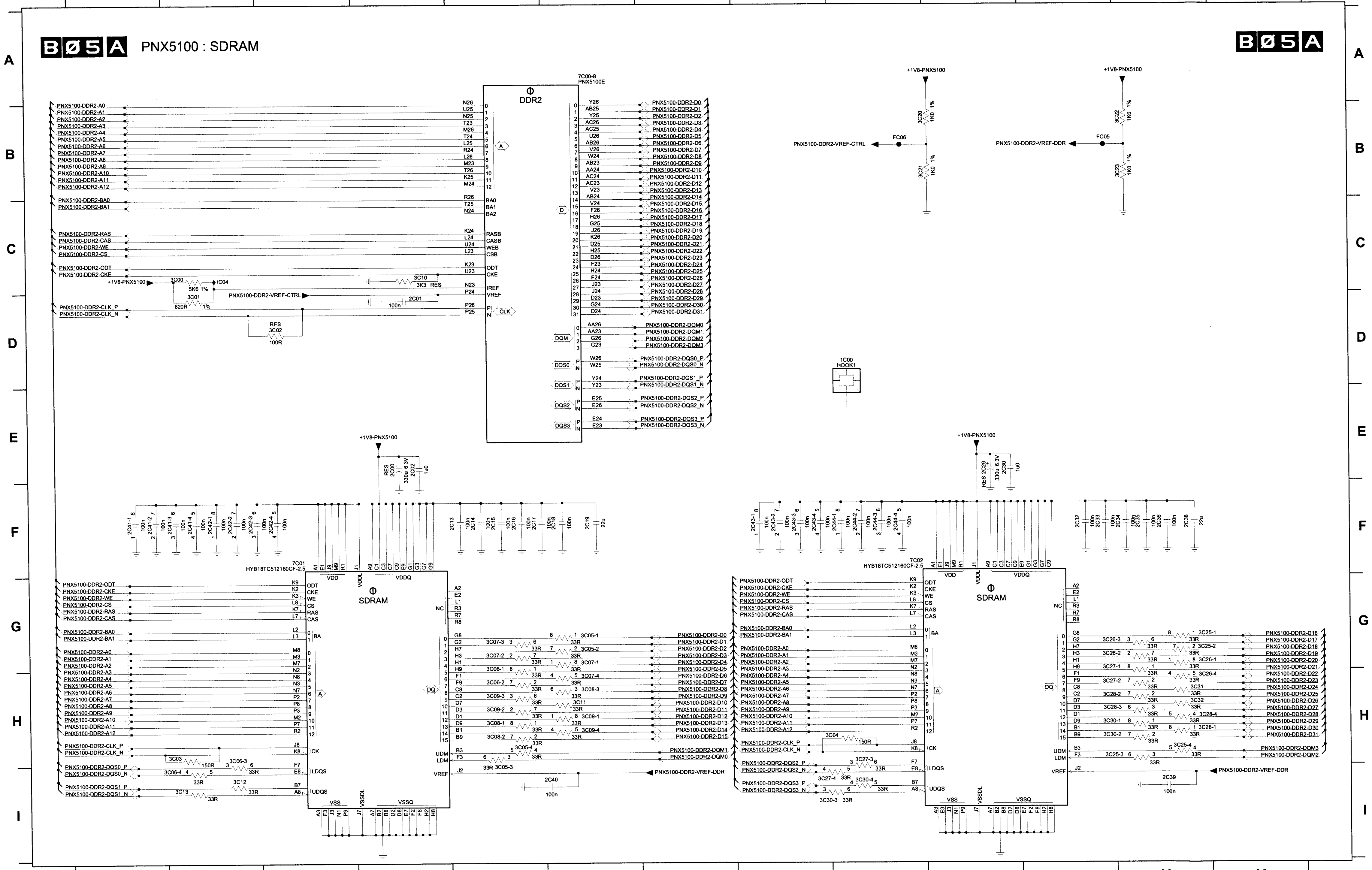

B04P
PNX 8543 : POWER
7H00-9
PNX85439EH/M2/24182
VDD
VDD_1V2_CORE
VDD_1V2_SBCORE
VDD_3V3_SBPER
VDDA_3V3_VID_1_1
VDDA_3V3_VID_1_2
VDDA_3V3_VID_4
VDDA_3V3_DCSCCO
VDDA_1V2_DCS_A
VDDA_1V2_VID
VSS_CL
VDDA_1V2_HDMI_EQ
VDD_3V3_HDMI_TERM_2
VDDA_HDMI_3V3_BIAS
VDDA_3V3_HDMI_PLL_2
VDD_1V2_HDMI_1
VDD_1V2_HDMI_2
VDDA_1V2_HDMI_EQ
VDD_3V3_HDMI_TERM_1
VDDA_3V3_HDMI_PLL_1
VPP_ID_8542
VPP_ID_8543
VDDA_3V3_VIDOUT
VDDA_1V2_ADC4A
VDD_3V3_PER
VDDA_1V2_CAB
VDDA_3V3_MCAB
JTAG_VSST1
VDDA_1V2_USB_PLL
VDDA_3V3_USB
GNDA_USB
VDDA_1V2_LVDS_PLL
VDD_3V3_LVDS
VDDA_3V3_LVDS
VDDA_1V2_AADC
VDDA_3V3_AADC
VDDA_3V3_ACT
VDDA_3V3_ADAC
VDDA_1V2_DLL
VDDA_3V3_DDRPLL0
VSSA_DDRPLL0
VDD_1V2_DDRPLL0
VSS_DDRPLL
VSSA_DLL
VDD_1V8_DDR
7H00-10
PNX85439EH/M2/24182
VSS
7H06
LD1117
IN
OUT
COM
RES
+1V2-PNX85XX
+1V2-STANDBY
+3V3-STANDBY
+3V3
+3V3-PER
+1V8-PNX85XX
RREF-PNX85XX
SENSE+1V2-PNX85XX
VDDA-AUDIO
VDDA-DAC
VDDA-ADC
VDDA-LVDS
CH53
FHK1

2H13	E4
2H14	D2
2H15	A3
2H16	A3
2H17	A3
2H18	A3
2H19	A4
2H20	A4
2H21	A4
2H22	A4
2H23	A5
2H24	F11
2H27	D10
2H28	D11
2H29	D11
2H30	A9
2H31	A9
2H32	A10
2H33	A10
2H34	A10
2H35	A10
2H36	A11
2H37	A11
2H38	A11
2H39	C10
2H40	C11
2H41	C11
2H42	C2
2H43	D2
2H44	D2
2H50	C4
2H51	C4
2H52	C3
2HH6	E11
2HH9	E11
2HU1	B3
2HU2	A12
2HU3	C12
2HU4	F9
2HU6	F9
2HU7	F3
2HU9	B2
2HUA	A2
2HV0	B4
2HV1	C3
2HV2	F2
2HV3	C4
2HV4	C3
2HV5	D4
2HV6	D4
2HV7	E2
2HV8	D2
2HV9	F2
2HVF	E3
2HVH	E5
2HVJ	F4
2HVK	D10
2HVL	C12
2HVM	C10
2HVN	B11
2HVP	B13
2HVR	B10
2HVS	B3
2HVT	B4
2HVU	A11
2HVV	A10
2HVW	A9
2HVY	G3
2HVZ	G3
2HY2	E2
2HY3	E3
2HY4	B11
2HY5	B12
2HY6	C10
2HY7	C11
2HY8	D11
2HY9	D12
2HYA	A13
2HYB	A13
2HYE	F4
2HYF	F5
2HZB	F10
2HZC-1	F11
2HZC-2	F11
2HZC-3	F10
2HZC-4	F10
2HZD	F11
2HZE	F10
2HZF	F9
2HZG	F9
2HZH	H4
2HZK	A5
2HZL	A4
2HZM	A3
2HZV	I4
2HZY-1	B3
2HZY-2	B2
2HZY-3	B2
2HZY-4	B2
3H55	D2
3H57	C2
5H50	C3
5HG0	E12
5HV0	B4
5HV1	C3
5HV2	C1
5HV3	F4
5HV4	C3
5HV5	D3
5HV6	D1
5HV7	E1
5HV8	F2
5HV9	E3
5HVA	E3
5HVB	D11
5HVC	C13
5HVD	C13
5HVE	B12
5HVF	B13
5HVG	B10
5HVH	A12
5HY2	A12
5HY3	C11
5HY4	H3
5HY5	D12
5HY6	A13
5HY7	I3
5HYB	E4
7H00-10	F6
7H00-9	A6
7H06	C2
9H18	E5
9H19	E5
9H20	E5
9H21	E5
CH53	F3
FHK1	D4
IH05	E5
IH10	E5
IH28	B10
IH49	C4
IH60	C2
IH61	D2
IHK1	B12
IHK2	D11
IHK3	C12
IHK4	C12
IHSK	E11
IHSL	B11
IHSN	D11
IHSP	A13
IHY0	E5
IHY1	H3
IHY2	I4
IHY3	F11
IHY4	A12
IHY5	A11
IHY6	C10
IHY7	E4
IHY8	D4
IHY9	B5
IHYA	E2
IHYC	D4
IHYF	C3
IHYH	D2
IHYM	F5
IHYN	F2
IHYP	F3

CHN	SETNAME				
CLASS_NO	POWER PNX8543 TV543 R2 LDIPNX	8204 000 8927	2	2008-11-21	
2008-10-10 3					
NAME Maelegheer Ingrid	SUPERS.	16	130 – 16		A2
CHECK	DATE 2007-11-29				

18310_517_090302.eps
090302

SSB: PNX5100 - SDRAM


B05A
PNX5100 : SDRAM
7C00-8
PNX5100E
DDR2
PNX5100-DDR2-A0 … PNX5100-DDR2-A12
PNX5100-DDR2-BA0
PNX5100-DDR2-BA1
PNX5100-DDR2-RAS
PNX5100-DDR2-CAS
PNX5100-DDR2-WE
PNX5100-DDR2-CS
PNX5100-DDR2-ODT
PNX5100-DDR2-CKE
PNX5100-DDR2-CLK_P
PNX5100-DDR2-CLK_N
PNX5100-DDR2-D0 … PNX5100-DDR2-D31
PNX5100-DDR2-DQM0 … PNX5100-DDR2-DQM3
PNX5100-DDR2-DQS0_P
PNX5100-DDR2-DQS0_N
PNX5100-DDR2-DQS1_P
PNX5100-DDR2-DQS1_N
PNX5100-DDR2-DQS2_P
PNX5100-DDR2-DQS2_N
PNX5100-DDR2-DQS3_P
PNX5100-DDR2-DQS3_N
PNX5100-DDR2-VREF-CTRL
PNX5100-DDR2-VREF-DDR
+1V8-PNX5100
3C00 5K6 1%
3C01 820R 1%
IC04
3C10 3K3 RES
2C01 100n
3C02 RES 100R
FC06
FC05
3C20 1K0 1%
3C21 1K0 1%
3C22 1K0 1%
3C23 1K0 1%
1C00 HOOK1
2C00 RES
2C02 330µ 6.3V
2C29 RES
2C30 330µ 6.3V
7C01
HYB18TC512160CF-2.5
7C02
HYB18TC512160CF-2.5
SDRAM
VDD
VDDQ
VDDL
VSS
VSSQ
VSSDL
ODT
CKE
WE
CS
RAS
CAS
BA
CK
LDQS
UDQS
UDM
LDM
VREF
NC
DQ
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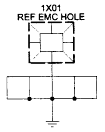
3C03 150R
3C04 150R
3C12 33R
3C13 33R
33R
100n
22u

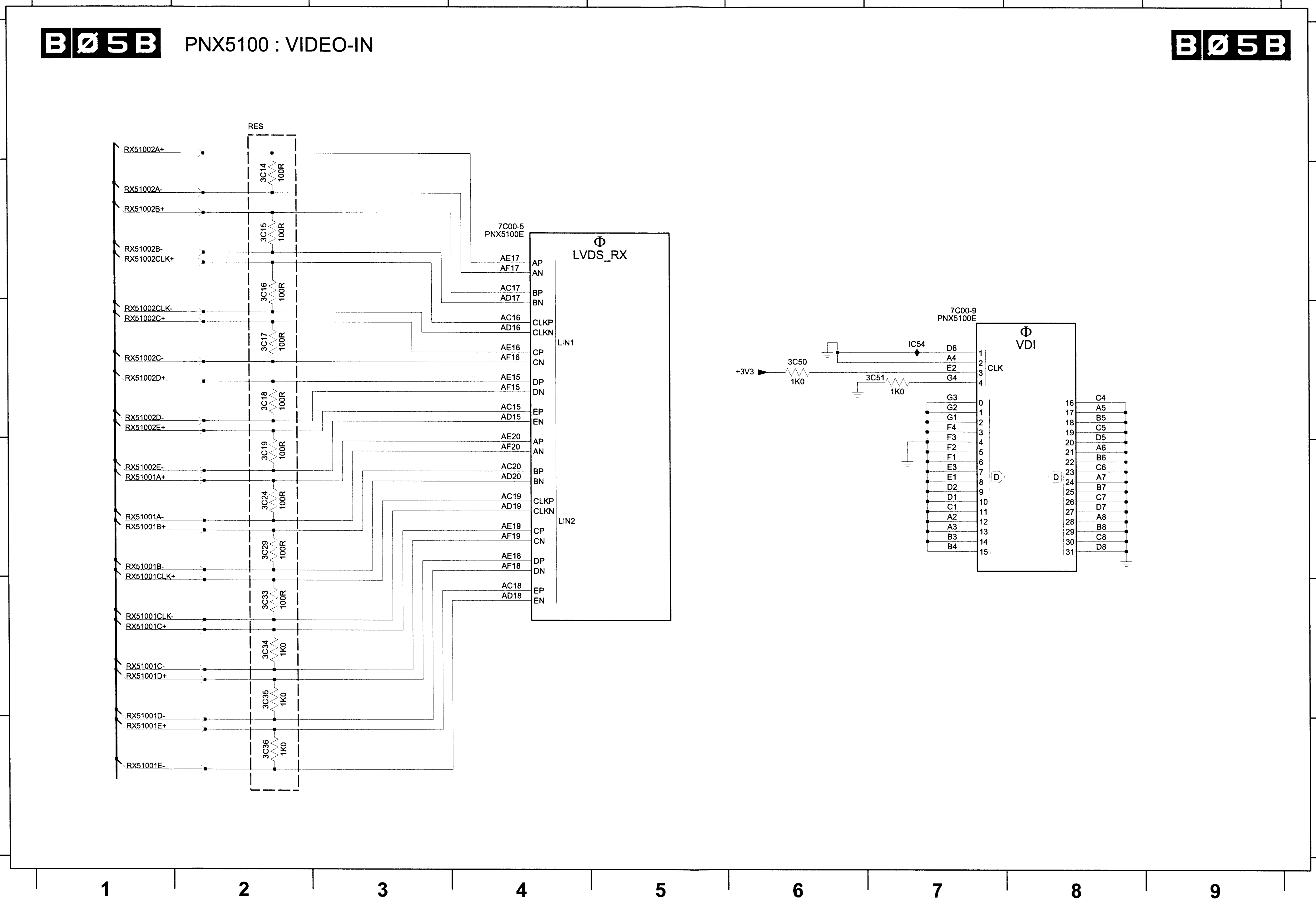

1X01
REF_EMC_HOLE

1C00	D9
2C00	E4
2C01	D4
2C02	E4
2C13	F4
2C14	F5
2C15	F5
2C16	F5
2C17	F5
2C18	F6
2C19	F6
2C29	E10
2C30	E10
2C32	F11
2C33	F11
2C34	F12
2C35	F12
2C36	F12
2C38	F12
2C39	I12
2C40	I6
2C41-1	F1
2C41-2	F1
2C41-3	F2
2C41-4	F2
2C42-1	F2
2C42-2	F2
2C42-3	F2
2C42-4	F3
2C43-1	F8
2C43-2	F8
2C43-3	F8
2C43-4	F8
2C44-1	F9
2C44-2	F9
2C44-3	F9
2C44-4	F9
3C00	C2
3C01	D2
3C02	D3
3C03	H2
3C04	H8
3C05-1	G6
3C05-2	G6
3C05-3	I5
3C05-4	H5
3C06-1	H5
3C06-2	H5
3C06-3	H2
3C06-4	I2
3C07-1	G6
3C07-2	G5
3C07-3	G5
3C07-4	H6
3C08-1	H5
3C08-2	H5
3C08-3	H6
3C09-1	H6
3C09-2	H5
3C09-3	H5
3C09-4	H6
3C10	C4
3C11	H6
3C12	I2
3C13	I2
3C20	B9
3C21	B9
3C22	B12
3C23	B12
3C25-1	G12
3C25-2	G12
3C25-3	H11
3C25-4	H12
3C26-1	G12
3C26-2	G11
3C26-3	G11
3C26-4	H12
3C27-1	H11
3C27-2	H11
3C27-3	H9
3C27-4	I8
3C28-1	H12
3C28-2	H11
3C28-3	H11
3C28-4	H12
3C30-1	H11
3C30-2	H11
3C30-3	I8
3C30-4	I9
3C31	H12
3C32	H12
7C00-8	A6
7C01	F3
7C02	F9
FC05	B11
FC06	B9
IC04	C2

CHN
SETNAME
CLASS_NO
DDR2 PNX5100
TV543 R2 LDIPNX
8204 000 8928
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid
SUPERS. 9
130 - 1
A2
CHECK
DATE

18310_518_090302.eps
090302

SSB: PNX5100 - Video-In

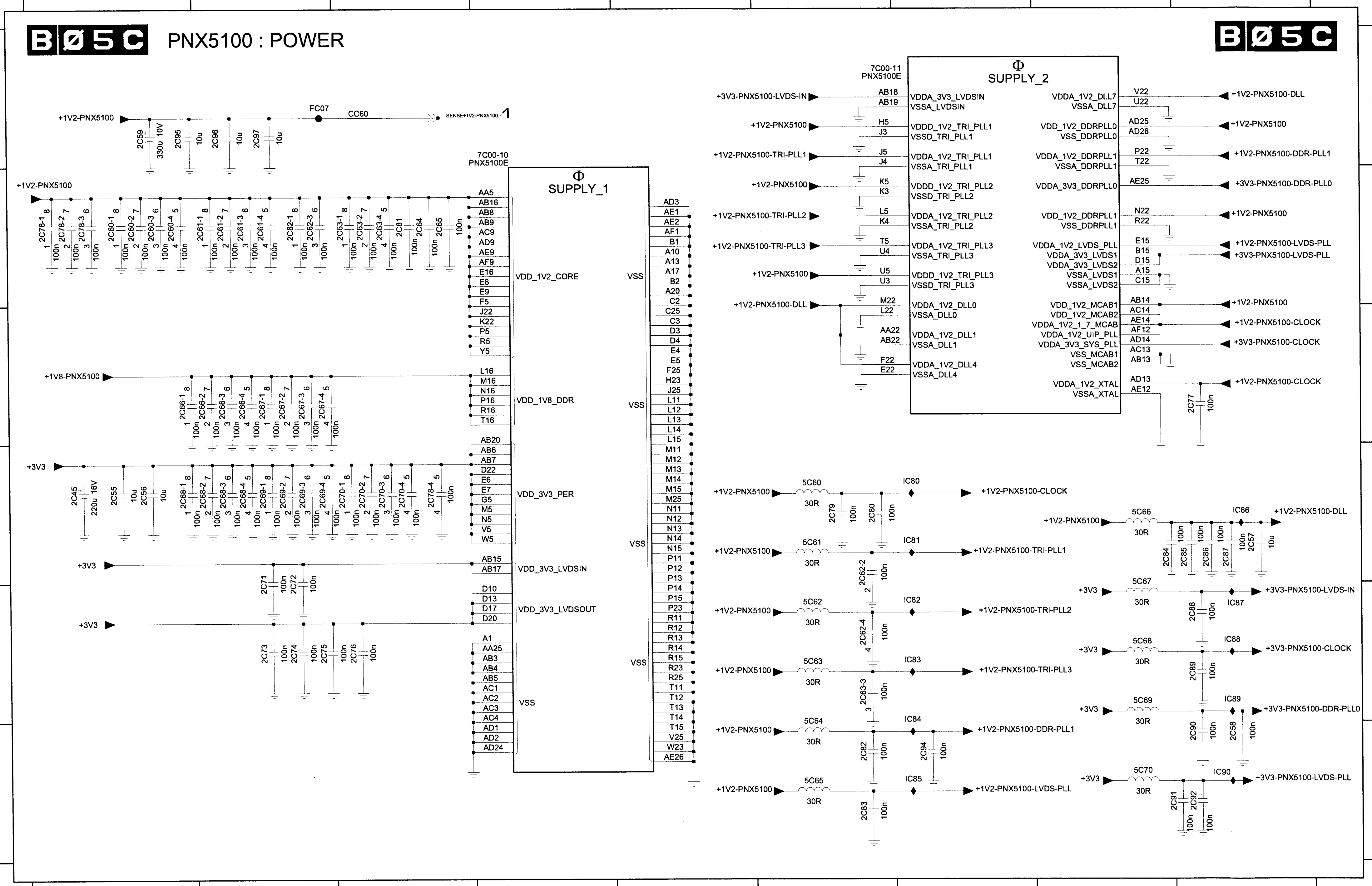

B05B
PNX5100 : VIDEO-IN
B05B
RES
RX51002A+
RX51002A-
RX51002B+
RX51002B-
RX51002CLK+
RX51002CLK-
RX51002C+
RX51002C-
RX51002D+
RX51002D-
RX51002E+
RX51002E-
RX51001A+
RX51001A-
RX51001B+
RX51001B-
RX51001CLK+
RX51001CLK-
RX51001C+
RX51001C-
RX51001D+
RX51001D-
RX51001E+
RX51001E-
3C14 100R
3C15 100R
3C16 100R
3C17 100R
3C18 100R
3C19 100R
3C24 100R
3C29 100R
3C33 100R
3C34 1K0
3C35 1K0
3C36 1K0
7C00-5
PNX5100E
Φ
LVDS_RX
AE17 AP
AF17 AN
AC17 BP
AD17 BN
AC16 CLKP
AD16 CLKN
AE16 CP
AF16 CN
AE15 DP
AF15 DN
AC15 EP
AD15 EN
LIN1
AE20 AP
AF20 AN
AC20 BP
AD20 BN
AC19 CLKP
AD19 CLKN
AE19 CP
AF19 CN
AE18 DP
AF18 DN
AC18 EP
AD18 EN
LIN2
7C00-9
PNX5100E
Φ
VDI
IC54
+3V3
3C50 1K0
3C51 1K0
D6 1
A4 2
E2 3
G4 4
CLK
G3 0
G2 1
G1 2
F4 3
F3 4
F2 5
F1 6
E3 7
E1 8
D2 9
D1 10
C1 11
A2 12
A3 13
B3 14
B4 15
D
D
16 C4
17 A5
18 B5
19 C5
20 D5
21 A6
22 B6
23 C6
24 A7
25 B7
26 C7
27 D7
28 A8
29 B8
30 C8
31 D8
1 2 3 4 5 6 7 8 9
A B C D E F

3C14	B2
3C15	B2
3C16	B2
3C17	C2
3C18	C2
3C19	D2
3C24	D2
3C29	D2
3C33	E2
3C34	E2
3C35	E2
3C36	F2
3C50	C6
3C51	C7
7C00-5	B4
7C00-9	C7
IC54	C7

CHN
SETNAME
CLASS_NO
2008-10-10 3
VIDEO PNX5100
TV543 R2 LDIPNX
8204 000 8928
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 9
130 - 2
A3
CHECK
DATE

18310_519_090302.eps
090302

SSB: PNX5100 - Power


B05C
PNX5100 : POWER
B05C
+1V2-PNX5100
FC07
CC60
SENSE+1V2-PNX5100
1
2C59 330u 10V
2C95 10u
2C96 10u
2C97 10u
7C00-10
PNX5100E
Φ
SUPPLY_1
+1V2-PNX5100
2C78-1 2C78-2 2C78-3
2C60-1 2C60-2 2C60-3 2C60-4
2C61-1 2C61-2 2C61-3 2C61-4
2C62-1 2C62-3
2C63-1 2C63-2 2C63-4
2C81 2C64 2C65
100n
AA5 AB16 AB8 AB9 AC9 AD9 AE9 AF9 E16 E8 E9 F5 J22 K22 P5 R5 Y5
VDD_1V2_CORE
+1V8-PNX5100
2C66-1 2C66-2 2C66-3 2C66-4 2C67-1 2C67-2 2C67-3 2C67-4
L16 M16 N16 P16 R16 T16
VDD_1V8_DDR
+3V3
2C45 220u 16V
2C55 10u
2C56 10u
2C68-1 2C68-2 2C68-3 2C68-4 2C69-1 2C69-2 2C69-3 2C69-4 2C70-1 2C70-2 2C70-3 2C70-4 2C78-4
AB20 AB6 AB7 D22 E6 E7 G5 M5 N5 V5 W5
VDD_3V3_PER
+3V3
2C71 100n 2C72 100n
AB15 AB17
VDD_3V3_LVDSIN
+3V3
2C73 100n 2C74 100n 2C75 100n 2C76 100n
D10 D13 D17 D20
VDD_3V3_LVDSOUT
A1 AA25 AB3 AB4 AB5 AC1 AC2 AC3 AC4 AD1 AD2 AD24
VSS
VSS
AD3 AE1 AE2 AF1 B1 A10 A13 A17 B2 A20 C2 C25 C3 D3 D4 E4 E5 F25 H23 J25 L11 L12 L13 L14 L15 M11 M12 M13 M14 M15 M25 N11 N12 N13 N14 N15 P11 P12 P13 P14 P15 P23 R11 R12 R13 R14 R15 R23 R25 T11 T12 T13 T14 T15 V25 W23 AE26
7C00-11
PNX5100E
Φ
SUPPLY_2
+3V3-PNX5100-LVDS-IN
AB18 VDDA_3V3_LVDSIN
AB19 VSSA_LVDSIN
+1V2-PNX5100
H5 VDDD_1V2_TRI_PLL1
J3 VSSD_TRI_PLL1
+1V2-PNX5100-TRI-PLL1
J5 VDDA_1V2_TRI_PLL1
J4 VSSA_TRI_PLL1
+1V2-PNX5100
K5 VDDD_1V2_TRI_PLL2
K3 VSSD_TRI_PLL2
+1V2-PNX5100-TRI-PLL2
L5 VDDA_1V2_TRI_PLL2
K4 VSSA_TRI_PLL2
+1V2-PNX5100-TRI-PLL3
T5 VDDA_1V2_TRI_PLL3
U4 VSSA_TRI_PLL3
+1V2-PNX5100
U5 VDDD_1V2_TRI_PLL3
U3 VSSD_TRI_PLL3
+1V2-PNX5100-DLL
M22 VDDA_1V2_DLL0
L22 VSSA_DLL0
AA22 VDDA_1V2_DLL1
AB22 VSSA_DLL1
F22 VDDA_1V2_DLL4
E22 VSSA_DLL4
VDDA_1V2_DLL7 V22
VSSA_DLL7 U22
+1V2-PNX5100-DLL
VDD_1V2_DDRPLL0 AD25
VSS_DDRPLL0 AD26
+1V2-PNX5100
VDDA_1V2_DDRPLL1 P22
VSSA_DDRPLL1 T22
+1V2-PNX5100-DDR-PLL1
VDDA_3V3_DDRPLL0 AE25
+3V3-PNX5100-DDR-PLL0
VDD_1V2_DDRPLL1 N22
VSS_DDRPLL1 R22
+1V2-PNX5100
VDDA_1V2_LVDS_PLL E15
VDDA_3V3_LVDS1 B15
VDDA_3V3_LVDS2 D15
VSSA_LVDS1 A15
VSSA_LVDS2 C15
+1V2-PNX5100-LVDS-PLL
+3V3-PNX5100-LVDS-PLL
VDD_1V2_MCAB1 AB14
VDD_1V2_MCAB2 AC14
VDDA_1V2_1_7_MCAB AE14
VDDA_1V2_UIP_PLL AF12
VDDA_3V3_SYS_PLL AD14
VSS_MCAB1 AC13
VSS_MCAB2 AB13
+1V2-PNX5100
+1V2-PNX5100-CLOCK
+3V3-PNX5100-CLOCK
VDDA_1V2_XTAL AD13
VSSA_XTAL AE12
+1V2-PNX5100-CLOCK
2C77 100n
+1V2-PNX5100 5C60 30R 2C79 100n 2C80 100n IC80 +1V2-PNX5100-CLOCK
+1V2-PNX5100 5C61 30R 2C62-2 100n IC81 +1V2-PNX5100-TRI-PLL1
+1V2-PNX5100 5C62 30R 2C62-4 100n IC82 +1V2-PNX5100-TRI-PLL2
+1V2-PNX5100 5C63 30R 2C63-3 100n IC83 +1V2-PNX5100-TRI-PLL3
+1V2-PNX5100 5C64 30R 2C82 100n IC84 2C94 100n +1V2-PNX5100-DDR-PLL1
+1V2-PNX5100 5C65 30R 2C83 100n IC85 +1V2-PNX5100-LVDS-PLL
+1V2-PNX5100 5C66 30R 2C84 100n 2C85 100n 2C86 100n 2C87 100n 2C57 10u IC86 +1V2-PNX5100-DLL
+3V3 5C67 30R 2C88 100n IC87 +3V3-PNX5100-LVDS-IN
+3V3 5C68 30R 2C89 100n IC88 +3V3-PNX5100-CLOCK
+3V3 5C69 30R 2C90 100n IC89 2C58 100n +3V3-PNX5100-DDR-PLL0
+3V3 5C70 30R 2C91 100n 2C92 100n IC90 +3V3-PNX5100-LVDS-PLL
A B C D E F
1 2 3 4 5 6 7 8 9

2C45	D1
2C55	D1
2C56	D1
2C57	D9
2C58	F9
2C59	A1
2C60-1	B1
2C60-2	B1
2C60-3	B1
2C60-4	B1
2C61-1	B2
2C61-2	B2
2C61-3	B2
2C61-4	B2
2C62-1	B2
2C62-2	D6
2C62-3	B2
2C62-4	E6
2C63-1	B3
2C63-2	B3
2C63-3	E6
2C63-4	B3
2C64	B3
2C65	B3
2C66-1	C1
2C66-2	C2
2C66-3	C2
2C66-4	C2
2C67-1	C2
2C67-2	C2
2C67-3	C2
2C67-4	C2
2C68-1	D1
2C68-2	D2
2C68-3	D2
2C68-4	D2
2C69-1	D2
2C69-2	D2
2C69-3	D2
2C69-4	D2
2C70-1	D3
2C70-2	D3
2C70-3	D3
2C70-4	D3
2C71	E2
2C72	E2
2C73	E2
2C74	E2
2C75	E2
2C76	E3
2C77	C9
2C78-1	B1
2C78-2	B1
2C78-3	B1
2C78-4	D3
2C79	D6
2C80	D6
2C81	B3
2C82	F6
2C83	F6
2C84	D8
2C85	D9
2C86	D9
2C87	D9
2C88	E9
2C89	E9
2C90	F9
2C91	F8
2C92	F9
2C94	F7
2C95	A1
2C96	A2
2C97	A2
5C60	D6
5C61	D6
5C62	E6
5C63	E6
5C64	F6
5C65	F6
5C66	D8
5C67	E8
5C68	E8
5C69	E8
5C70	F8
7C00-10	A4
7C00-11	A7
CC60	A3
FC07	A2
IC80	D7
IC81	D7
IC82	E7
IC83	E7
IC84	E7
IC85	F7
IC86	D9
IC87	E9
IC88	E9
IC89	E9
IC90	F9

PHILIPS

CHN
SETNAME
CLASS_NO
SUPPLY PNX5100
TV543 R2 LDIPNX
2008-10-10 3
8204 000 8928
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 9
130 - 3
A3
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DATE

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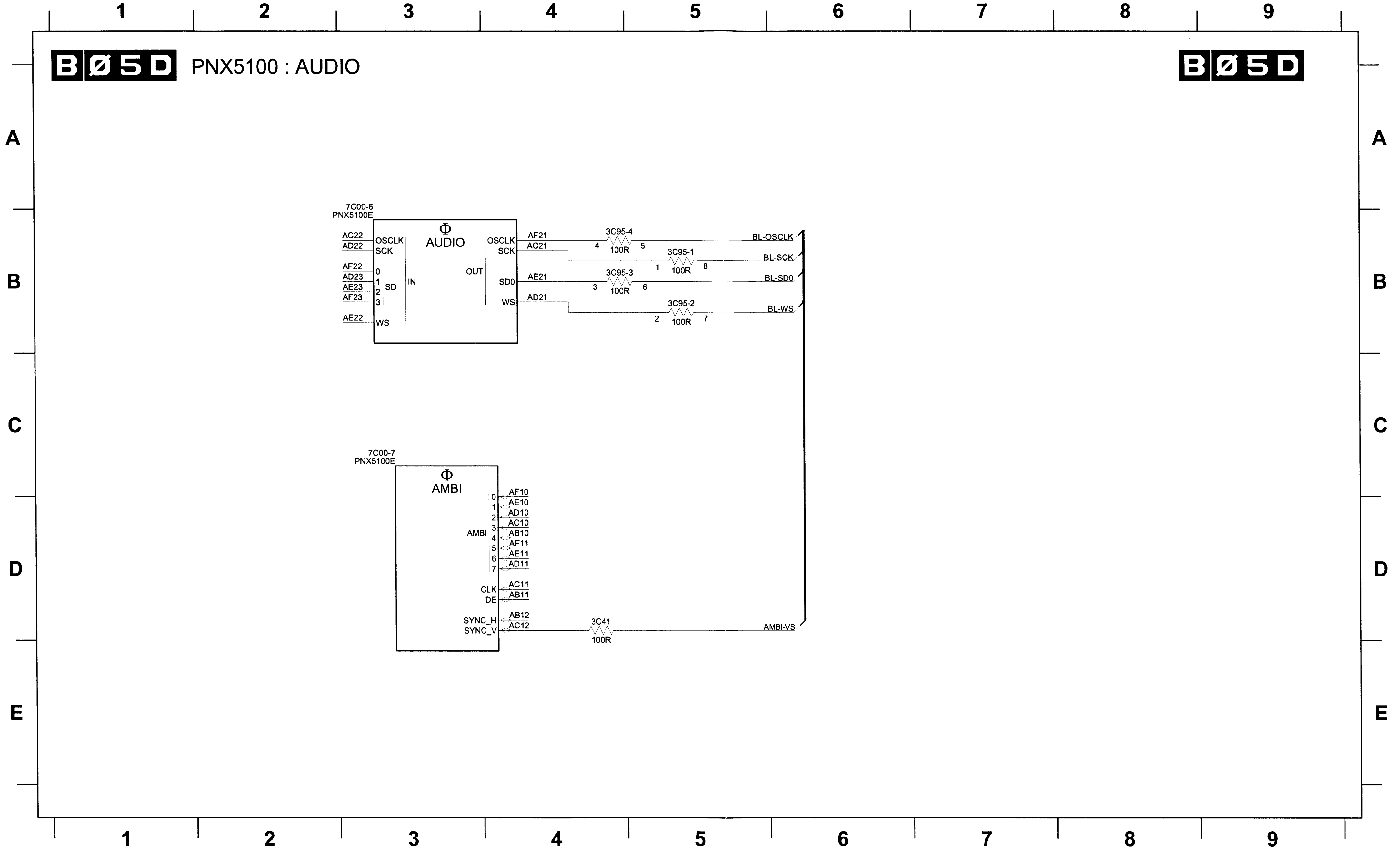
SSB: PNX5100 - Audio

3C41 D4
3C95-1 B5
3C95-2 B5
3C95-3 B4
3C95-4 B4
7C00-6 B3
7C00-7 C3


B05D
PNX5100 : AUDIO
B05D
7C00-6
PNX5100E
AUDIO
AC22
AD22
OSCLK
SCK
AF22
AD23
AE23
AF23
0
1
2
3
SD
IN
AE22
WS
OUT
OSCLK
SCK
SD0
WS
AF21
AC21
AE21
AD21
3C95-4
4
100R
5
3C95-1
1
100R
8
3C95-3
3
100R
6
3C95-2
2
100R
7
BL-OSCLK
BL-SCK
BL-SD0
BL-WS
7C00-7
PNX5100E
AMBI
AMBI
0
1
2
3
4
5
6
7
AF10
AE10
AD10
AC10
AB10
AF11
AE11
AD11
CLK
DE
AC11
AB11
SYNC_H
SYNC_V
AB12
AC12
3C41
100R
AMBI-VS
A
B
C
D
E
1
2
3
4
5
6
7
8
9

CHN	SETNAME		
CLASS_NO	AUDIO PNX5100 TV543 R2 LDIPNX	8204 000 8928	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 9	130 - 4	A3
CHECK	DATE		

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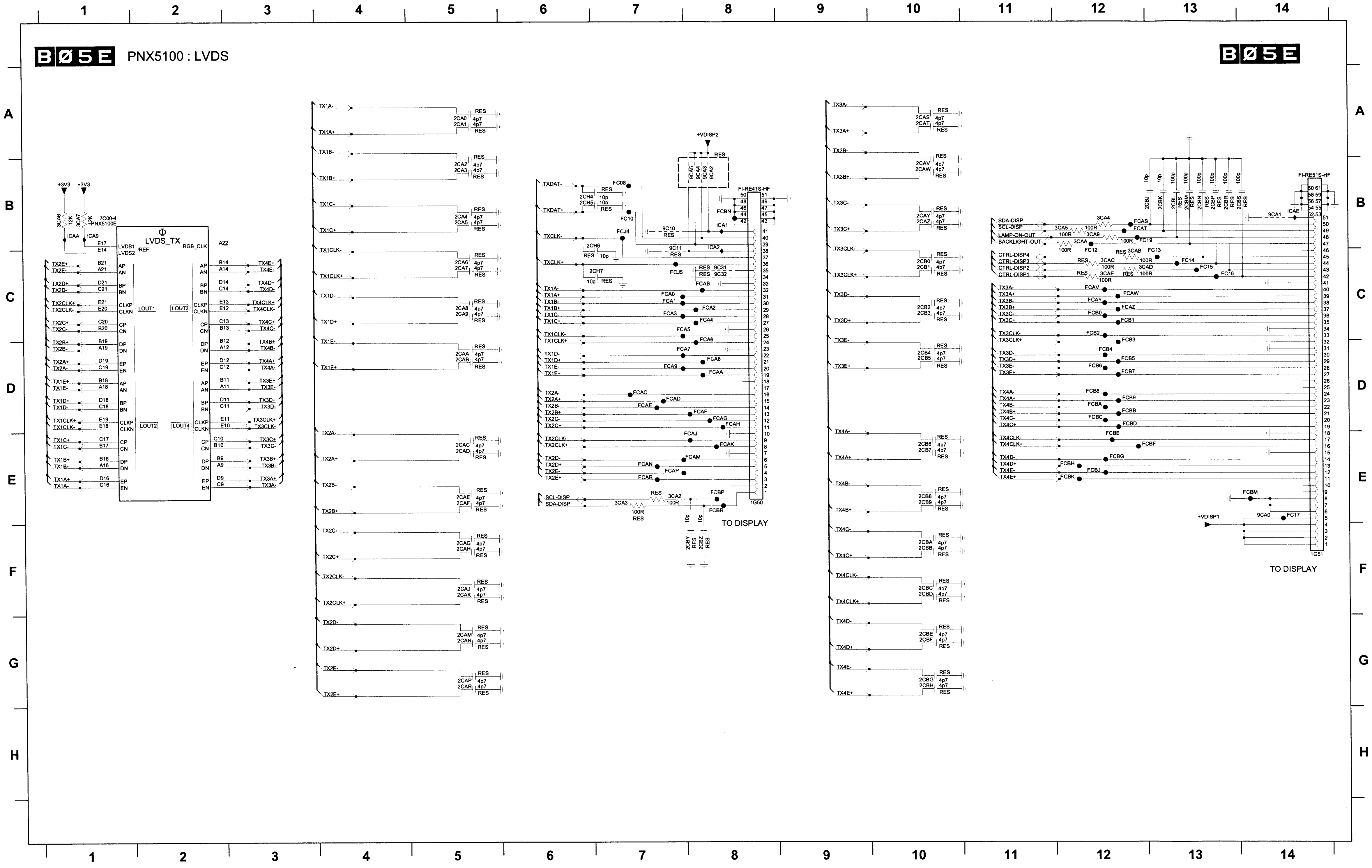
SSB: PNX5100 - LVDS



1G50	E8
1G51	F14
2CA0	A5
2CA1	A5
2CA2	B5
2CA3	B5
2CA4	B5
2CA5	B5
2CA6	C5
2CA7	C5
2CA8	C5
2CA9	C5
2CAA	D5
2CAB	D5
2CAC	E5
2CAD	E5
2CAE	E5
2CAF	E5
2CAG	F5
2CAH	F5
2CAJ	F5
2CAK	F5
2CAM	G5
2CAN	G5
2CAP	G5
2CAR	G5
2CAS	A10
2CAT	A10
2CAV	B10
2CAW	B10
2CAY	B10
2CAZ	B10
2CB0	C10
2CB1	C10
2CB2	C10
2CB3	C10
2CB4	D10
2CB5	D10
2CB6	E10
2CB7	E10
2CB8	E10
2CB9	E10
2CBA	F10
2CBB	F10
2CBC	F10
2CBD	F10
2CBE	G10
2CBF	G10
2CBG	G10
2CBH	G10
2CBJ	B13
2CBK	B13
2CBL	B13
2CBM	B13
2CBN	B13
2CBP	B13
2CBR	B13
2CBS	B14
2CBY	F8
2CBZ	F8
2CH4	B6
2CH5	B6
2CH6	B7
2CH7	C7
3CA2	E7
3CA3	E7
3CA4	B12
3CA5	B12
3CA6	B1
3CA7	B1
3CA9	B12
3CAA	B12
3CAB	C12
3CAC	C12
3CAD	C12
3CAE	C12
7C00-4	B1
9C10	B7
9C11	C7
9C31	C8
9C32	C8
9CA0	E14
9CA1	B14
9CA2	B8
9CA3	B8
9CA4	B8
9CA5	B8
FC08	B7
FC10	B7
FC12	C12
FC13	C13
FC14	C13
FC15	C13
FC16	C13
FC17	E14
FC19	B12
FCA0	C7
FCA1	C7
FCA2	C8
FCA3	C7
FCA4	C8
FCA5	C7
FCA6	D8
FCA7	D7
FCA8	D8
FCA9	D7
FCAA	D8
FCAB	C8
FCAC	D7
FCAD	D7
FCAE	D7
FCAF	D8
FCAG	D8
FCAH	D8
FCAJ	E8
FCAK	E8
FCAM	E8
FCAN	E7
FCAP	E7
FCAR	E7
FCAS	B12
FCAT	B12
FCAV	C12
FCAW	C12
FCAY	C12
FCAZ	C12
FCB0	C12
FCB1	C12
FCB2	C12
FCB3	D12
FCB4	D12
FCB5	D12
FCB6	D12
FCB7	D12
FCB8	D12
FCB9	D12
FCBA	D12
FCBB	D12
FCBC	D12
FCBD	D12
FCBE	E12
FCBF	E13
FCBG	E12
FCBH	E12
FCBJ	E12
FCBK	E12
FCBM	E14
FCBN	B8
FCBP	E8
FCBR	E8
FCJ4	B7
FCJ5	C7
ICA1	B8
ICA2	B8
ICA9	B1
ICAA	B1
ICAE	B14

CHN	SETNAME			
CLASS_NO	LVDS PNX5100 TV543 R2 LDIPNX	8204 000 8928	2	2008-11-21
2008-10-10 3				
NAME Maelegheer Ingrid	SUPERS. 9	130 – 5		A2
CHECK	DATE	ⓒ ROYAL PHILIPS ELECTRONICS N.V. 2008		

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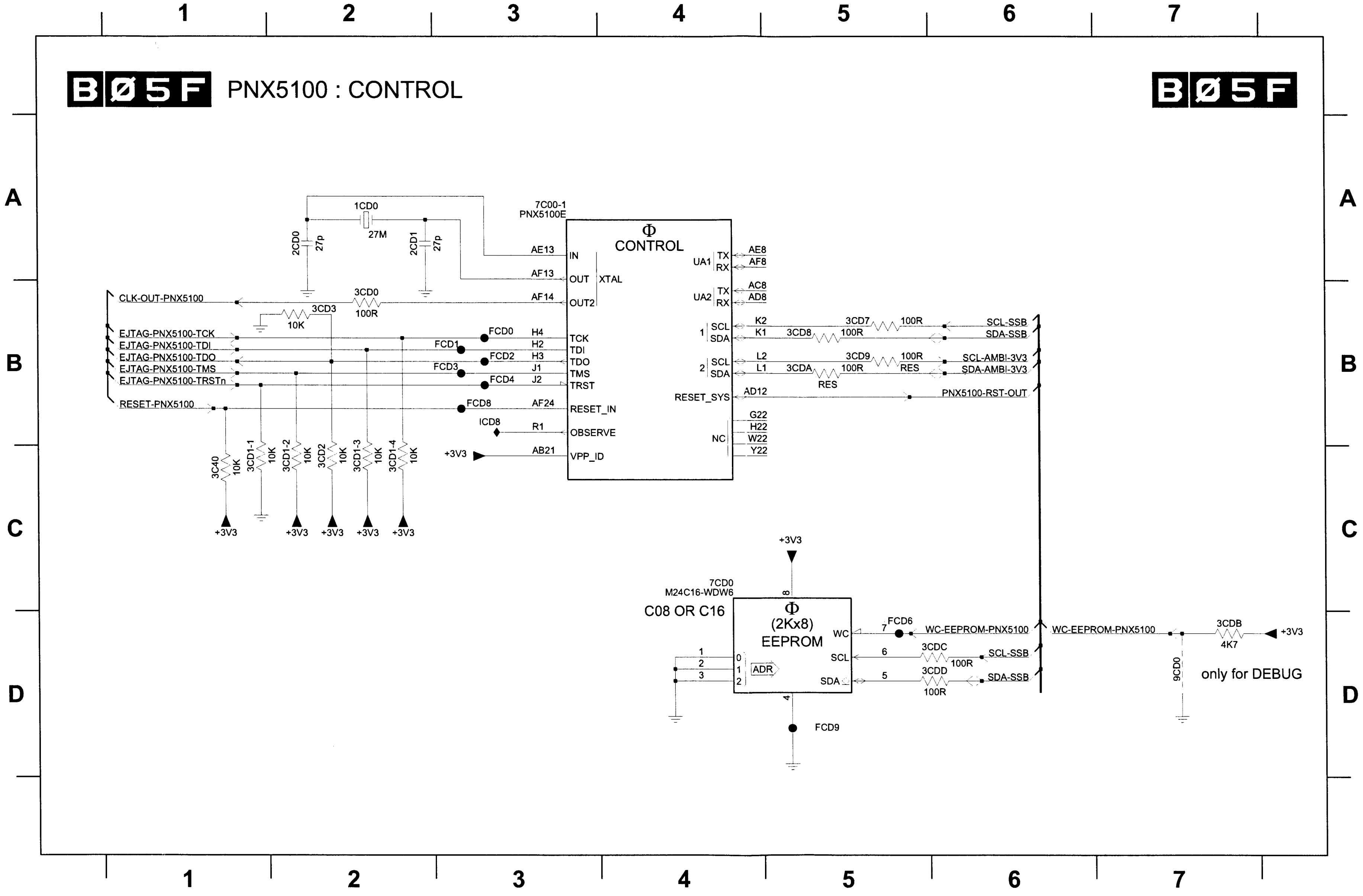
SSB: PNX5100 - Control


B05F
PNX5100 : CONTROL
B05F
7C00-1
PNX5100E
Φ
CONTROL
1CD0
27M
2CD0
27p
2CD1
27p
AE13
IN
AF13
OUT
XTAL
AF14
OUT2
CLK-OUT-PNX5100
3CD0
100R
3CD3
10K
EJTAG-PNX5100-TCK
EJTAG-PNX5100-TDI
EJTAG-PNX5100-TDO
EJTAG-PNX5100-TMS
EJTAG-PNX5100-TRSTn
RESET-PNX5100
FCD0
FCD1
FCD2
FCD3
FCD4
FCD8
H4
H2
H3
J1
J2
AF24
TCK
TDI
TDO
TMS
TRST
RESET_IN
ICD8
R1
OBSERVE
+3V3
AB21
VPP_ID
3C40
10K
3CD1-1
10K
3CD1-2
10K
3CD2
10K
3CD1-3
10K
3CD1-4
10K
+3V3
UA1
TX
RX
AE8
AF8
UA2
TX
RX
AC8
AD8
1
SCL
SDA
K2
K1
3CD7
100R
3CD8
100R
SCL-SSB
SDA-SSB
2
SCL
SDA
L2
L1
3CD9
100R
RES
3CDA
100R
RES
SCL-AMBI-3V3
SDA-AMBI-3V3
RESET_SYS
AD12
PNX5100-RST-OUT
NC
G22
H22
W22
Y22
+3V3
7CD0
M24C16-WDW6
C08 OR C16
Φ
(2Kx8)
EEPROM
8
4
WC
SCL
SDA
0
1
2
ADR
1
2
3
7
6
5
FCD6
WC-EEPROM-PNX5100
3CDC
100R
SCL-SSB
3CDD
100R
SDA-SSB
FCD9
WC-EEPROM-PNX5100
3CDB
4K7
+3V3
9CD0
only for DEBUG
1
2
3
4
5
6
7
A
B
C
D

1CD0	A2
2CD0	A2
2CD1	A2
3C40	C1
3CD0	B2
3CD1-1	C2
3CD1-2	C2
3CD1-3	C2
3CD1-4	C1
3CD2	C2
3CD3	B2
3CD7	B5
3CD8	B5
3CD9	B5
3CDA	B5
3CDB	D7
3CDC	D6
3CDD	D6
7C00-1	A3
7CD0	C4
9CD0	D7
FCD0	B3
FCD1	B3
FCD2	B3
FCD3	B3
FCD4	B3
FCD6	D5
FCD8	B3
FCD9	D5
ICD8	B3

CHN
SETNAME
CLASS_NO
CONTROL PNX5100
TV543 R2 LDIPNX
2008-10-10 3
8204 000 8928
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 9
130 - 6
A3
CHECK
DATE

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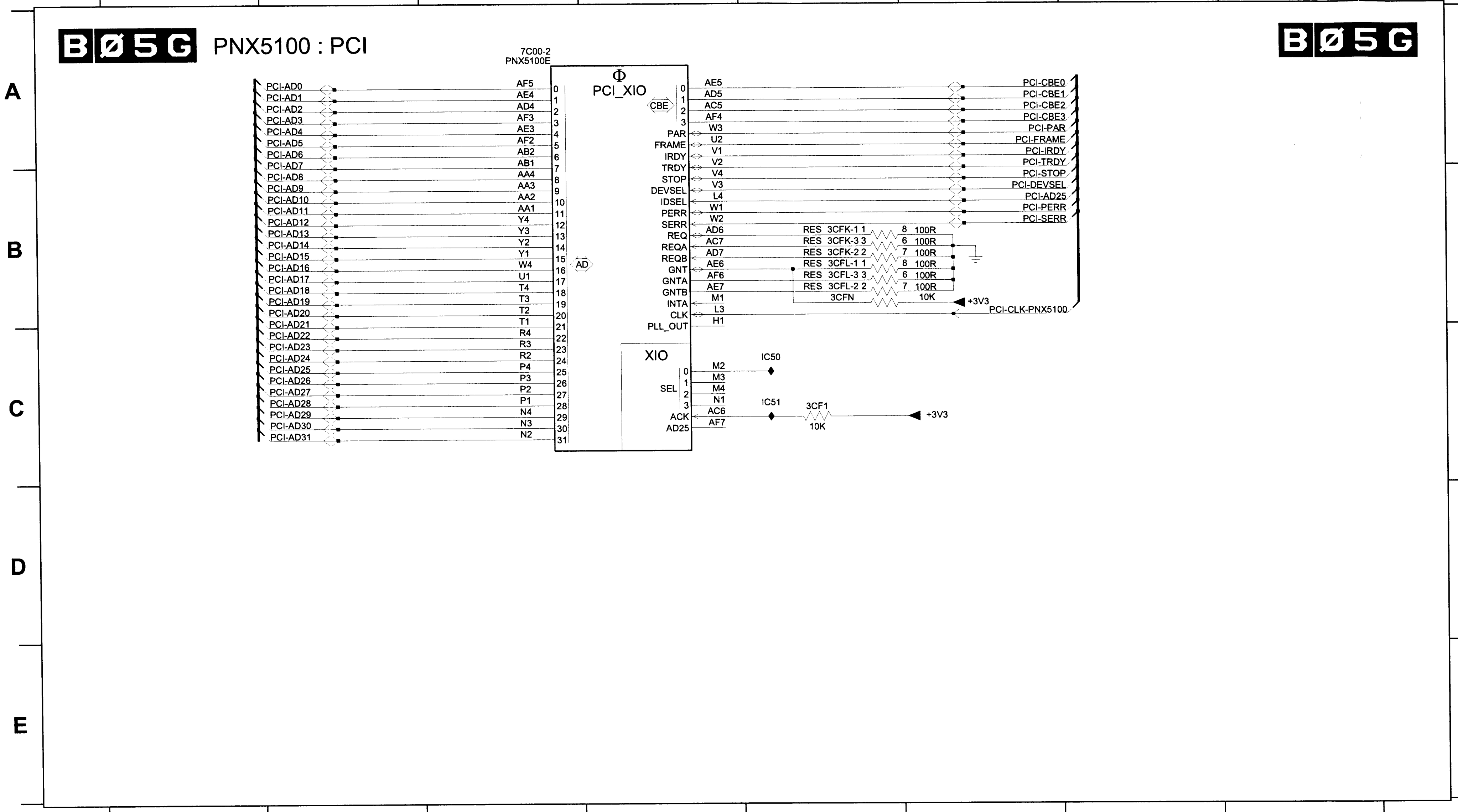
SSB: PNX5100 - PCI

B05G PNX5100 : PCI


7C00-2
PNX5100E
Φ
PCI_XIO
AD
CBE
PCI-AD0 AF5 0
PCI-AD1 AE4 1
PCI-AD2 AD4 2
PCI-AD3 AF3 3
PCI-AD4 AE3 4
PCI-AD5 AF2 5
PCI-AD6 AB2 6
PCI-AD7 AB1 7
PCI-AD8 AA4 8
PCI-AD9 AA3 9
PCI-AD10 AA2 10
PCI-AD11 AA1 11
PCI-AD12 Y4 12
PCI-AD13 Y3 13
PCI-AD14 Y2 14
PCI-AD15 Y1 15
PCI-AD16 W4 16
PCI-AD17 U1 17
PCI-AD18 T4 18
PCI-AD19 T3 19
PCI-AD20 T2 20
PCI-AD21 T1 21
PCI-AD22 R4 22
PCI-AD23 R3 23
PCI-AD24 R2 24
PCI-AD25 P4 25
PCI-AD26 P3 26
PCI-AD27 P2 27
PCI-AD28 P1 28
PCI-AD29 N4 29
PCI-AD30 N3 30
PCI-AD31 N2 31
0 AE5 PCI-CBE0
1 AD5 PCI-CBE1
2 AC5 PCI-CBE2
3 AF4 PCI-CBE3
PAR W3 PCI-PAR
FRAME U2 PCI-FRAME
IRDY V1 PCI-IRDY
TRDY V2 PCI-TRDY
STOP V4 PCI-STOP
DEVSEL V3 PCI-DEVSEL
IDSEL L4 PCI-AD25
PERR W1 PCI-PERR
SERR W2 PCI-SERR
REQ AD6 RES 3CFK-1 1 8 100R
REQA AC7 RES 3CFK-3 3 6 100R
REQB AD7 RES 3CFK-2 2 7 100R
GNT AE6 RES 3CFL-1 1 8 100R
GNTA AF6 RES 3CFL-3 3 6 100R
GNTB AE7 RES 3CFL-2 2 7 100R
INTA M1 3CFN 10K +3V3
CLK L3 PCI-CLK-PNX5100
PLL_OUT H1
XIO
SEL 0 M2 IC50
1 M3
2 M4
3 N1
ACK AC6 IC51 3CF1 10K +3V3
AD25 AF7
B05G

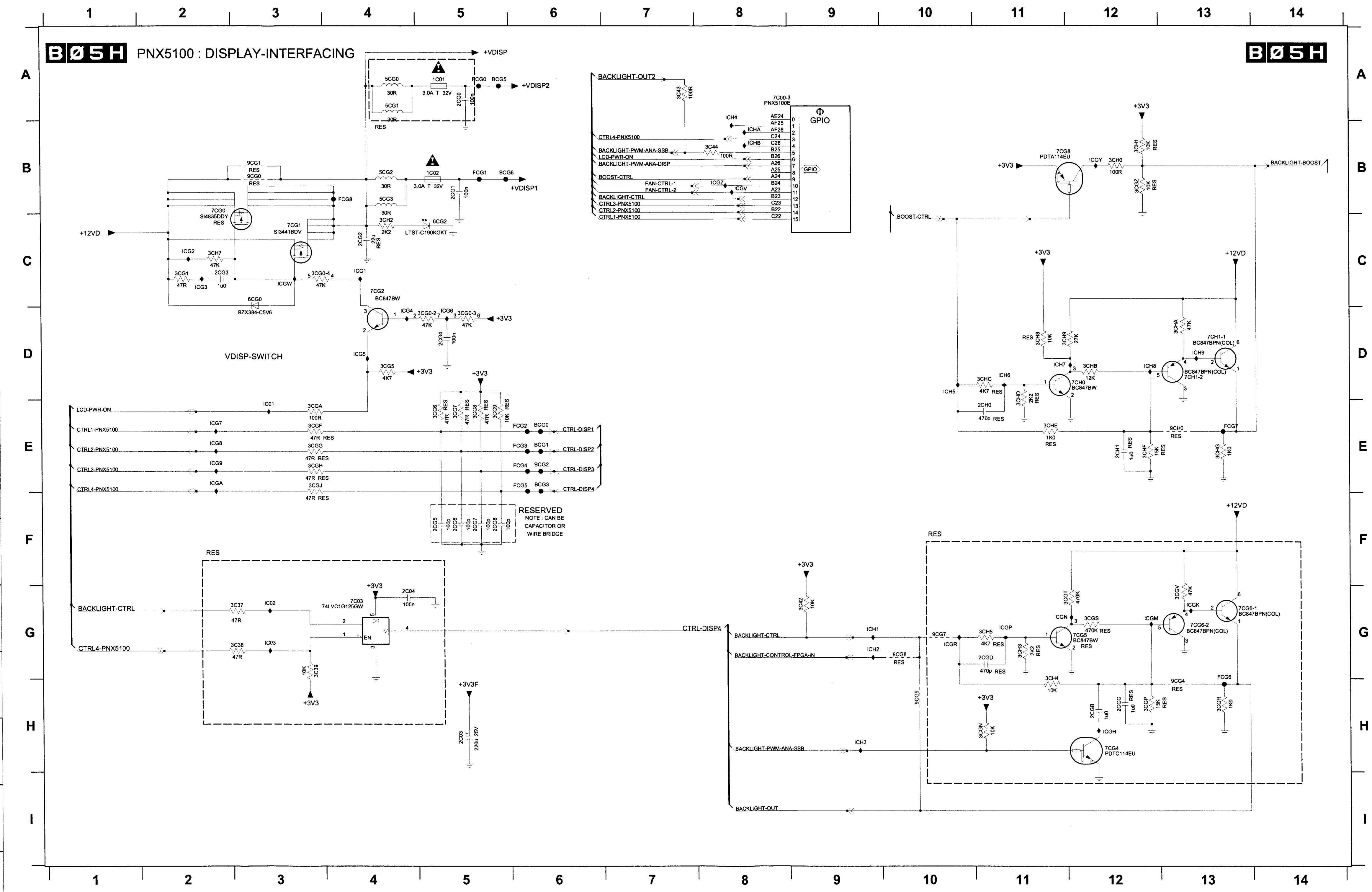
3CF1	C5
3CFK-1	B5
3CFK-2	B5
3CFK-3	B5
3CFL-1	B5
3CFL-2	B5
3CFL-3	B5
3CFN	B5
7C00-2	A3
IC50	C5
IC51	C5

CHN
SETNAME
CLASS_NO

PCI PNX5100
TV543 R2 LDIPNX

2008-10-10 3
2 2008-11-21
8204 000 8928
NAME Maelegheer Ingrid
SUPERS. 9
130 - 7 A3
CHECK
DATE

SSB: PNX5100 - Display-Interfacing

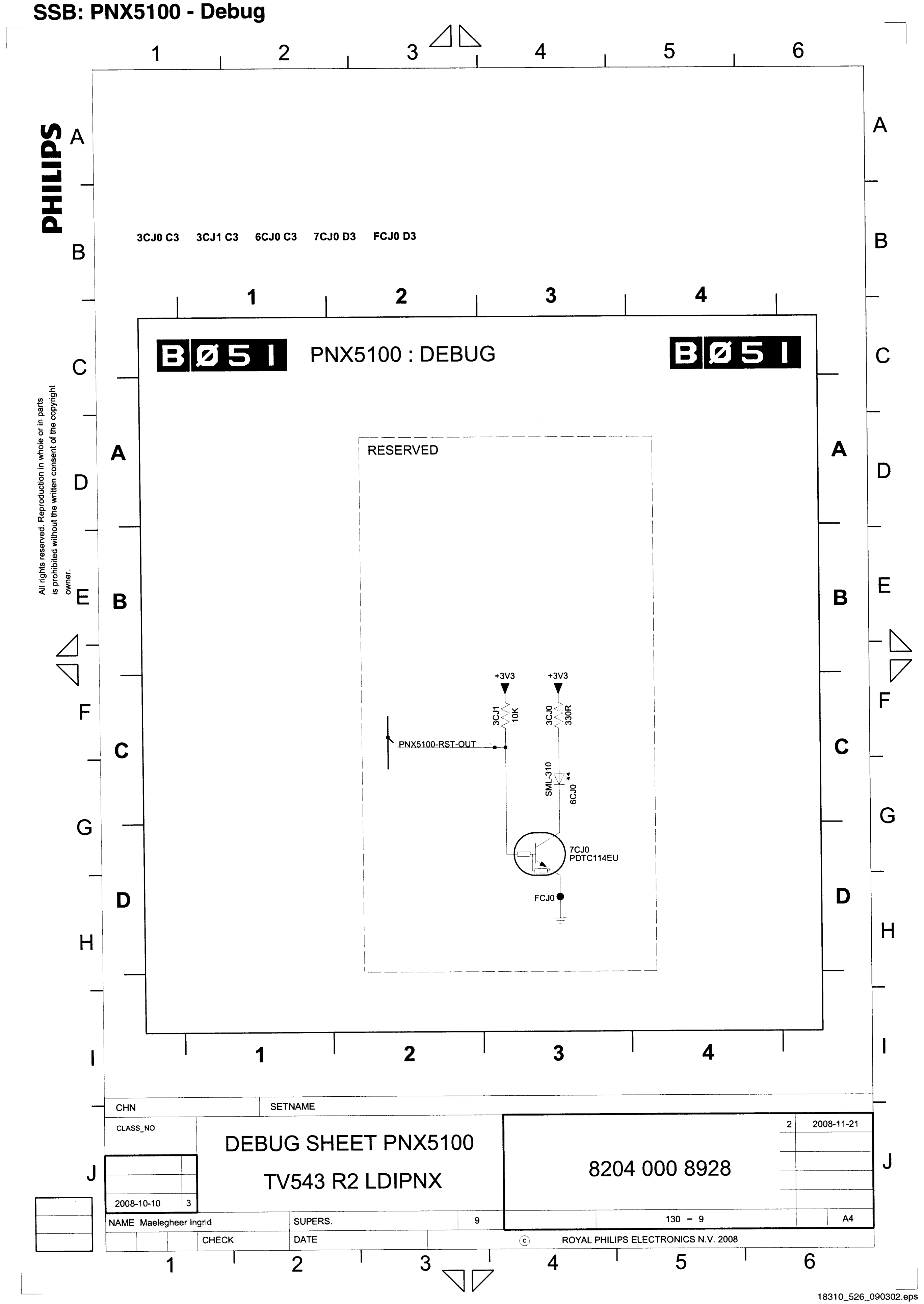

B05H
PNX5100 : DISPLAY-INTERFACING
+VDISP
5CG0 30R
5CG1 30R
1C01 3.0A T 32V
2CG0 100n
FCG0
BCG5
+VDISP2
RES
9CG1 RES
9CG0 RES
FCG8
7CG0 SI4835DDY RES
7CG1 SI3441BDV
5CG2 30R
5CG3 30R
1C02 3.0A T 32V
2CG1 100n
FCG1
BCG6
+VDISP1
3CH2 2K2
6CG2 LTST-C190KGKT
2CG2 22u RES
+12VD
ICG2
3CH7 47K
3CG1 47R
ICG3
2CG3 1u0
ICGW
3CG0-4 47K
ICG1
6CG0 BZX384-C5V6
7CG2 BC847BW
ICG4
3CG0-2 47K
ICG6
3CG0-3 47K
+3V3
2CG4 100n
ICG5
3CG5 4K7
VDISP-SWITCH
LCD-PWR-ON
IC01
3CGA 100R
CTRL1-PNX5100
ICG7
3CGF 47R RES
CTRL2-PNX5100
ICG8
3CGG 47R RES
CTRL3-PNX5100
ICG9
3CGH 47R RES
CTRL4-PNX5100
ICGA
3CGJ 47R RES
3CG6 47R RES
3CG7 47R RES
3CG8 47R RES
3CG9 10K RES
FCG2 BCG0 CTRL-DISP1
FCG3 BCG1 CTRL-DISP2
FCG4 BCG2 CTRL-DISP3
FCG5 BCG3 CTRL-DISP4
2CG5 100p
2CG6 100p
2CG7 100p
2CG8 100p
RESERVED
NOTE : CAN BE CAPACITOR OR WIRE BRIDGE
BACKLIGHT-OUT2
3C43 100R
7C00-3 PNX5100E
GPIO
ICH4
ICHA
ICHB
3C44 100R
BACKLIGHT-PWM-ANA-SSB
BACKLIGHT-PWM-ANA-DISP
BOOST-CTRL
FAN-CTRL-1
FAN-CTRL-2
ICGZ
ICGV
BACKLIGHT-CTRL
AE24 AF25 AF26 C24 C26 B25 B26 A26 A25 A24 B24 A23 B23 C23 B22 C22
7CG8 PDTA114EU
ICGY
3CH0 100R
3CH1 10K RES
3CGZ 10K RES
BACKLIGHT-BOOST
3CH8 10K RES
3CH9 27K
3CHA 47K
7CH1-1 BC847BPN(COL)
ICH9
ICH7
3CHB 12K
ICH8
7CH1-2 BC847BPN(COL)
7CH0 BC847BW
3CHC 4K7 RES
ICH6
ICH5
2CH0 470p RES
3CHD 2K2 RES
3CHE 1K0 RES
2CH1 1u0 RES
3CHF 15K RES
9CH0 RES
FCG7
3CHG 1K0
RES
3C37 47R
IC02
3C38 47R
IC03
3C39 10K
7C03 74LVC1G125GW
2C04 100n
EN
CTRL-DISP4
+3V3F
2C03 220u 25V
3C42 10K
ICH1
ICH2
BACKLIGHT-CONTROL-FPGA-IN
9CG8 RES
9CG7
ICGR
3CH5 4K7 RES
ICGP
2CGD 470p RES
3CH3 2K2 RES
7CG5 BC847BW
3CGS 470K RES
ICGN
3CGT 470K
3CGV 47K
ICGK
ICGM
7CG6-1 BC847BPN(COL)
7CG6-2 BC847BPN(COL)
3CH4 10K
2CGB 1u0
2CGC 1u0 RES
3CGP 15K RES
9CG4 RES
FCG6
3CGR 1K0
ICGH
3CGN 10K
9CG9
ICH3
7CG4 PDTC114EU
BACKLIGHT-OUT
+12VD

1C01	A5
1C02	B5
2C03	H5
2C04	G4
2CG0	A5
2CG1	B5
2CG2	C4
2CG3	C2
2CG4	D5
2CG5	F5
2CG6	F5
2CG7	F5
2CG8	F5
2CGB	H12
2CGC	H12
2CGD	G11
2CH0	E11
2CH1	E12
3C37	G3
3C38	G3
3C39	G3
3C42	G9
3C43	A7
3C44	B8
3CG0-2	D5
3CG0-3	D5
3CG0-4	C3
3CG1	C2
3CG5	D4
3CG6	E5
3CG7	E5
3CG8	E5
3CG9	E5
3CGA	E3
3CGF	E3
3CGG	E3
3CGH	E3
3CGJ	E3
3CGN	H11
3CGP	H12
3CGR	H13
3CGS	G12
3CGT	G11
3CGV	G13
3CGZ	B12
3CH0	B12
3CH1	B12
3CH2	C4
3CH3	G11
3CH4	H11
3CH5	G11
3CH7	C2
3CH8	D11
3CH9	D11
3CHA	D13
3CHB	D12
3CHC	D11
3CHD	D11
3CHE	E11
3CHF	E12
3CHG	E13
5CG0	A4
5CG1	A4
5CG2	B4
5CG3	B4
6CG0	C3
6CG2	C5
7C00-3	A9
7C03	G4
7CG0	B2
7CG1	C3
7CG2	C4
7CG4	H12
7CG5	G12
7CG6-1	G13
7CG6-2	G13
7CG8	B12
7CH0	D12
7CH1-1	D13
7CH1-2	D13
9CG0	B3
9CG1	B3
9CG4	H13
9CG7	G10
9CG8	G10
9CG9	H10
9CH0	E13
BCG0	E6
BCG1	E6
BCG2	E6
BCG3	E6
BCG5	A5
BCG6	B5
FCG0	A5
FCG1	B5
FCG2	E6
FCG3	E6
FCG4	E6
FCG5	E6
FCG6	H13
FCG7	E13
FCG8	B4
IC01	E3
IC02	G3
IC03	G3
ICG1	C4
ICG2	C2
ICG3	C2
ICG4	D4
ICG5	D4
ICG6	D5
ICG7	E2
ICG8	E2
ICG9	E2
ICGA	E2
ICGH	H12
ICGK	G13
ICGM	G12
ICGN	G11
ICGP	G11
ICGR	G10
ICGV	B8
ICGW	C3
ICGY	B12
ICGZ	B8
ICH1	G9
ICH2	G9
ICH3	H9
ICH4	A8
ICH5	D10
ICH6	D11
ICH7	D11
ICH8	D12
ICH9	D13
ICHA	B8
ICHB	B8

CHN		SETNAME			
CLASS_NO	DISPLAY INTERF PNX5100 TV543 R2 LDIPNX		8204 000 8928	2	2008-11-21
2008-10-10 3					
NAME Maelegheer Ingrid		SUPERS.	9	130 - 8	A2
CHECK		DATE		© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_525_090302.eps
090302

SSB: PNX5100 - Debug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1
2
3
4
5
6
A
B
C
D
E
F
G
H
I
J
3CJ0 C3
3CJ1 C3
6CJ0 C3
7CJ0 D3
FCJ0 D3
B051
PNX5100 : DEBUG
RESERVED
+3V3
+3V3
3CJ1
10K
3CJ0
330R
PNX5100-RST-OUT
SML-310
6CJ0
7CJ0
PDTC114EU
FCJ0
CHN
SETNAME
CLASS_NO
DEBUG SHEET PNX5100
TV543 R2 LDIPNX
8204 000 8928
2
2008-11-21
2008-10-10
3
NAME Maelegheer Ingrid
SUPERS.
9
130 - 9
A4
CHECK
DATE
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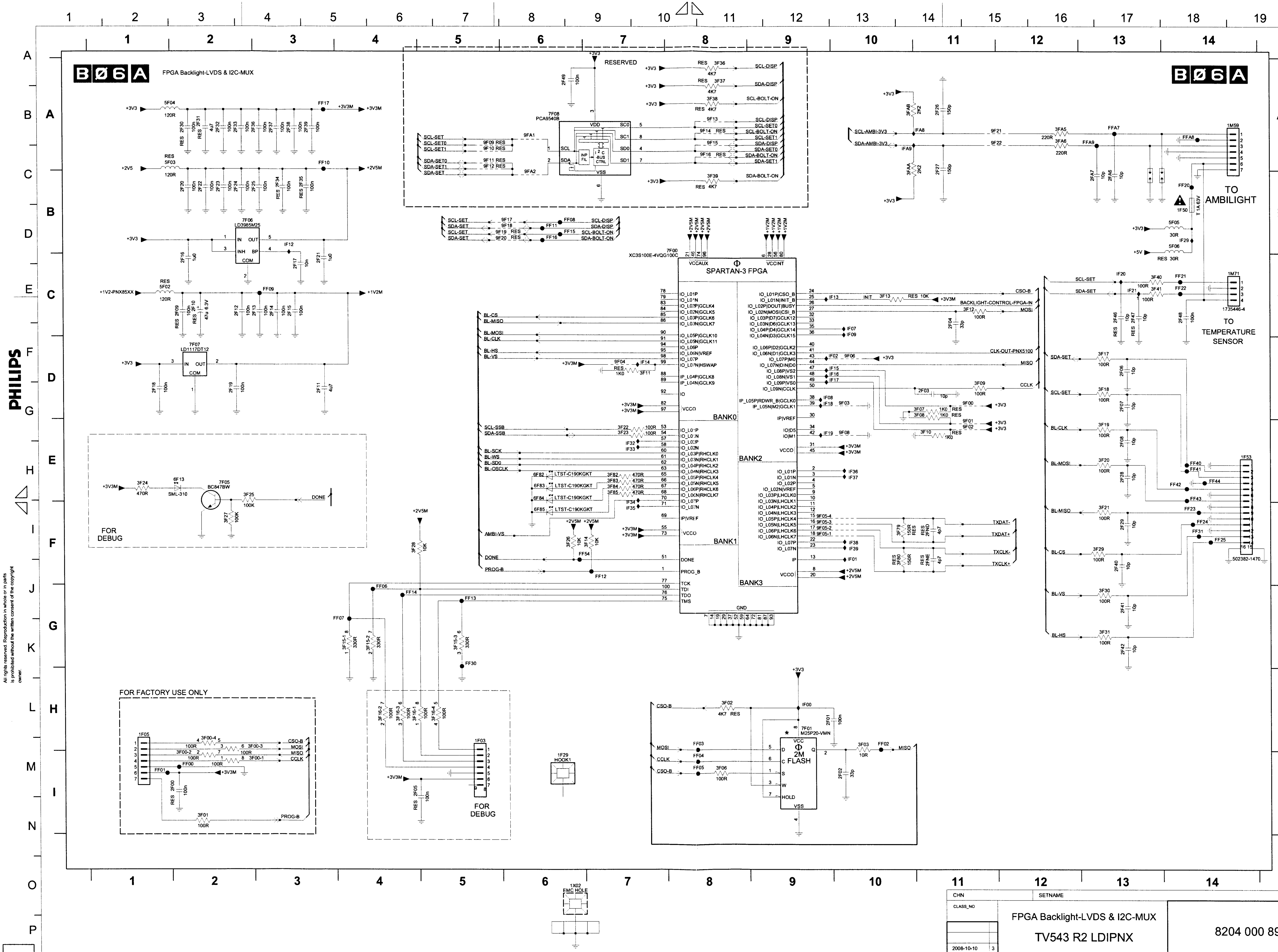
090302

Personal Notes:

10000_012_090121.eps
090121

SSB: FPGA Backlight-LVDS I^{2}C-Mux

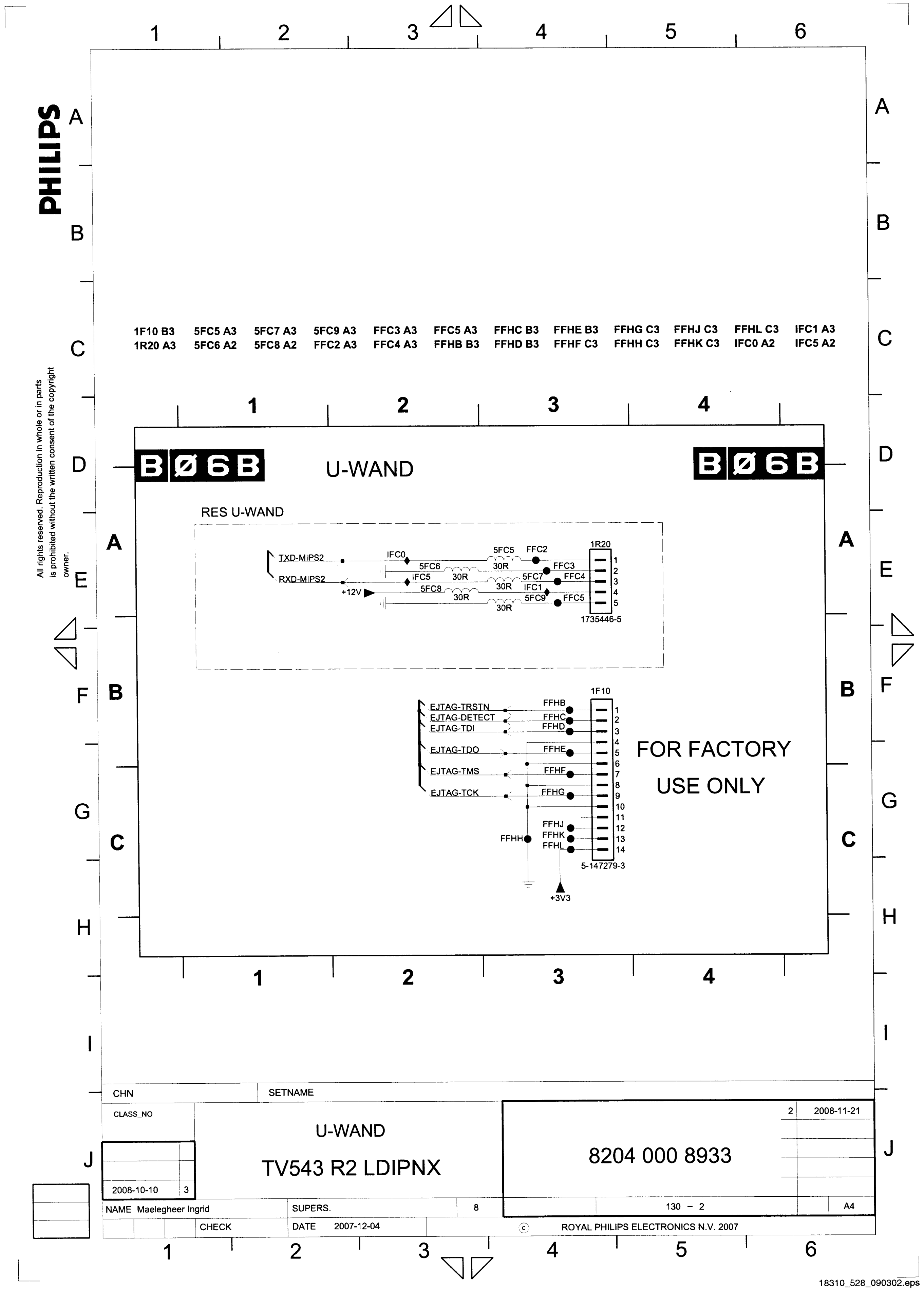

B06A
FPGA Backlight-LVDS & I2C-MUX
RESERVED
PCA9540B
SPARTAN-3 FPGA
XC3S100E-4VQG100C
BANK0
BANK1
BANK2
BANK3
LD3985M25
LD1117DT12
M25P20-VMN
2M FLASH
TO AMBILIGHT
TO TEMPERATURE SENSOR
FOR DEBUG
FOR FACTORY USE ONLY
HOOK1
EMC HOLE
PHILIPS

1F03	H5
1F05	H1
1F29	I6
1F50	B14
1F53	E14
1M59	A14
1M71	C14
2F00	I2
2F01	H9
2F02	I10
2F03	D11
2F04	C11
2F05	I4
2F06	D13
2F07	D13
2F08	E13
2F09	C2
2F10	C2
2F11	D3
2F12	C2
2F13	C3
2F14	C3
2F15	C3
2F16	C2
2F17	C3
2F18	D1
2F19	D2
2F20	B2
2F21	C3
2F22	B2
2F23	B2
2F24	B2
2F25	B3
2F26	A11
2F27	A11
2F28	E13
2F29	F13
2F30	A2
2F31	A2
2F32	A2
2F33	A2
2F34	B3
2F35	B3
2F36	A3
2F37	A3
2F38	A3
2F39	A3
2F40	F13
2F41	G13
2F42	G13
2F46	C13
2F47	C13
2F48	C14
2F49	A6
2FA6	B13
2FA7	B13
2FND	F11
2FNE	F11
3F00-1	I3
3F00-2	I2
3F00-3	H2
3F00-4	H2
3F01	I2
3F02	H8
3F03	H10
3F06	I8
3F07	D11
3F08	D11
3F09	D11
3F10	E11
3F11	D7
3F12	C11
3F13	C10
3F14	F7
3F15-1	G4
3F15-2	G4
3F15-3	G5
3F16-1	H4
3F16-2	H4
3F16-3	H4
3F16-4	H5
3F17	D13
3F18	D13
3F19	E13
3F20	E13
3F21	F13
3F22	E7
3F23	E7
3F24	E1
3F25	E2
3F26	F6
3F27	F2
3F28	F4
3F29	F13
3F30	G13
3F31	G13
3F36	A8
3F37	A8
3F38	A8
3F39	B8
3F40	C13
3F41	C13
3F79	F10
3F80	F10
3F82	E7
3F83	E7
3F84	E7
3F85	E7
3FA5	A12
3FA6	A12
3FAA	A10
3FAB	A10
5F02	C1
5F03	A2
5F04	A2
5F05	B14
5F06	B14
6F13	E2
6F82	E6
6F83	E6
6F84	E6
6F85	F6
7F00	B8
7F01	H9
7F05	E2
7F06	B2
7F07	D2
7F08	A6
9F00	D11
9F01	E11
9F02	E11
9F03	D10
9F04	D7
9F05-1	F9
9F05-2	F9
9F05-3	F9
9F05-4	F9
9F06	D10
9F08	E10
9F09	A5
9F10	A5
9F11	A5
9F12	A5
9F13	A8
9F14	A8
9F15	A8
9F16	A8
9F17	B6
9F18	B6
9F19	B6
9F20	B6
9F21	A12
9F22	A12
9FA1	A6
9FA2	A6
FF00	I2
FF01	I1
FF02	H10
FF03	H8
FF04	I8
FF05	I8
FF06	G4
FF07	G4
FF08	B6
FF09	C3
FF10	A3
FF11	B6
FF12	F7
FF13	G5
FF14	G4
FF15	B6
FF16	B6
FF17	A3
FF20	B14
FF21	C14
FF22	C14
FF23	F14
FF24	F14
FF25	F14
FF30	G5
FF31	F14
FF40	E14
FF41	E14
FF42	E14
FF43	E14
FF44	E14
FF54	F6
FFA7	A13
FFA8	A14
FFA9	A13
IF00	H9
IF01	F10
IF02	D10
IF07	C10
IF08	D9
IF09	C10
IF12	B3
IF13	C10
IF14	D7
IF15	D10
IF16	D10
IF17	D10
IF18	D9
IF19	E9
IF20	C13
IF21	C13
IF29	B14
IF32	E7
IF33	E7
IF34	F7
IF35	F7
IF36	E10
IF37	E10
IF38	F10
IF39	F10
IFA8	A11
IFA9	A10

CHN	SETNAME			
CLASS_NO	FPGA Backlight-LVDS & I2C-MUX TV543 R2 LDIPNX	8204 000 8933	2	2008-11-21
2008-10-10	3			
NAME Maelegheer Ingrid	SUPERS.	8	130 – 1	A2
CHECK	DATE 2007-12-04			

18310_527_090302.eps
090302

SSB: U-Wand


PHILIPS
1F10 B3
1R20 A3
5FC5 A3
5FC6 A2
5FC7 A3
5FC8 A2
5FC9 A3
FFC2 A3
FFC3 A3
FFC4 A3
FFC5 A3
FFHB B3
FFHC B3
FFHD B3
FFHE B3
FFHF C3
FFHG C3
FFHH C3
FFHJ C3
FFHK C3
FFHL C3
IFC0 A2
IFC1 A3
IFC5 A2
B06B
U-WAND
RES U-WAND
TXD-MIPS2
RXD-MIPS2
+12V
IFC0
IFC5
IFC1
5FC5
5FC6
5FC7
5FC8
5FC9
30R
FFC2
FFC3
FFC4
FFC5
1R20
1735446-5
1F10
EJTAG-TRSTN
EJTAG-DETECT
EJTAG-TDI
EJTAG-TDO
EJTAG-TMS
EJTAG-TCK
FFHB
FFHC
FFHD
FFHE
FFHF
FFHG
FFHH
FFHJ
FFHK
FFHL
5-147279-3
+3V3
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CHN
SETNAME
CLASS_NO
U-WAND
TV543 R2 LDIPNX
8204 000 8933
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid
SUPERS.
8
130 - 2
A4
CHECK
DATE 2007-12-04
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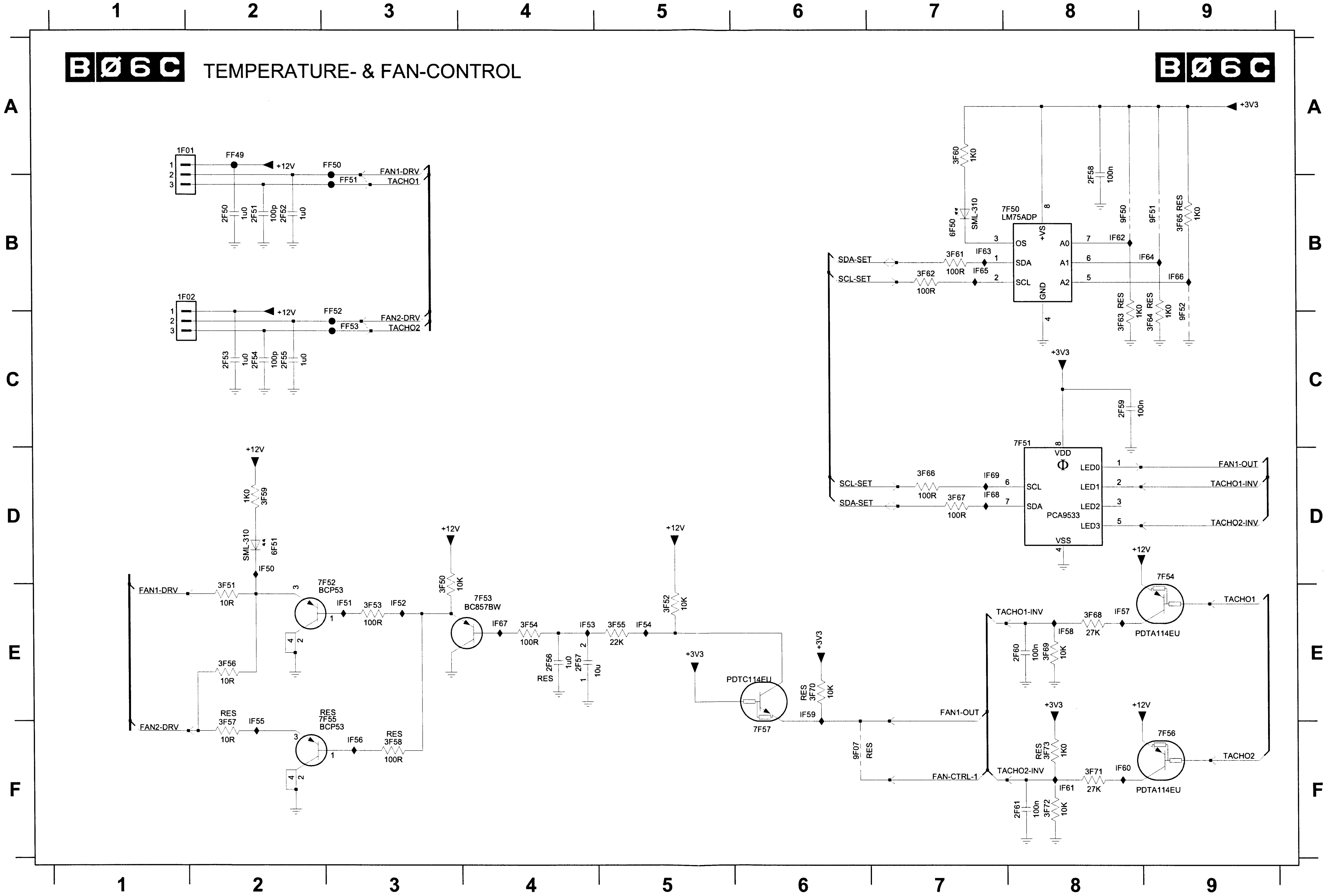
090302

Personal Notes:

10000_012_090121.eps
090121

SSB: Temperature & Fan control

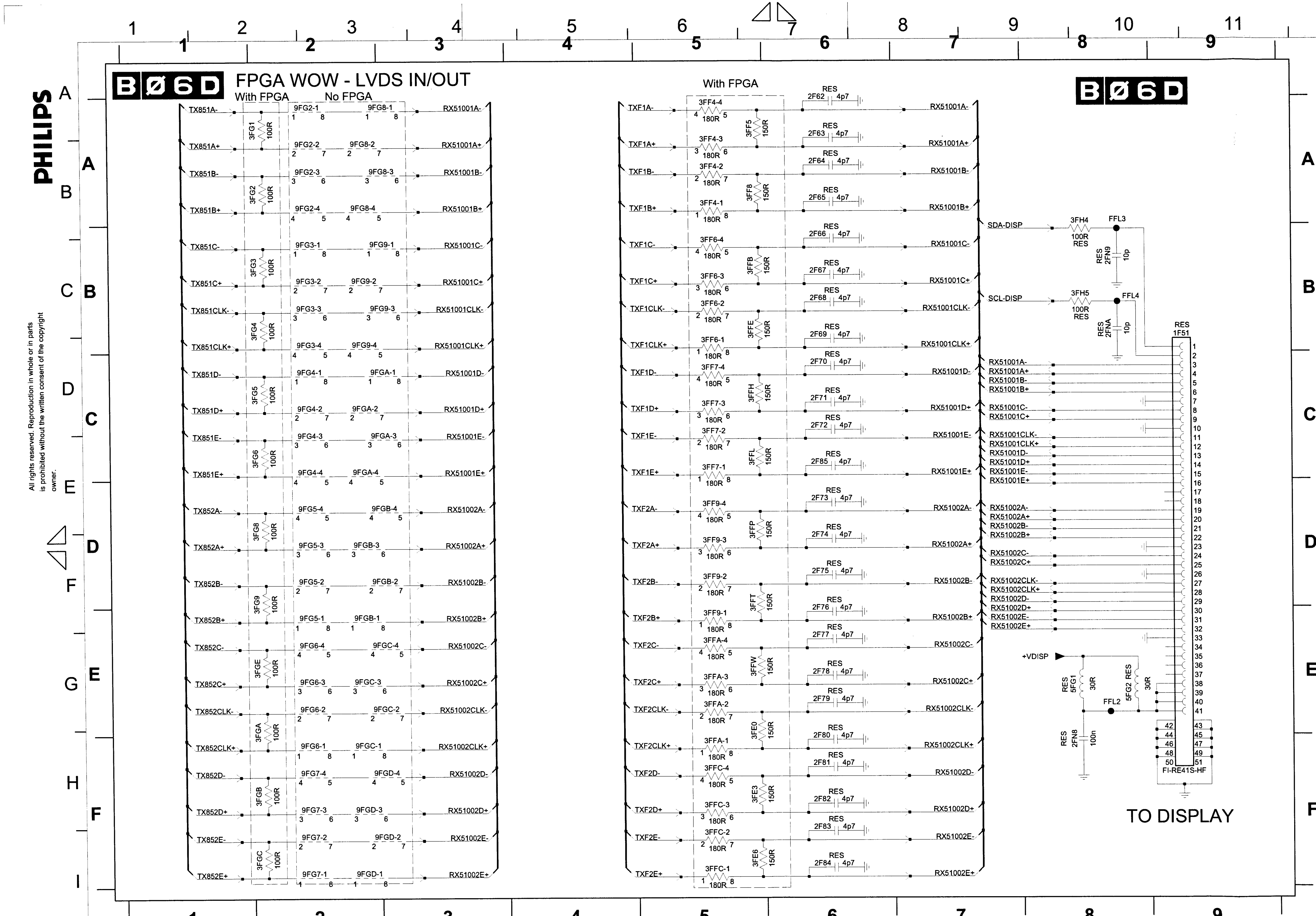

B06C TEMPERATURE- & FAN-CONTROL
B06C
1F01
FF49
+12V
FF50
FAN1-DRV
FF51
TACHO1
2F50 1u0
2F51 100p
2F52 1u0
1F02
+12V
FF52
FAN2-DRV
FF53
TACHO2
2F53 1u0
2F54 100p
2F55 1u0
+3V3
3F60 1K0
2F58 100n
6F50 SML-310
7F50 LM75ADP
OS SDA SCL +VS GND A0 A1 A2
IF62 IF64 IF66
9F50 9F51
3F65 RES 1K0
SDA-SET
SCL-SET
3F61 100R
IF63
IF65
3F62 100R
3F63 RES 1K0
3F64 RES 1K0
9F52
+3V3
2F59 100n
7F51
VDD
LED0 LED1 LED2 LED3
SCL SDA
PCA9533
VSS
SCL-SET
SDA-SET
3F66 100R
IF69
IF68
3F67 100R
FAN1-OUT
TACHO1-INV
TACHO2-INV
+12V
1K0 3F59
SML-310 6F51
IF50
FAN1-DRV
3F51 10R
7F52 BCP53
IF51
3F53 100R
IF52
+12V
3F50 10K
7F53 BC857BW
IF67
3F54 100R
IF53
3F55 22K
IF54
+12V
3F52 10K
2F56 RES 1u0
2F57 10u
3F56 10R
+3V3
PDTC114EU
7F57
+3V3
RES 3F70 10K
IF59
FAN2-DRV
RES 3F57 10R
IF55
RES 7F55 BCP53
IF56
RES 3F58 100R
9F07 RES
FAN1-OUT
FAN-CTRL-1
+12V
7F54
TACHO1
TACHO1-INV
3F68 27K
IF57
IF58
2F60 100n
3F69 10K
PDTA114EU
+3V3
RES 3F73 1K0
+12V
7F56
TACHO2
TACHO2-INV
3F71 27K
IF60
IF61
2F61 100n
3F72 10K
PDTA114EU

1F01 A1	IF66 B9
1F02 B1	IF67 E4
2F50 B2	IF68 D7
2F51 B2	IF69 D7
2F52 B2	
2F53 C2	
2F54 C2	
2F55 C2	
2F56 E4	
2F57 E4	
2F58 B8	
2F59 C8	
2F60 E8	
2F61 F8	
3F50 E3	
3F51 E2	
3F52 E5	
3F53 E3	
3F54 E4	
3F55 E5	
3F56 E2	
3F57 F2	
3F58 F3	
3F59 D2	
3F60 A7	
3F61 B7	
3F62 B7	
3F63 C8	
3F64 C9	
3F65 B9	
3F66 D7	
3F67 D7	
3F68 E8	
3F69 E8	
3F70 E6	
3F71 F8	
3F72 F8	
3F73 F8	
6F50 B7	
6F51 D2	
7F50 B7	
7F51 C8	
7F52 D3	
7F53 E4	
7F54 D9	
7F55 E3	
7F56 F9	
7F57 F6	
9F07 F6	
9F50 B8	
9F51 B9	
9F52 C9	
FF49 A2	
FF50 A3	
FF51 B3	
FF52 C3	
FF53 C3	
IF50 D2	
IF51 E3	
IF52 E3	
IF53 E4	
IF54 E5	
IF55 F2	
IF56 F3	
IF57 E8	
IF58 E8	
IF59 E6	
IF60 F8	
IF61 F8	
IF62 B8	
IF63 B7	
IF64 B9	
IF65 B7	

CHN
SETNAME
CLASS_NO
TEMPERATURE- & FAN-CONTROL
TV543 R2 LDIPNX
8204 000 8933
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid
SUPERS. 8
130 - 3
A3
CHECK
DATE 2007-12-04

18310_529_090303.eps
090303

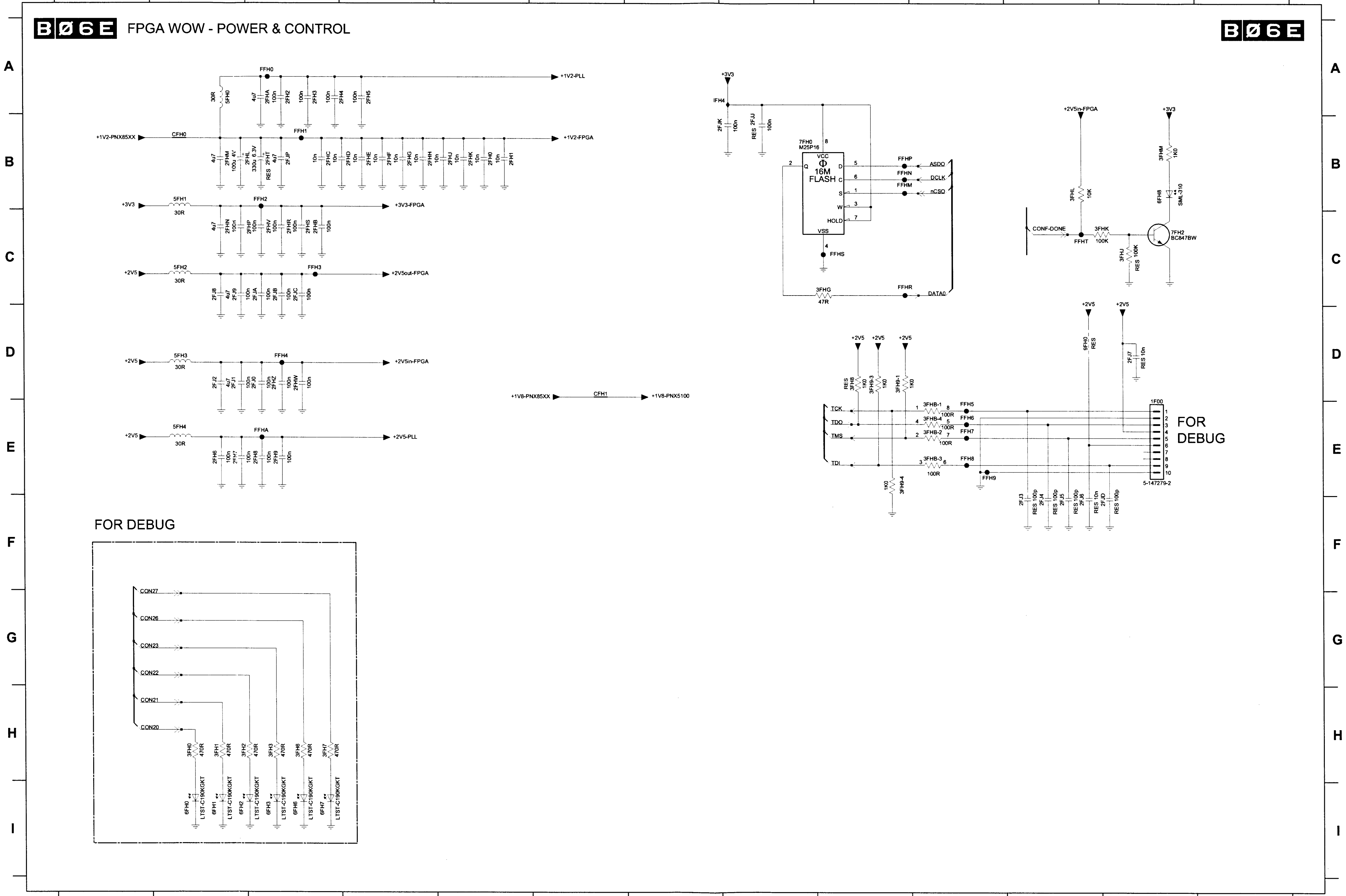
SSB: FPGA WOW - LVDS In/Out


B06D
FPGA WOW - LVDS IN/OUT
With FPGA
No FPGA
With FPGA
RES
TX851A- … TX852E+
RX51001A- … RX51002E+
TXF1A- … TXF2E+
100R
180R
150R
4p7
SDA-DISP
SCL-DISP
3FH4 100R RES
3FH5 100R RES
FFL3
FFL4
2FN9 10p
2FNA 10p
RES 1F51
FI-RE41S-HF
+VDISP
5FG1 30R
5FG2 30R
FFL2
2FN8 100n
TO DISPLAY

1F51	B9
2F62	A6
2F63	A6
2F64	A6
2F65	A6
2F66	B6
2F67	B6
2F68	B6
2F69	B6
2F70	C6
2F71	C6
2F72	C6
2F73	D6
2F74	D6
2F75	D6
2F76	E6
2F77	E6
2F78	E6
2F79	E6
2F80	F6
2F81	F6
2F82	F6
2F83	F6
2F84	F6
2F85	C6
2FN8	F8
2FN9	B8
2FNA	B8
3FE0	E5
3FE3	F5
3FE6	F5
3FF4-1	A5
3FF4-2	A5
3FF4-3	A5
3FF4-4	A5
3FF5	A5
3FF6-1	B5
3FF6-2	B5
3FF6-3	B5
3FF6-4	B5
3FF7-1	C5
3FF7-2	C5
3FF7-3	C5
3FF7-4	C5
3FF8	A5
3FF9-1	E5
3FF9-2	D5
3FF9-3	D5
3FF9-4	D5
3FFA-1	F5
3FFA-2	E5
3FFA-3	E5
3FFA-4	E5
3FFB	B5
3FFC-1	F5
3FFC-2	F5
3FFC-3	F5
3FFC-4	F5
3FFE	B5
3FFH	C5
3FFL	C5
3FFP	D5
3FFT	D5
3FFW	E5
3FG1	A2
3FG2	A2
3FG3	B2
3FG4	B2
3FG5	C2
3FG6	C2
3FG8	D2
3FG9	D2
3FGA	E2
3FGB	F2
3FGC	F2
3FGE	E2
3FH4	A8
3FH5	B8
5FG1	E8
5FG2	E8
9FG2-1	A2
9FG2-2	A2
9FG2-3	A2
9FG2-4	A2
9FG3-1	B2
9FG3-2	B2
9FG3-3	B2
9FG3-4	B2
9FG4-1	C2
9FG4-2	C2
9FG4-3	C2
9FG4-4	C2
9FG5-1	E2
9FG5-2	D2
9FG5-3	D2
9FG5-4	D2
9FG6-1	F2
9FG6-2	E2
9FG6-3	E2
9FG6-4	E2
9FG7-1	F2
9FG7-2	F2
9FG7-3	F2
9FG7-4	F2
9FG8-1	A3
9FG8-2	A2
9FG8-3	A3
9FG8-4	A2
9FG9-1	B3
9FG9-2	B2
9FG9-3	B3
9FG9-4	B2
9FGA-1	C3
9FGA-2	C2
9FGA-3	C3
9FGA-4	C2
9FGB-1	E2
9FGB-2	D3
9FGB-3	D2
9FGB-4	D3
9FGC-1	F2
9FGC-2	E3
9FGC-3	E2
9FGC-4	E3
9FGD-1	F2
9FGD-2	F3
9FGD-3	F2
9FGD-4	F3
FFL2	E8
FFL3	A8
FFL4	B8

CHN	SETNAME		
CLASS_NO	FPGA WOW - LVDS IN/OUT TV543 R2 LDIPNX	8204 000 8933	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 8	130 - 4	A3
CHECK	DATE 2007-12-04		

SSB: FPGA WOW - Power & Control


B06E
FPGA WOW - POWER & CONTROL
B06E
FFH0
+1V2-PLL
30R
5FH0
4u7
2FHA
100n
2FH2
100n
2FH3
100n
2FH4
100n
2FH5
+1V2-PNX85XX
CFH0
FFH1
+1V2-FPGA
4u7
2FHM
100u 4V
2FHL
330u 6.3V
2FHT
RES
4u7
2FJP
10n
2FHC
10n
2FHD
10n
2FHE
10n
2FHF
10n
2FHG
10n
2FHH
10n
2FHJ
10n
2FHK
10n
2FH0
10n
2FH1
+3V3
5FH1
30R
FFH2
+3V3-FPGA
4u7
2FHN
100n
2FHP
100n
2FHV
100n
2FHR
100n
2FHS
2FHB
100n
+2V5
5FH2
30R
FFH3
+2V5out-FPGA
2FJ8
4u7
2FJ9
100n
2FJA
100n
2FJB
100n
2FJC
100n
+2V5
5FH3
30R
FFH4
+2V5in-FPGA
2FJ2
4u7
2FJ1
100n
2FJ0
100n
2FHZ
100n
2FHW
100n
+2V5
5FH4
30R
FFHA
+2V5-PLL
2FH6
100n
2FH7
100n
2FH8
100n
2FH9
100n
+1V8-PNX85XX
CFH1
+1V8-PNX5100
+3V3
IFH4
2FJK
100n
RES 2FJJ
100n
7FH0
M25P16
8
VCC
Φ
16M
FLASH
Q
D
C
S
W
HOLD
VSS
2
5
6
1
3
7
4
FFHS
FFHP
ASDO
FFHN
DCLK
FFHM
nCSO
3FHG
47R
FFHR
DATA0
+2V5in-FPGA
3FHL
10K
+3V3
3FHM
1K0
6FH8
SML-310
CONF-DONE
FFHT
3FHK
100K
3FHJ
RES 100K
7FH2
BC847BW
+2V5
+2V5
9FH0
RES
2FJ7
RES 10n
+2V5
+2V5
+2V5
RES
3FH8
1K0
3FH9-3
1K0
3FH9-1
1K0
TCK
TDO
TMS
TDI
3FHB-1
100R
3FHB-4
100R
3FHB-2
100R
3FHB-3
100R
FFH5
FFH6
FFH7
FFH8
FFH9
1K0
3FH9-4
2FJ3
RES 100p
2FJ4
RES 100p
2FJ5
RES 100p
2FJ6
RES 10n
2FJD
RES 100p
1F00
1
2
3
4
5
6
7
8
9
10
5-147279-2
FOR DEBUG
FOR DEBUG
CON27
CON26
CON23
CON22
CON21
CON20
3FH0
470R
3FH1
470R
3FH2
470R
3FH3
470R
3FH6
470R
3FH7
470R
6FH0
LTST-C190KGKT
6FH1
LTST-C190KGKT
6FH2
LTST-C190KGKT
6FH3
LTST-C190KGKT
6FH6
LTST-C190KGKT
6FH7
LTST-C190KGKT

1F00	E12
2FH0	B5
2FH1	B5
2FH2	A3
2FH3	A3
2FH4	A3
2FH5	A4
2FH6	E2
2FH7	E2
2FH8	E3
2FH9	E3
2FHA	A3
2FHB	C3
2FHC	B3
2FHD	B4
2FHE	B4
2FHF	B4
2FHG	B4
2FHH	B4
2FHJ	B5
2FHK	B5
2FHL	B2
2FHM	B2
2FHN	C2
2FHP	C3
2FHR	C3
2FHS	C3
2FHT	B3
2FHV	C3
2FHW	D3
2FHZ	D3
2FJ0	D3
2FJ1	D2
2FJ2	D2
2FJ3	F11
2FJ4	F11
2FJ5	F11
2FJ6	F11
2FJ7	D12
2FJ8	C2
2FJ9	C2
2FJA	C3
2FJB	C3
2FJC	C3
2FJD	F12
2FJJ	B8
2FJK	B7
2FJP	B3
3FH0	H2
3FH1	H2
3FH2	H2
3FH3	H3
3FH6	H3
3FH7	H3
3FH8	D9
3FH9-1	D9
3FH9-2	D9
3FH9-3	E9
3FHB-1	E10
3FHB-2	E10
3FHB-3	E10
3FHB-4	E10
3FHG	C9
3FHJ	C12
3FHK	C12
3FHL	B11
3FHM	B12
5FH0	A2
5FH1	B2
5FH2	C2
5FH3	D2
5FH4	E2
6FH0	I2
6FH1	I2
6FH2	I2
6FH3	I3
6FH6	I3
6FH7	I3
6FH8	B12
7FH0	B8
7FH2	C12
9FH0	D11
CFH0	B2
CFH1	D6
FFH0	A3
FFH1	B3
FFH2	B3
FFH3	C3
FFH4	D3
FFH5	E10
FFH6	E10
FFH7	E10
FFH8	E10
FFH9	E10
FFHA	E3
FFHM	B9
FFHN	B9
FFHP	B9
FFHR	C9
FFHS	C9
FFHT	C11
IFH4	A7

CHN	SETNAME			
CLASS_NO	FPGA WOW - POWER & CONTROL TV543 R2 LDIPNX	8204 000 8933	2	2008-11-21
2008-10-10 3				
NAME Maelegheer Ingrid	SUPERS. 8	130 - 5		A2
CHECK	DATE 2007-12-04			

18310_531_090303.eps
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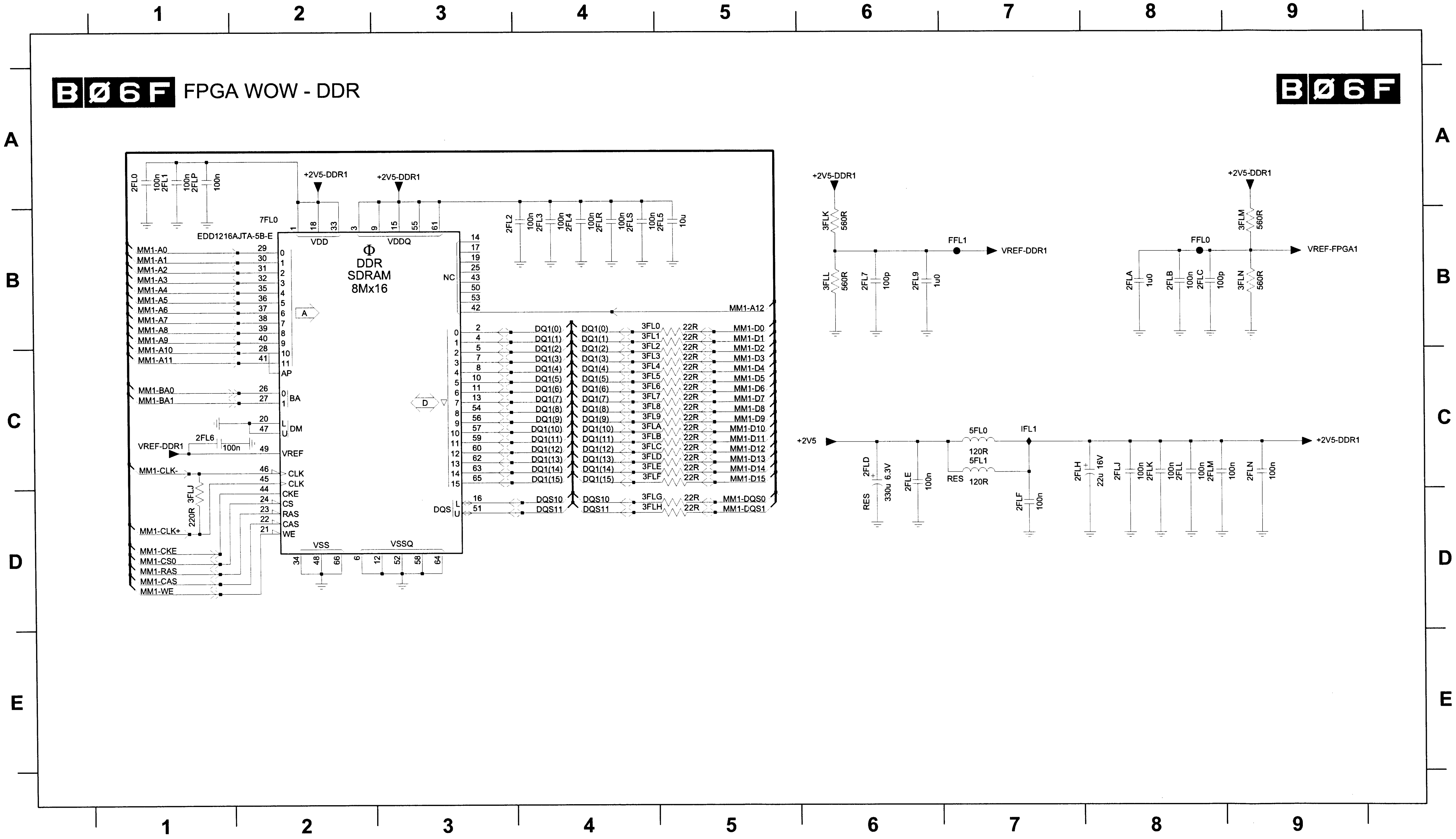
SSB: FPGA WOW - DDR


B06F FPGA WOW - DDR
B06F
7FL0
EDD1216AJTA-5B-E
DDR SDRAM 8Mx16
VDD
VDDQ
VSS
VSSQ
NC
DQS
VREF
CLK
CKE
CS
RAS
CAS
WE
BA
DM
AP
+2V5-DDR1
2FL0
2FL1
2FLP
100n
2FL2
2FL3
2FL4
2FLR
2FLS
2FL5
10u
MM1-A0
MM1-A1
MM1-A2
MM1-A3
MM1-A4
MM1-A5
MM1-A6
MM1-A7
MM1-A8
MM1-A9
MM1-A10
MM1-A11
MM1-A12
MM1-BA0
MM1-BA1
VREF-DDR1
2FL6
MM1-CLK-
MM1-CLK+
3FLJ
220R
MM1-CKE
MM1-CS0
MM1-RAS
MM1-CAS
MM1-WE
DQ1(0)
DQ1(15)
DQS10
DQS11
3FL0
3FLF
3FLG
3FLH
22R
MM1-D0
MM1-D15
MM1-DQS0
MM1-DQS1
3FLK
3FLL
560R
2FL7
100p
2FL9
1u0
FFL1
VREF-DDR1
FFL0
VREF-FPGA1
2FLA
2FLB
2FLC
3FLM
3FLN
+2V5
5FL0
5FL1
120R
RES
IFL1
2FLD
330u 6.3V
2FLE
2FLF
2FLH
22u 16V
2FLJ
2FLK
2FLL
2FLM
2FLN
+2V5-DDR1

2FL0	A1
2FL1	A1
2FL2	B3
2FL3	B4
2FL4	B4
2FL5	B5
2FL6	C1
2FL7	B6
2FL9	B6
2FLA	B8
2FLB	B8
2FLC	B8
2FLD	C6
2FLE	C6
2FLF	D7
2FLH	C7
2FLJ	C8
2FLK	C8
2FLL	C8
2FLM	C8
2FLN	C9
2FLP	A1
2FLR	B4
2FLS	B4
3FL0	B4
3FL1	B4
3FL2	C4
3FL3	C4
3FL4	C4
3FL5	C4
3FL6	C4
3FL7	C4
3FL8	C4
3FL9	C4
3FLA	C4
3FLB	C4
3FLC	C4
3FLD	C4
3FLE	C4
3FLF	C4
3FLG	D4
3FLH	D4
3FLJ	D1
3FLK	B6
3FLL	B6
3FLM	B9
3FLN	B9
5FL0	C7
5FL1	C7
7FL0	B2
FFL0	B8
FFL1	B7
IFL1	C7

CHN
SETNAME
CLASS_NO
FPGA WOW - DDR
TV543 R2 LDIPNX
2008-10-10 3
8204 000 8933
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 8
130 - 6
A3
CHECK
DATE 2007-12-04

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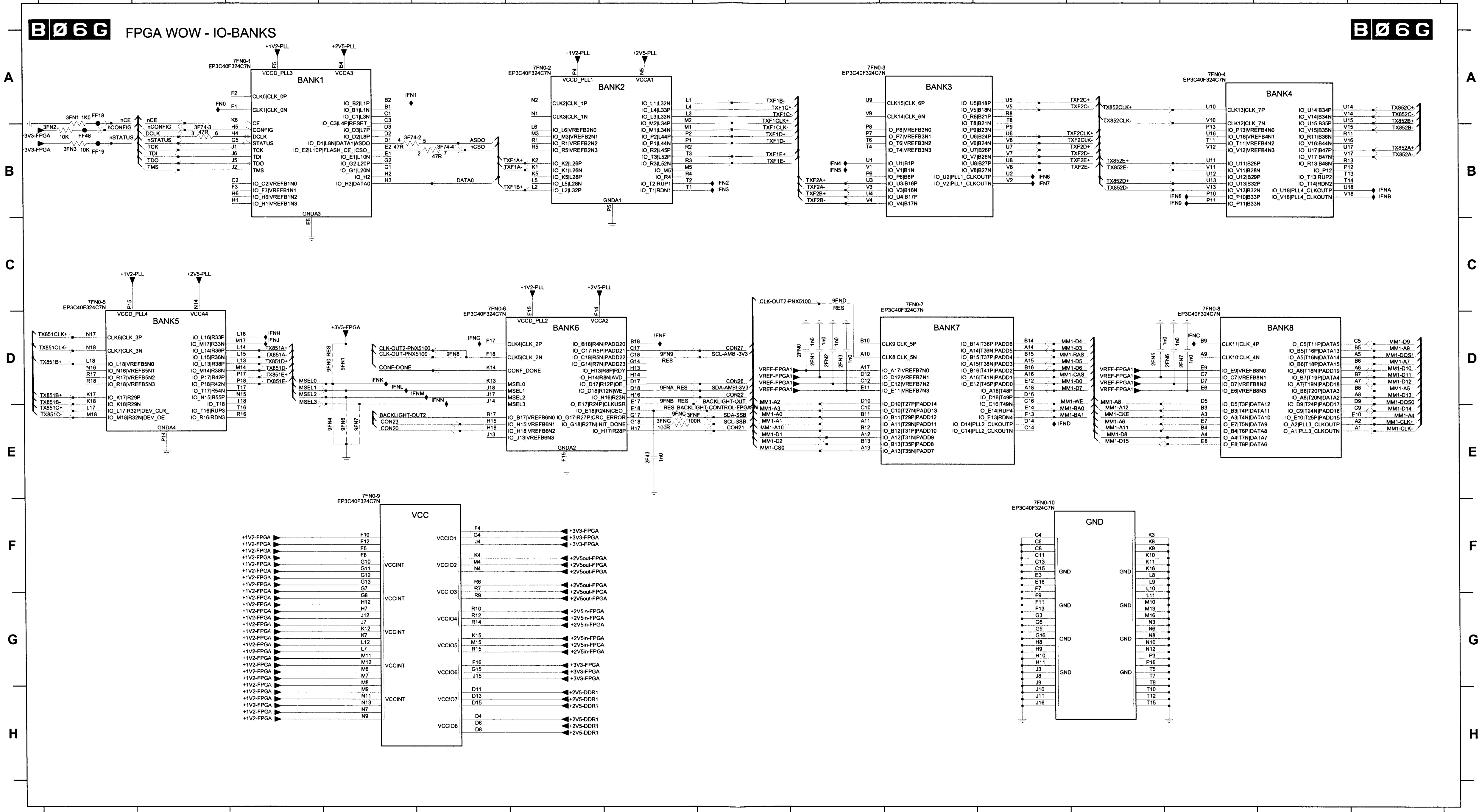
SSB: FPGA WOW - I/O Banks

2F43 E7
2FN0 D9
2FN1 D9
2FN2 D9
2FN3 D9
2FN5 D12
2FN6 D13
2FN7 D13
3F74-2 B4
3F74-3 B2
3F74-4 B5
3FN1 A1
3FN2 B1
3FN3 B1
3FNF E7
3FNG E7
7FN0-1 A3
7FN0-10 F11
7FN0-2 A6
7FN0-3 A10
7FN0-4 A13
7FN0-5 C1
7FN0-6 C5
7FN0-7 C10
7FN0-8 C13
7FN0-9 E4
9FN0 D4
9FN1 D4
9FN4 E4
9FN6 E4
9FN7 E4
9FN8 D5
9FN9 D7
9FNA D7
9FNB D7
9FNC E7
9FND C9
FF18 A1
FF19 B1
FF48 B1
IFN0 A2
IFN1 A4
IFN2 B8
IFN3 B8
IFN4 B9
IFN5 B9
IFN6 B11
IFN7 B11
IFN8 B13
IFN9 B13
IFNA B15
IFNB B15
IFNC D13
IFND E11
IFNF D7
IFNG D5
IFNH D3
IFNJ D3
IFNK D4
IFNL D4
IFNM D5
IFNN D5


B06G
FPGA WOW - IO-BANKS
B06G
7FN0-1
EP3C40F324C7N
BANK1
+1V2-PLL
+2V5-PLL
VCCD_PLL3
VCCA3
GNDA3
7FN0-2
EP3C40F324C7N
BANK2
VCCD_PLL1
VCCA1
GNDA1
7FN0-3
EP3C40F324C7N
BANK3
7FN0-4
EP3C40F324C7N
BANK4
7FN0-5
EP3C40F324C7N
BANK5
VCCD_PLL4
VCCA4
GNDA4
7FN0-6
EP3C40F324C7N
BANK6
VCCD_PLL2
VCCA2
GNDA2
7FN0-7
EP3C40F324C7N
BANK7
7FN0-8
EP3C40F324C7N
BANK8
7FN0-9
EP3C40F324C7N
VCC
VCCINT
7FN0-10
EP3C40F324C7N
GND
+3V3-FPGA
+1V2-FPGA
+2V5out-FPGA
+2V5in-FPGA
+2V5-DDR1
nCE
nCONFIG
nSTATUS
DCLK
TCK
TDI
TDO
TMS
ASDO
nCSO
DATA0
CLK-OUT2-PNX5100
CONF_DONE
BACKLIGHT-OUT2
CON23
CON20
MSEL0
MSEL1
MSEL2
MSEL3
SCL-AMB-3V3
SDA-AMBI-3V3
BACKLIGHT-CONTROL-FPGA
SDA-SSB
SCL-SSB
CON21
CON22
VREF-FPGA1
MM1-A0
MM1-A1
MM1-A2
MM1-A3
MM1-CS0
MM1-DQS0
MM1-DQS1
MM1-CLK+
MM1-CLK-
MM1-RAS
MM1-CAS
MM1-WE
MM1-CKE
TX851CLK+
TX851CLK-
TX852CLK+
TX852CLK-
TXF1CLK+
TXF1CLK-
TXF2CLK+
TXF2CLK-

CHN	SETNAME		
CLASS_NO	FPGA WOW - IO-BANKS TV543 R2 LDIPNX	8204 000 8933	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 8	130 - 7	A2
CHECK	DATE 2007-12-06	© ROYAL PHILIPS ELECTRONICS N.V. 2007	

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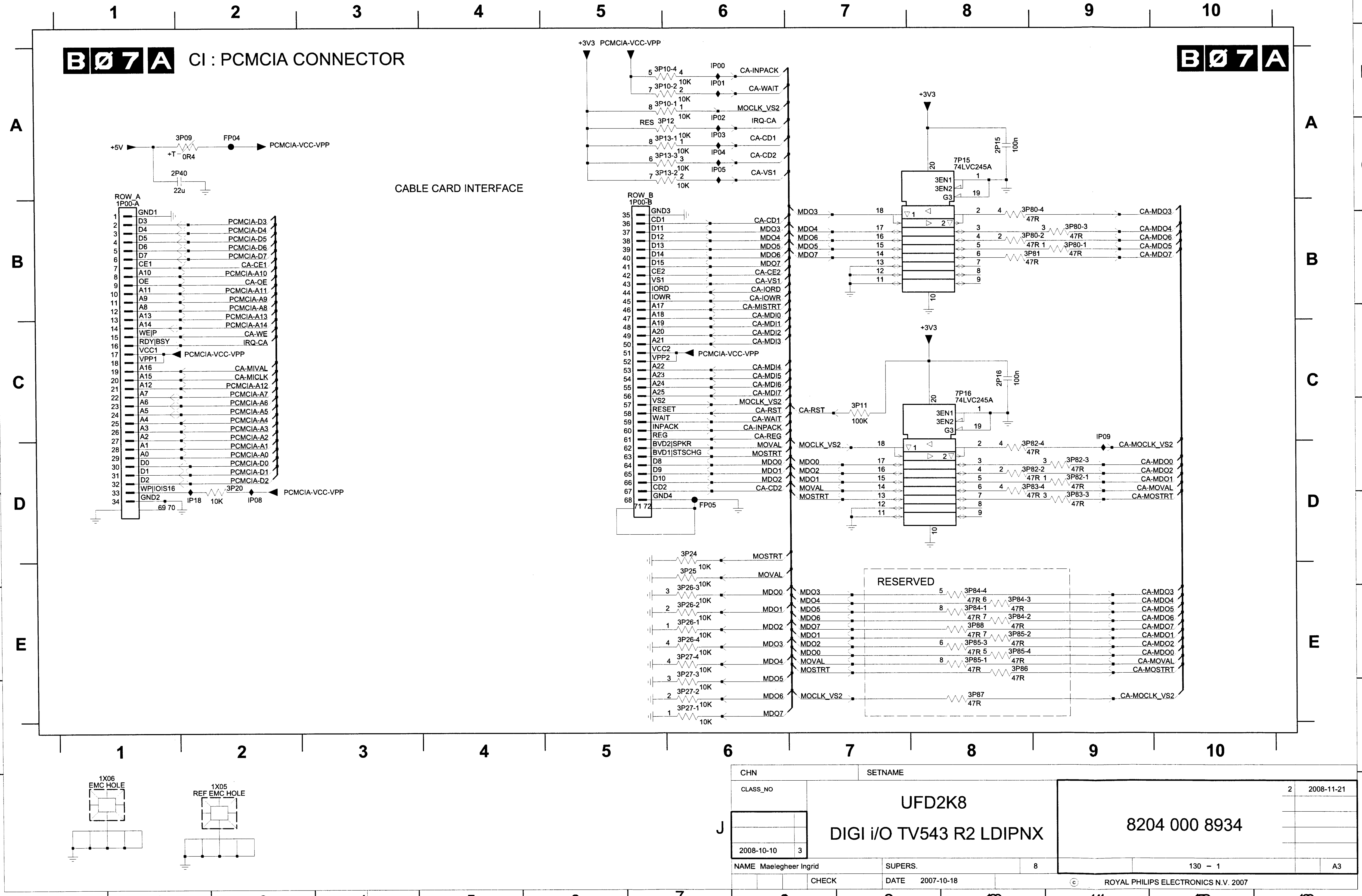
SSB: CI: PCMCIA Connector

1P00-A B1
1P00-B B5
2P15 A8
2P16 C8
2P40 A2
3P09 A2
3P10-1 A6
3P10-2 A6
3P10-4 A6
3P11 C7
3P12 A6
3P13-1 A6
3P13-2 A6
3P13-3 A6
3P20 D2
3P24 D6
3P25 E6
3P26-1 E6
3P26-2 E6
3P26-3 E6
3P26-4 E6
3P27-1 E6
3P27-2 E6
3P27-3 E6
3P27-4 E6
3P80-1 B9
3P80-2 B9
3P80-3 B9
3P80-4 B9
3P81 B9
3P82-1 D9
3P82-2 D9
3P82-3 D9
3P82-4 D9
3P83-3 D9
3P83-4 D9
3P84-1 E8
3P84-2 E8
3P84-3 E8
3P84-4 E8
3P85-1 E8
3P85-2 E8
3P85-3 E8
3P85-4 E8
3P86 E8
3P87 E8
3P88 E8
7P15 A8
7P16 C8
FP04 A2
FP05 D6
IP00 A6
IP01 A6
IP02 A6
IP03 A6
IP04 A6
IP05 A6
IP08 D2
IP09 C9
IP18 D2


B07A CI : PCMCIA CONNECTOR
CABLE CARD INTERFACE
+5V
3P09
0R4
FP04
PCMCIA-VCC-VPP
2P40
22u
ROW_A 1P00-A
ROW_B 1P00-B
+3V3
IP00 IP01 IP02 IP03 IP04 IP05
CA-INPACK
CA-WAIT
MOCLK_VS2
IRQ-CA
CA-CD1
CA-CD2
CA-VS1
3P20
10K
IP18
IP08
FP05
7P15 74LVC245A
7P16 74LVC245A
2P15 100n
2P16 100n
3P11 100K
CA-RST
IP09
CA-MOCLK_VS2
RESERVED
3P87 47R
MOSTRT
MOVAL
MDO0 MDO1 MDO2 MDO3 MDO4 MDO5 MDO6 MDO7
CA-MDO0 CA-MDO1 CA-MDO2 CA-MDO3 CA-MDO4 CA-MDO5 CA-MDO6 CA-MDO7
CA-MOVAL
CA-MOSTRT
1X06 EMC HOLE
1X05 REF EMC HOLE
CHN
SETNAME
CLASS_NO
UFD2K8
DIGI i/O TV543 R2 LDIPNX
8204 000 8934
2 2008-11-21
2008-10-10 3
NAME Maeleghee Ingrid
SUPERS.
CHECK
DATE 2007-10-18
130 - 1
A3
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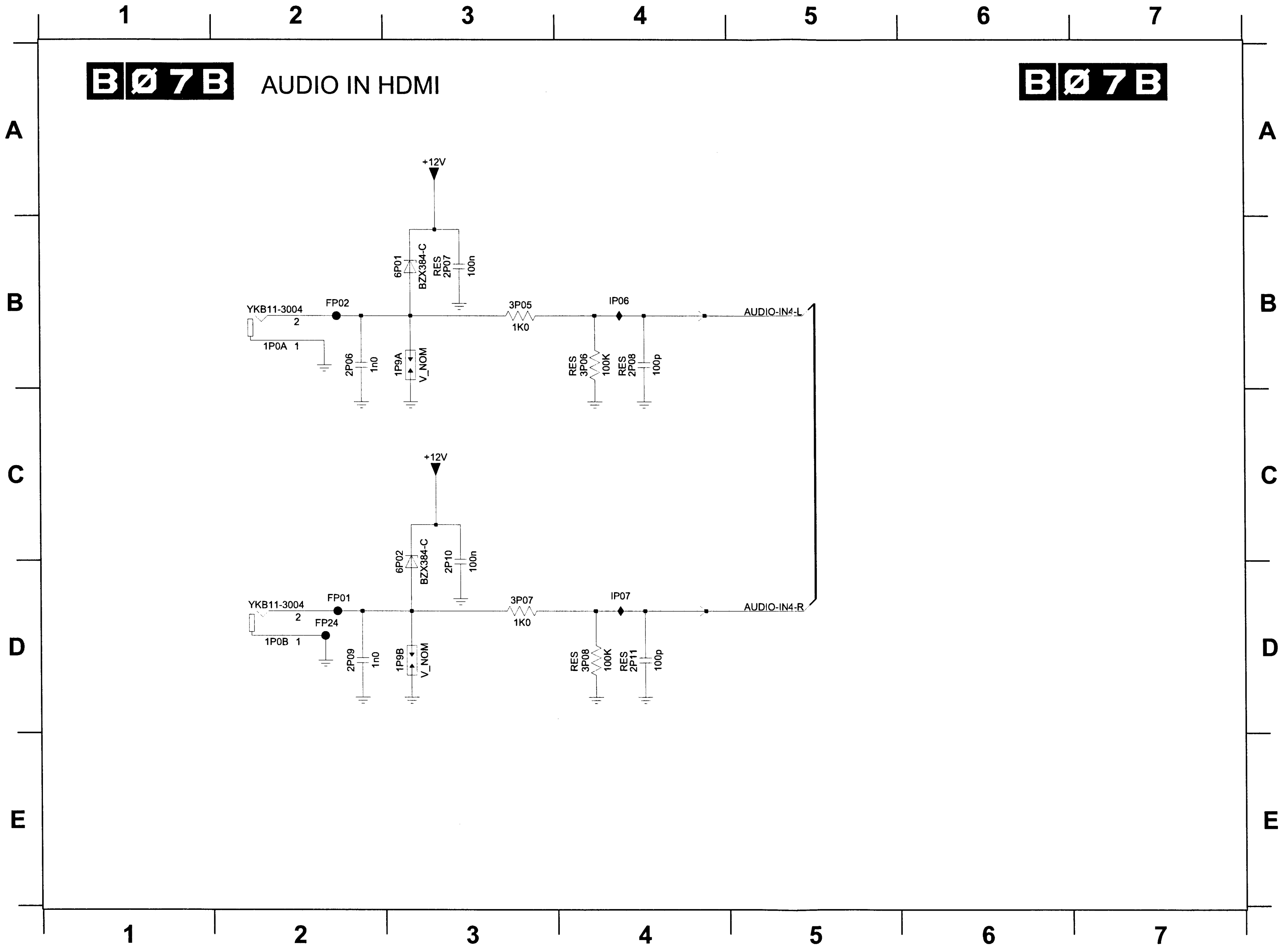
SSB: Audio In HDMI


B07B
AUDIO IN HDMI
B07B
+12V
6P01
BZX384-C
RES
2P07
100n
YKB11-3004
2
FP02
1P0A 1
2P06
1n0
1P9A
V_NOM
3P05
1K0
IP06
RES
3P06
100K
RES
2P08
100p
AUDIO-IN4-L
+12V
6P02
BZX384-C
2P10
100n
YKB11-3004
2
FP01
FP24
1P0B 1
2P09
1n0
1P9B
V_NOM
3P07
1K0
IP07
RES
3P08
100K
RES
2P11
100p
AUDIO-IN4-R
A
B
C
D
E
1
2
3
4
5
6
7

1P0A	B2
1P0B	D2
1P9A	B3
1P9B	D3
2P06	B2
2P07	B3
2P08	B4
2P09	D2
2P10	D3
2P11	D4
3P05	B3
3P06	B4
3P07	D3
3P08	D4
6P01	B3
6P02	D3
FP01	D2
FP02	B2
FP24	D2
IP06	B4
IP07	D4

CHN
SETNAME
CLASS_NO
UFD2K8
DIGI I/O TV543 R2 LDIPNX
8204 000 8934
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid
SUPERS. 8
130 – 2
A3
CHECK
DATE 2007-10-18

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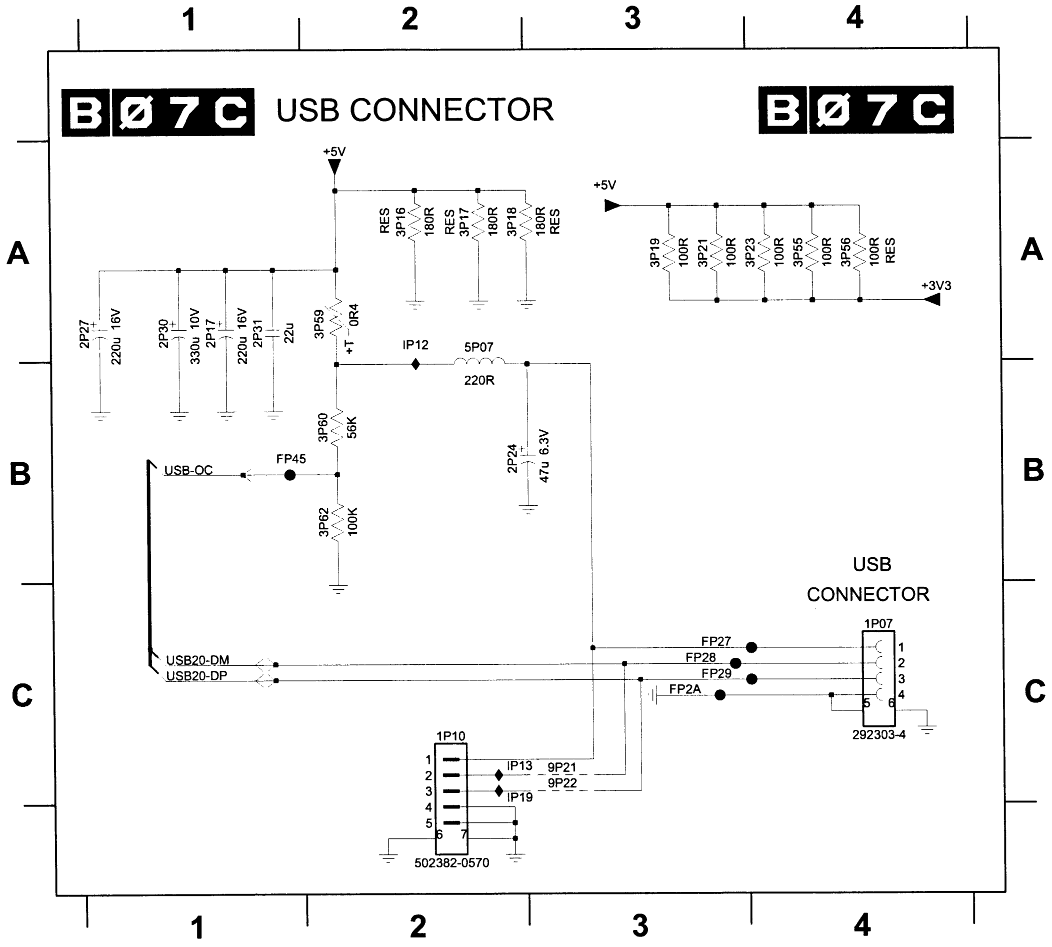
090303

SSB: USB Connector

1P07 C4	2P24 B2	2P31 A1	3P18 A2	3P23 A4	3P59 A2	5P07 A2	FP27 C3	FP2A C3	IP13 C2
1P10 C2	2P27 A1	3P16 A2	3P19 A3	3P55 A4	3P60 B2	9P21 C3	FP28 C3	FP45 B1	IP19 C2
2P17 A1	2P30 A1	3P17 A2	3P21 A3	3P56 A4	3P62 B2	9P22 C3	FP29 C3	IP12 A2	


B07C
USB CONNECTOR
B07C
+5V
RES
3P16
180R
RES
3P17
180R
3P18
180R
RES
+5V
3P19
100R
3P21
100R
3P23
100R
3P55
100R
3P56
100R
RES
+3V3
2P27
220u 16V
2P30
330u 10V
2P17
220u 16V
2P31
22u
3P59
0R4
+T
IP12
5P07
220R
3P60
56K
2P24
47u 6.3V
USB-OC
FP45
3P62
100K
USB
CONNECTOR
1P07
FP27
FP28
FP29
FP2A
USB20-DM
USB20-DP
1
2
3
4
5
6
292303-4
1P10
IP13
9P21
9P22
IP19
7
502382-0570
A
B
C
1
2
3
4

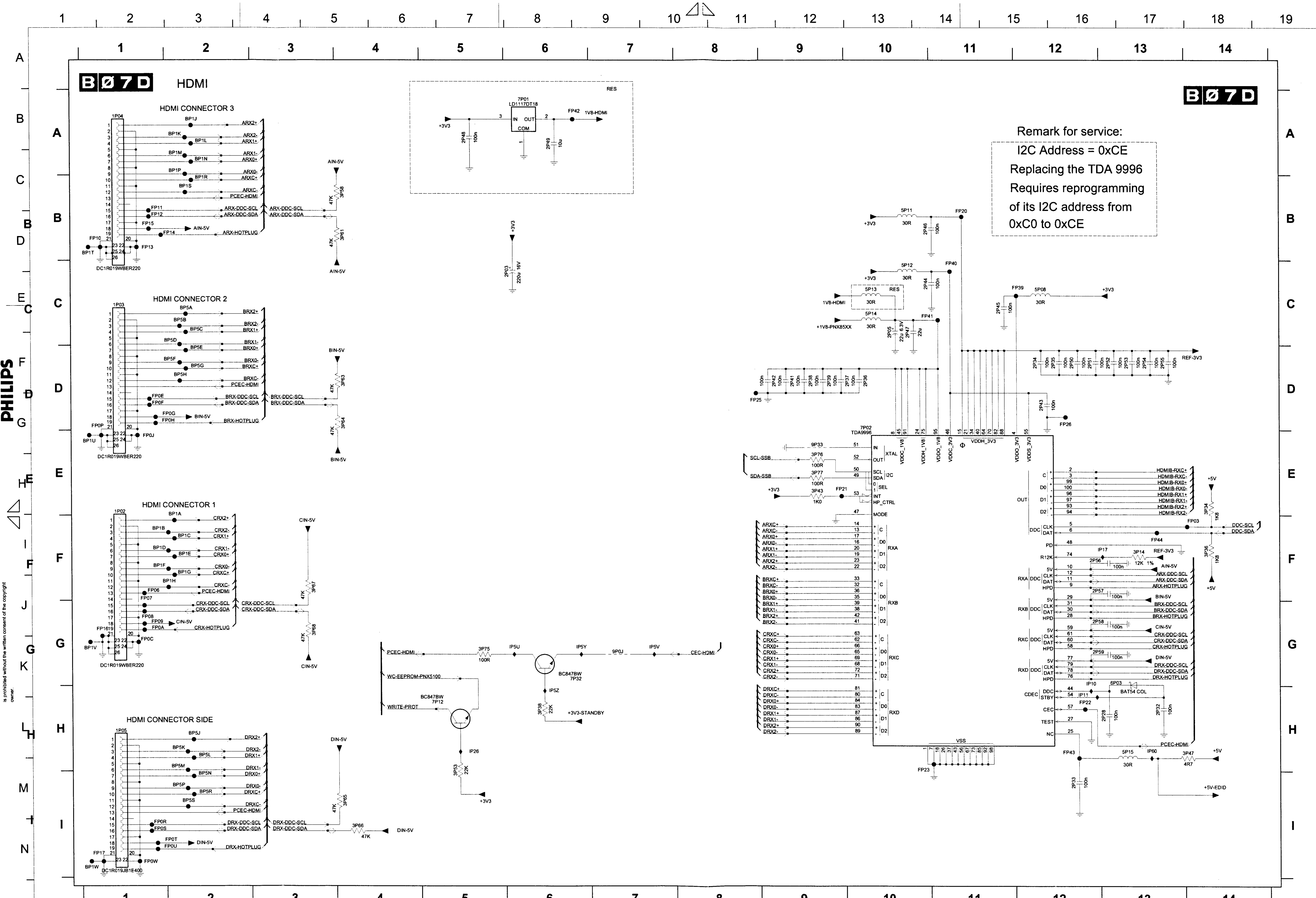
CHN
SETNAME
CLASS_NO
DIGI I/O UFD2K8
TV 543 R2 LDIPNX
8204 000 8934
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid
SUPERS. 8
130 - 3
A4
CHECK
DATE 2007-10-18

18310_536_090303.eps
090303

Personal Notes:

10000_012_090121.eps
090121

SSB: HDMI


B07D
HDMI
HDMI CONNECTOR 3
1P04
DC1R019WBER220
HDMI CONNECTOR 2
1P03
HDMI CONNECTOR 1
1P02
HDMI CONNECTOR SIDE
1P05
DC1R019JB1E400
7P01
LD1117DT18
1V8-HDMI
RES
+3V3
AIN-5V
BIN-5V
CIN-5V
DIN-5V
ARX-DDC-SCL
ARX-DDC-SDA
ARX-HOTPLUG
PCEC-HDMI
CEC-HDMI
WC-EEPROM-PNX5100
WRITE-PROT
BC847BW
7P12
7P32
+3V3-STANDBY
7P02
TDA9996
REF-3V3
SCL-SSB
SDA-SSB
+1V8-PNX85XX
VDDH_3V3
VSS
HDMIB-RXC+
HDMIB-RXC-
DDC-SCL
DDC-SDA
BAT54 COL
+5V
+5V-EDID
1X07
EMC HOLE

Remark for service:

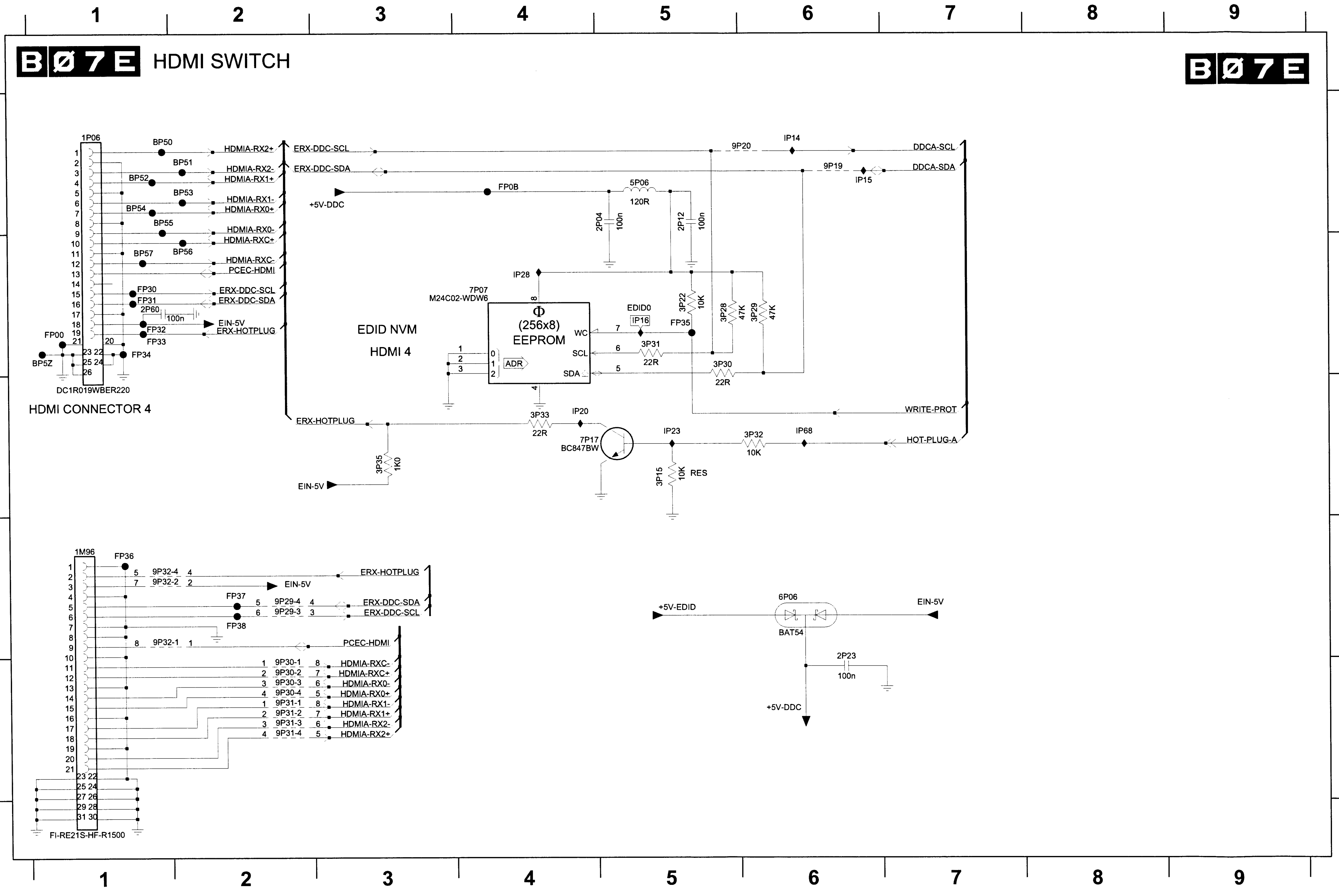
I2C Address = 0xCE
Replacing the TDA 9996
Requires reprogramming
of its I2C address from
0xC0 to 0xCE

1P02	E1
1P03	C1
1P04	A1
1P05	H1
2P03	C6
2P05	C10
2P28	H13
2P32	H13
2P33	I12
2P34	D12
2P35	D12
2P36	D10
2P37	D10
2P38	D9
2P39	D9
2P41	D9
2P42	D9
2P43	D12
2P44	C10
2P45	C11
2P46	B10
2P47	C10
2P48	A5
2P49	A6
2P50	D12
2P51	D12
2P52	D13
2P53	D13
2P54	D13
2P55	D13
2P56	F12
2P57	F12
2P58	G12
2P59	G12
3P14	F13
3P34	E14
3P36	F14
3P38	H6
3P43	E9
3P47	H14
3P53	H5
3P58	B4
3P61	B4
3P63	D4
3P64	D4
3P65	I4
3P66	I4
3P67	F3
3P68	G3
3P75	G5
3P76	E9
3P77	E9
5P08	C12
5P11	B10
5P12	C10
5P13	C10
5P14	C10
5P15	H13
6P03	G13
7P01	A6
7P02	D10
7P12	H5
7P32	G6
9P0J	G7
9P33	E9
BP1A	F2
BP1B	F1
BP1C	F2
BP1D	F1
BP1E	F2
BP1F	F1
BP1G	F2
BP1H	F2
BP1J	A2
BP1K	A2
BP1L	A2
BP1M	A2
BP1N	A2
BP1P	A2
BP1R	B2
BP1S	B2
BP1T	B1
BP1U	E1
BP1V	G1
BP1W	I1
BP5A	C2
BP5B	C2
BP5C	C2
BP5D	C2
BP5E	D2
BP5F	D2
BP5G	D2
BP5H	D2
BP5J	H2
BP5K	H2
BP5L	H2
BP5M	H2
BP5N	I2
BP5P	I2
BP5R	I2
BP5S	I2
FP03	F14
FP06	F1
FP07	F1
FP08	G1
FP09	G1
FP0A	G1
FP0C	G1
FP0E	D1
FP0F	D1
FP0G	D2
FP0H	D2
FP0J	E1
FP0P	D1
FP0R	I1
FP0S	I1
FP0T	I2
FP0U	I2
FP0W	I1
FP10	B1
FP11	B1
FP12	B1
FP13	B1
FP14	B2
FP15	B1
FP16	G1
FP17	I1
FP20	B11
FP21	E9
FP22	H12
FP23	I10
FP25	D8
FP26	D12
FP39	C12
FP40	C11
FP41	C10
FP42	A6
FP43	H12
FP44	F13
IP10	G12
IP11	H12
IP17	F13
IP26	H5
IP5U	G6
IP5V	G7
IP5Y	G6
IP5Z	H6
IP60	H13

CHN	SETNAME			
CLASS_NO	UFD2K8 DIGI IO TV543 R2 LDIPNX	8204 000 8934	2	2008-11-21
2008-10-10	3			
NAME Maelegheer Ingrid	SUPERS.	8	130 - 4	A2
CHECK	DATE 2007-10-18			

18310_537_090303.eps
090303

SSB: HDMI Switch

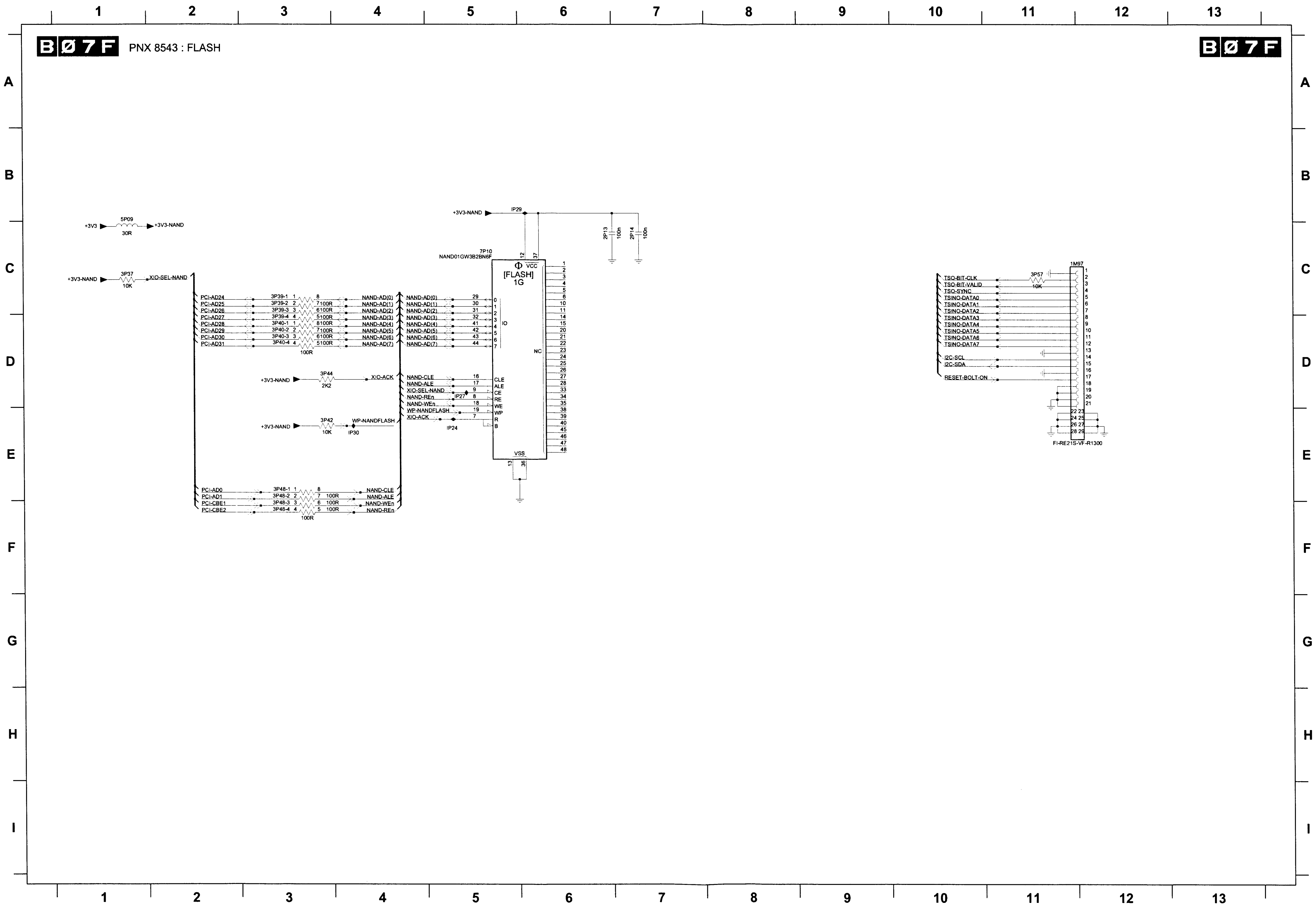

B07E HDMI SWITCH
B07E
1P06
BP50
BP51
BP52
BP53
BP54
BP55
BP56
BP57
HDMIA-RX2+
HDMIA-RX2-
HDMIA-RX1+
HDMIA-RX1-
HDMIA-RX0+
HDMIA-RX0-
HDMIA-RXC+
HDMIA-RXC-
PCEC-HDMI
FP30
FP31
2P60
100n
FP32
FP33
FP34
FP00
BP5Z
ERX-DDC-SCL
ERX-DDC-SDA
EIN-5V
ERX-HOTPLUG
DC1R019WBER220
HDMI CONNECTOR 4
+5V-DDC
FP0B
5P06
120R
2P04
100n
2P12
100n
9P20
IP14
DDCA-SCL
9P19
IP15
DDCA-SDA
IP28
7P07
M24C02-WDW6
Φ
(256x8)
EEPROM
ADR
WC
SCL
SDA
EDID NVM
HDMI 4
EDID0
IP16
FP35
3P22
10K
3P28
47K
3P29
47K
3P31
22R
3P30
22R
WRITE-PROT
3P33
22R
IP20
7P17
BC847BW
IP23
3P32
10K
IP68
HOT-PLUG-A
3P35
1K0
3P15
10K
RES
1M96
FP36
9P32-4
9P32-2
FP37
9P29-4
9P29-3
FP38
9P32-1
9P30-1
9P30-2
9P30-3
9P30-4
9P31-1
9P31-2
9P31-3
9P31-4
FI-RE21S-HF-R1500
+5V-EDID
6P06
BAT54
2P23
100n
EIN-5V
+5V-DDC

1M96	D1
1P06	A1
2P04	A5
2P12	A5
2P23	E6
2P60	B1
3P15	C5
3P22	B5
3P28	B5
3P29	B6
3P30	B5
3P31	B5
3P32	C6
3P33	C4
3P35	C3
5P06	A5
6P06	D6
7P07	B4
7P17	C5
9P19	A6
9P20	A6
9P29-3	D2
9P29-4	D2
9P30-1	E2
9P30-2	E2
9P30-3	E2
9P30-4	E2
9P31-1	E2
9P31-2	E2
9P31-3	E2
9P31-4	E2
9P32-1	D1
9P32-2	D1
9P32-4	D1
BP50	A1
BP51	A2
BP52	A1
BP53	A2
BP54	A1
BP55	A1
BP56	B2
BP57	B1
BP5Z	B1
FP00	B1
FP0B	A4
FP30	B1
FP31	B1
FP32	B1
FP33	B1
FP34	B1
FP35	B5
FP36	D1
FP37	D2
FP38	D2
IP14	A6
IP15	A6
IP16	B5
IP20	C4
IP23	C5
IP28	B4
IP68	C6

CHN
SETNAME
CLASS_NO
UFD2K8
DIGI I/O TV543 R2 LDIPNX
2008-10-10 3
8204 000 8934
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 8
CHECK
DATE 2007-10-18
130 – 5
A3

18310_538_090303.eps
090303

SSB: PNX8543: Flash

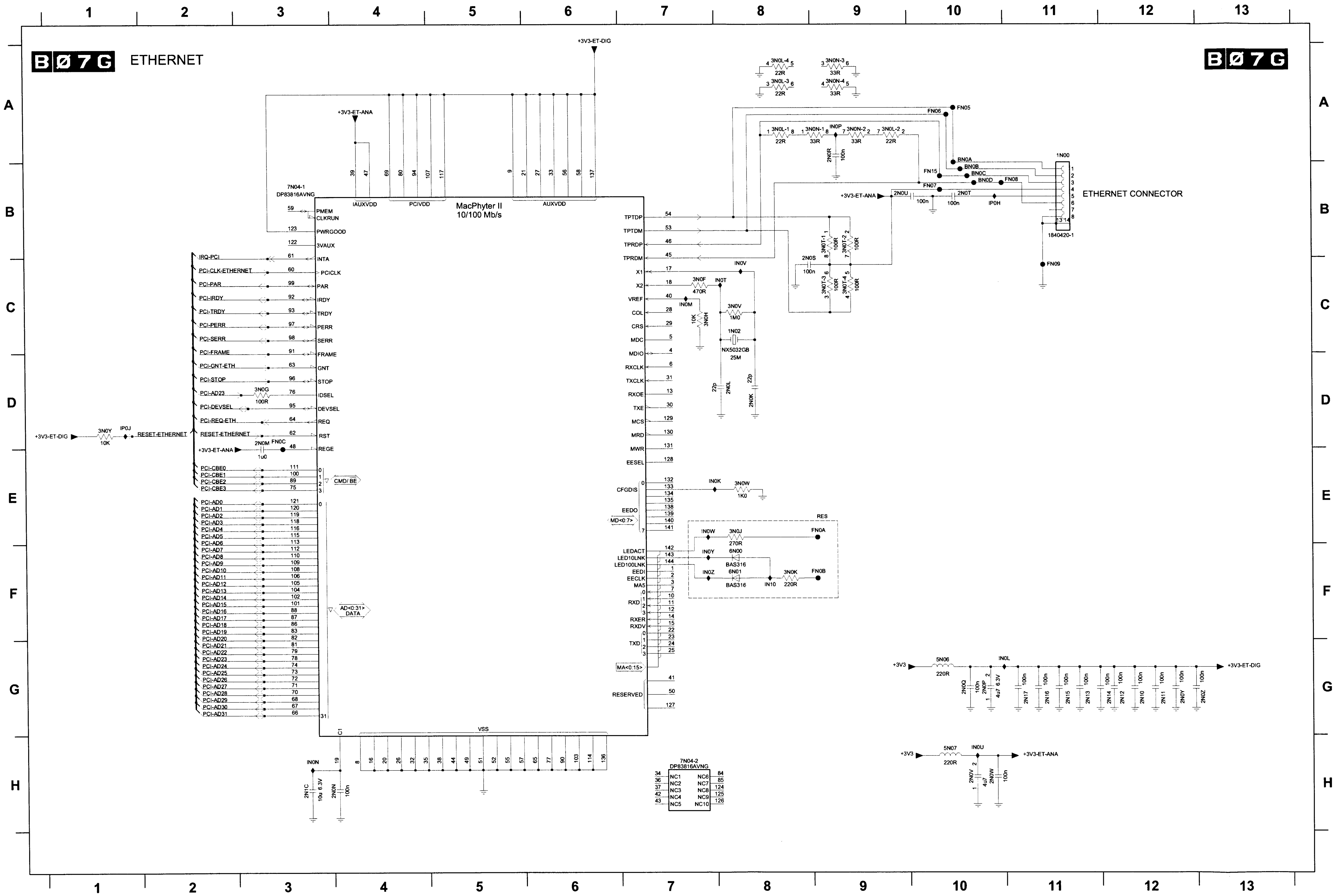

B07F
PNX 8543 : FLASH
B07F
+3V3
5P09
30R
+3V3-NAND
+3V3-NAND
3P37
10K
XIO-SEL-NAND
PCI-AD24
PCI-AD25
PCI-AD26
PCI-AD27
PCI-AD28
PCI-AD29
PCI-AD30
PCI-AD31
3P39-1
3P39-2
3P39-3
3P39-4
3P40-1
3P40-2
3P40-3
3P40-4
100R
7100R
6100R
5100R
8100R
NAND-AD(0)
NAND-AD(1)
NAND-AD(2)
NAND-AD(3)
NAND-AD(4)
NAND-AD(5)
NAND-AD(6)
NAND-AD(7)
+3V3-NAND
3P44
2K2
XIO-ACK
+3V3-NAND
3P42
10K
IP30
WP-NANDFLASH
PCI-AD0
PCI-AD1
PCI-CBE1
PCI-CBE2
3P48-1
3P48-2
3P48-3
3P48-4
100R
NAND-CLE
NAND-ALE
NAND-WEn
NAND-REn
NAND-CLE
NAND-ALE
XIO-SEL-NAND
NAND-REn
NAND-WEn
WP-NANDFLASH
XIO-ACK
IP27
IP24
+3V3-NAND
IP29
7P10
NAND01GW3B2BN6F
VCC
[FLASH]
1G
IO
NC
CLE
ALE
CE
RE
WE
WP
R
B
VSS
2P13
100n
2P14
100n
TSO-BIT-CLK
TSO-BIT-VALID
TSO-SYNC
TSINO-DATA0
TSINO-DATA1
TSINO-DATA2
TSINO-DATA3
TSINO-DATA4
TSINO-DATA5
TSINO-DATA6
TSINO-DATA7
I2C-SCL
I2C-SDA
RESET-BOLT-ON
3P57
10K
1M97
FI-RE21S-VF-R1300

1M97	C12
2P13	C6
2P14	C7
3P37	C1
3P39-1	C3
3P39-2	C3
3P39-3	C3
3P39-4	D3
3P40-1	D3
3P40-2	D3
3P40-3	D3
3P40-4	D3
3P42	E3
3P44	D3
3P48-1	E3
3P48-2	E3
3P48-3	F3
3P48-4	F3
3P57	C11
5P09	B1
7P10	C5
IP24	E5
IP27	D5
IP29	B5
IP30	E4

CHN
SETNAME
CLASS_NO
UFD 2K8
DIGI I/O TV543 R2 LDIPNX
8204 000 8934
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid
SUPERS. 8
130 - 6
A2
CHECK
DATE 2007-10-18

18310_539_090303.eps
090303

SSB: Ethernet


B07G
ETHERNET
+3V3-ET-DIG
+3V3-ET-ANA
7N04-1
DP83816AVNG
MacPhyter II
10/100 Mb/s
IAUXVDD
PCIVDD
AUXVDD
PMEM
CLKRUN
PWRGOOD
3VAUX
INTA
PCICLK
PAR
IRDY
TRDY
PERR
SERR
FRAME
GNT
STOP
IDSEL
DEVSEL
REQ
RST
REGE
IRQ-PCI
PCI-CLK-ETHERNET
PCI-PAR
PCI-IRDY
PCI-TRDY
PCI-PERR
PCI-SERR
PCI-FRAME
PCI-GNT-ETH
PCI-STOP
PCI-AD23
PCI-DEVSEL
PCI-REQ-ETH
RESET-ETHERNET
CMD/BE
AD<0:31>
DATA
PCI-CBE0
PCI-CBE1
PCI-CBE2
PCI-CBE3
PCI-AD0 … PCI-AD31
TPTDP
TPTDM
TPRDP
TPRDM
X1
X2
VREF
COL
CRS
MDC
MDIO
RXCLK
TXCLK
RXOE
TXE
MCS
MRD
MWR
EESEL
CFGDIS
EEDO
MD<0:7>
LEDACT
LED10LNK
LED100LNK
EEDI
EECLK
MA5
RXD
RXER
RXDV
TXD
MA<0:15>
RESERVED
VSS
1N02
NX5032GB
25M
RES
BAS316
ETHERNET CONNECTOR
1N00
1840420-1
5N06
5N07
220R
+3V3
7N04-2
DP83816AVNG
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10

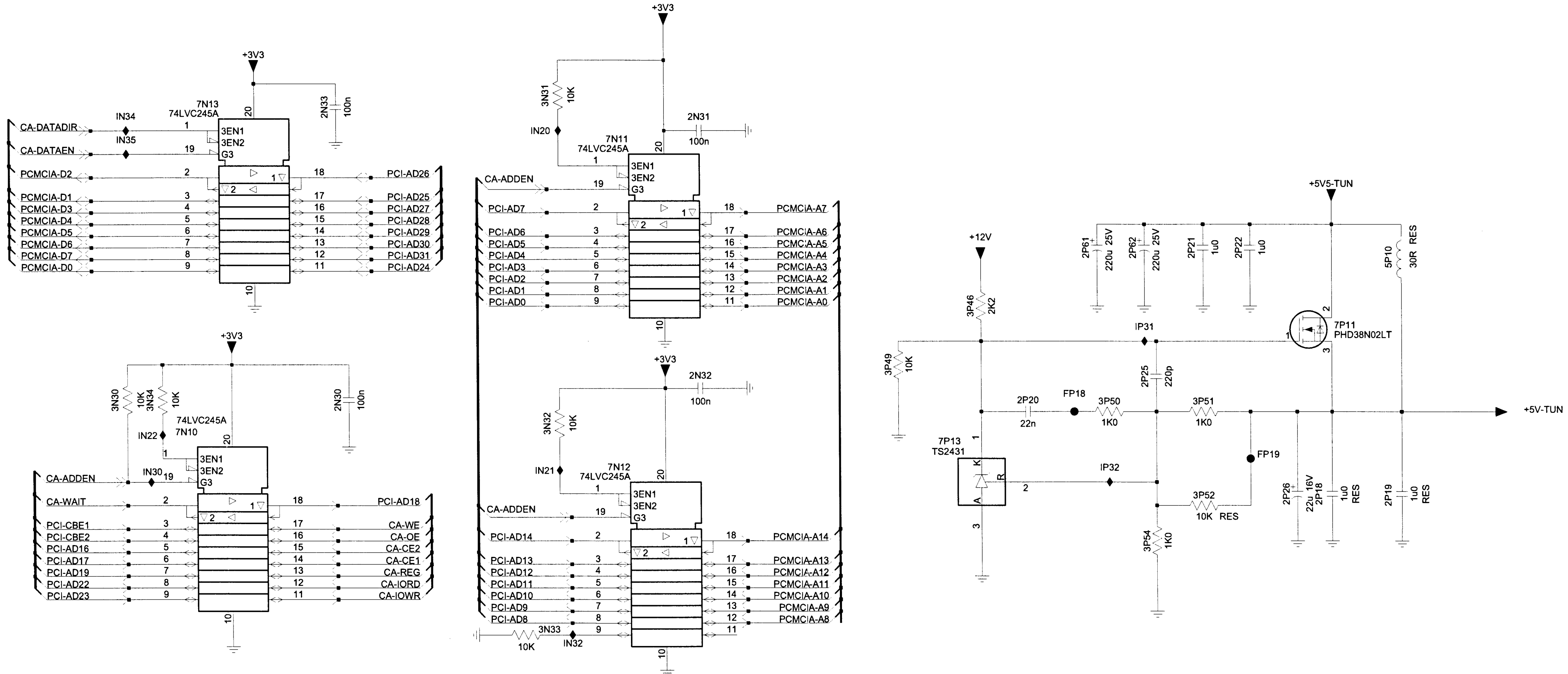
1N00	A11
1N02	C8
2N0K	D8
2N0L	D8
2N0M	D3
2N0N	H4
2N0P	G10
2N0Q	G10
2N0R	A9
2N0S	C8
2N0T	B10
2N0U	B9
2N0V	H10
2N0W	H10
2N0Y	G12
2N0Z	G13
2N10	G12
2N11	G12
2N12	G12
2N13	G11
2N14	G12
2N15	G11
2N16	G11
2N17	G11
2N1C	H3
3N0F	C7
3N0G	D3
3N0H	C7
3N0J	E8
3N0K	F8
3N0L-1	A8
3N0L-2	A9
3N0L-3	A8
3N0L-4	A8
3N0N-1	A9
3N0N-2	A9
3N0N-3	A9
3N0N-4	A9
3N0T-1	B9
3N0T-2	B9
3N0T-3	C9
3N0T-4	C9
3N0V	C8
3N0W	E8
3N0Y	D1
5N06	G10
5N07	H10
6N00	F8
6N01	F8
7N04-1	B3
7N04-2	H7
BN0A	A10
BN0B	B10
BN0C	B10
BN0D	B10
FN05	A10
FN06	A10
FN07	B10
FN08	B11
FN09	C11
FN0A	E9
FN0B	F9
FN0C	D3
FN15	B10
IN0K	E7
IN0L	G10
IN0M	C7
IN0N	H3
IN0P	A9
IN0T	C8
IN0U	H10
IN0V	C8
IN0W	E7
IN0Y	F7
IN0Z	F7
IN10	F8
IP0H	B10
IP0J	D1

CHN
SETNAME
CLASS_NO
2008-10-10 3
UFD 2K8
DIGI I/O TV543 R2 LDIPNX
8204 000 8934
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 8
130 – 7
A2
CHECK
DATE 2007-10-18

18310_540_090303.eps
090303

SSB: Buffering

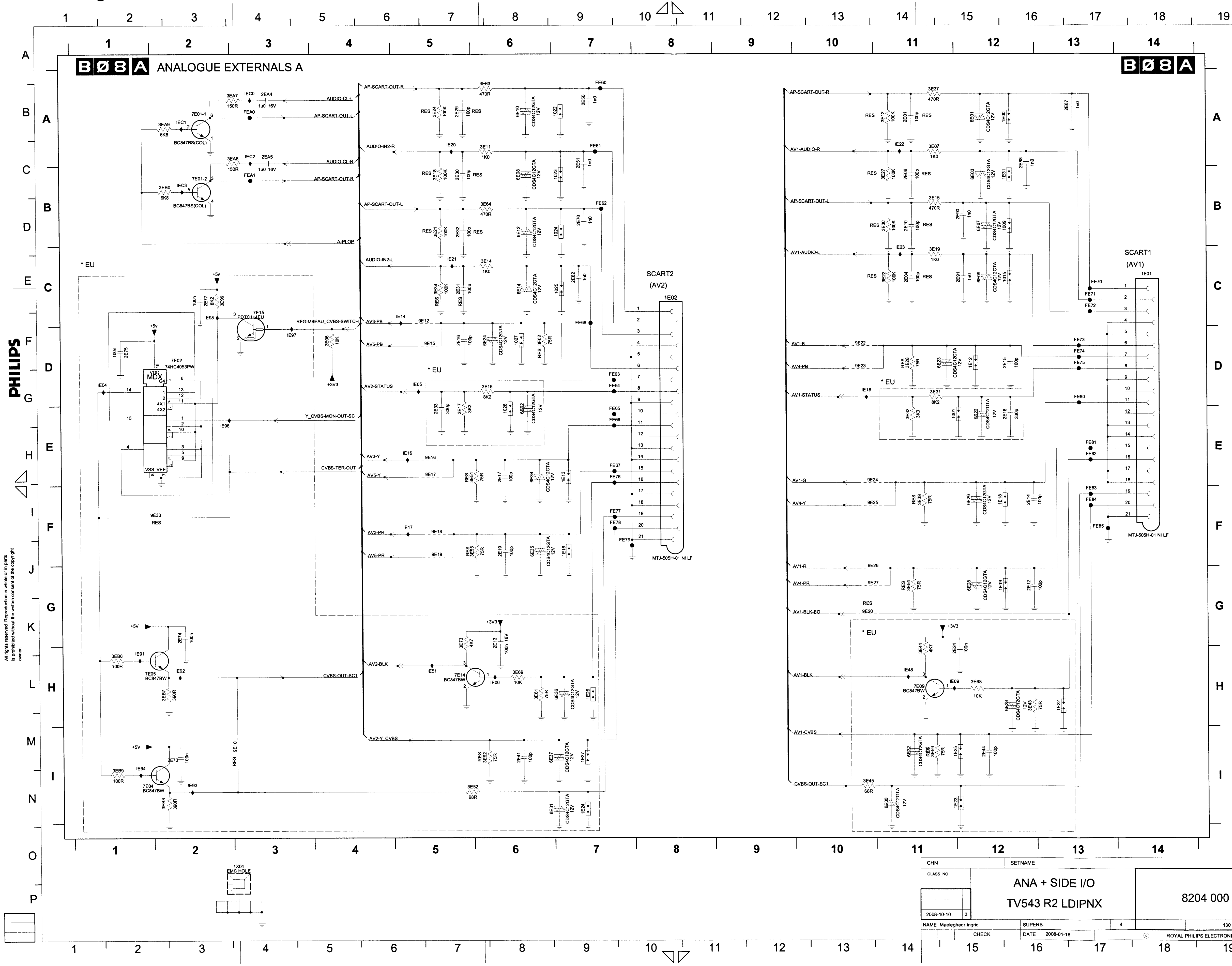
B07H BUFFERING


+3V3
7N13
74LVC245A
IN34
IN35
CA-DATADIR
CA-DATAEN
3EN1
3EN2
G3
2N33
100n
PCMCIA-D2
PCMCIA-D1
PCMCIA-D3
PCMCIA-D4
PCMCIA-D5
PCMCIA-D6
PCMCIA-D7
PCMCIA-D0
PCI-AD26
PCI-AD25
PCI-AD27
PCI-AD28
PCI-AD29
PCI-AD30
PCI-AD31
PCI-AD24
3N30
10K
3N34
10K
74LVC245A
7N10
IN22
IN30
2N30
100n
CA-ADDEN
CA-WAIT
PCI-CBE1
PCI-CBE2
PCI-AD16
PCI-AD17
PCI-AD19
PCI-AD22
PCI-AD23
PCI-AD18
CA-WE
CA-OE
CA-CE2
CA-CE1
CA-REG
CA-IORD
CA-IOWR
3N31
10K
IN20
7N11
74LVC245A
2N31
100n
PCI-AD7
PCI-AD6
PCI-AD5
PCI-AD4
PCI-AD3
PCI-AD2
PCI-AD1
PCI-AD0
PCMCIA-A7
PCMCIA-A6
PCMCIA-A5
PCMCIA-A4
PCMCIA-A3
PCMCIA-A2
PCMCIA-A1
PCMCIA-A0
2N32
100n
3N32
10K
IN21
7N12
74LVC245A
PCI-AD14
PCI-AD13
PCI-AD12
PCI-AD11
PCI-AD10
PCI-AD9
PCI-AD8
3N33
10K
IN32
PCMCIA-A14
PCMCIA-A13
PCMCIA-A12
PCMCIA-A11
PCMCIA-A10
PCMCIA-A9
PCMCIA-A8
+12V
3P46
2K2
3P49
10K
IP31
2P61
220u 25V
2P62
220u 25V
2P21
1u0
2P22
1u0
+5V5-TUN
5P10
30R RES
7P11
PHD38N02LT
2P25
220p
2P20
22n
FP18
3P50
1K0
3P51
1K0
+5V-TUN
FP19
7P13
TS2431
K
R
A
IP32
3P52
10K RES
3P54
1K0
2P26
22u 16V
2P18
1u0
RES
2P19
1u0
RES

2N30	D3
2N31	B5
2N32	D5
2N33	B3
2P18	E9
2P19	E9
2P20	D7
2P21	C8
2P22	C8
2P25	D8
2P26	E9
2P61	C7
2P62	C8
3N30	D1
3N31	B4
3N32	D4
3N33	E4
3N34	D2
3P46	C7
3P49	D6
3P50	D8
3P51	D8
3P52	E8
3P54	E8
5P10	C9
7N10	D2
7N11	B5
7N12	D5
7N13	B2
7P11	D9
7P13	D7
FP18	D7
FP19	D8
IN20	B4
IN21	D4
IN22	D2
IN30	D2
IN32	E4
IN34	B2
IN35	B2
IP31	D8
IP32	D8

CHN
SETNAME
CLASS_NO
UFD 2K8
DIGI I/O TV543 R2 LDIPNX
2008-10-10 3
8204 000 8934
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 8
130 - 8
A3
CHECK
DATE 2007-10-18

SSB: Analogue Externals A


B08A ANALOGUE EXTERNALS A
AP-SCART-OUT-R
AP-SCART-OUT-L
AUDIO-CL-L
AUDIO-CL-R
AUDIO-IN2-R
AUDIO-IN2-L
A-PLOP
7E01-1
7E01-2
BC847BS(COL)
* EU
7E02
74HC4053PW
7E15
PDTC114EU
REGIMBEAU_CVBS-SWITCH
Y_CVBS-MON-OUT-SC
CVBS-TER-OUT
CVBS-OUT-SC1
AV3-PB
AV5-PB
AV2-STATUS
AV3-Y
AV5-Y
AV3-PR
AV5-PR
AV2-BLK
AV2-Y_CVBS
7E05 BC847BW
7E04 BC847BW
7E14 BC847BW
SCART2
(AV2)
1E02
MTJ-505H-01 NI LF
SCART1
(AV1)
1E01
AV1-AUDIO-R
AV1-AUDIO-L
AV1-B
AV4-PB
AV1-STATUS
AV1-G
AV4-Y
AV1-R
AV4-PR
AV1-BLK-BO
AV1-BLK
AV1-CVBS
CVBS-OUT-SC1
7E09 BC847BW
+3V3
+5V
CDS4C12GTA
1X04
EMC HOLE

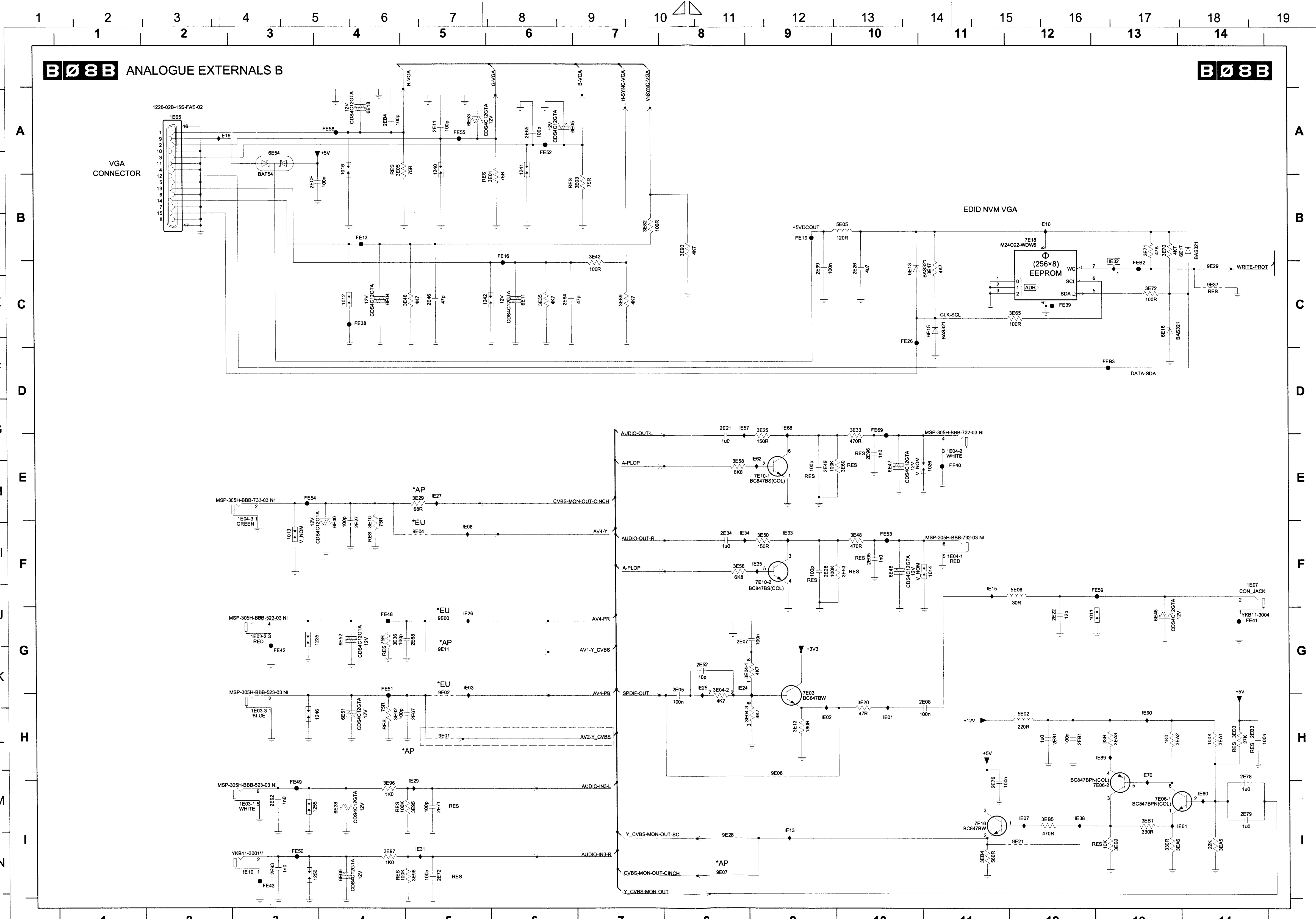
1001 E11
1009 B12
1015 C12
1022 A7
1023 B7
1024 B7
1025 C7
1027 D6
1028 E6
1E00 A12
1E01 C14
1E02 C8
1E12 D12
1E13 E7
1E16 F7
1E18 F12
1E19 G12
1E22 H13
1E23 I11
1E24 I7
1E25 I11
1E26 H7
1E27 I7
1E31 B12
2E01 A11
2E04 C11
2E06 B11
2E10 B11
2E12 G12
2E13 G6
2E14 F12
2E15 D12
2E16 D5
2E17 E6
2E18 E12
2E19 F6
2E24 H11
2E29 A5
2E30 B5
2E31 C5
2E32 B5
2E33 E5
2E41 I6
2E44 I12
2E50 A7
2E51 A7
2E70 B7
2E73 I2
2E74 G2
2E75 D1
2E77 C2
2E82 C7
2E87 A13
2E88 A12
2E90 B12
2E91 C12
2EA4 A3
2EA5 A3
3E02 D6
3E06 D4
3E07 A11
3E11 A6
3E12 A11
3E14 C6
3E15 B11
3E16 D6
3E17 E5
3E18 B5
3E19 C11
3E21 B5
3E22 C11
3E24 A5
3E27 B11
3E28 D11
3E30 B11
3E31 D11
3E32 E11
3E34 C5
3E37 A11
3E38 F11
3E43 H12
3E44 H11
3E45 I10
3E51 E5
3E52 I5
3E54 G11
3E55 F5
3E59 I11
3E61 H6
3E62 I6
3E63 A6
3E64 B6
3E68 H12
3E69 H6
3E73 G5
3E99 C2
3EA7 A3
3EA8 A3
3EA9 A2
3EB0 B2
3EB6 H1
3EB7 H2
3EB8 I2
3EB9 I1
6E01 A12
6E02 E6
6E03 B12
6E07 B12
6E08 B6
6E09 C12
6E10 A6
6E12 B6
6E14 C6
6E22 E12
6E23 D11
6E24 D6

6E26 F12
6E28 G12
6E29 H12
6E30 I11
6E31 I6
6E32 I11
6E34 E6
6E35 F6
6E36 H7
6E37 I6
7E01-1 A2
7E01-2 B2
7E02 D2
7E04 I1
7E05 H1
7E09 H11
7E14 H5
7E15 C3
9E10 I3
9E12 C5
9E15 D5
9E16 E5
9E17 E5
9E18 F5
9E19 F5
9E20 G10
9E22 D10
9E23 D10
9E24 E10
9E25 F10
9E26 G10
9E27 G10
9E33 F2
FE60 A7
FE61 A7
FE62 B7
FE63 D7
FE64 D7
FE65 E7
FE66 E7
FE67 E7
FE68 C7
FE70 C13
FE71 C13
FE72 C13
FE73 D13
FE74 D13
FE75 D13
FE76 E7
FE77 F7
FE78 F7
FE79 F7
FE80 D13
FE81 E13
FE82 E13
FE83 F13
FE84 F13
FE85 F13
FEA0 A3
FEA1 B3
IE04 D1
IE05 D5
IE06 H6
IE09 H11
IE14 C5
IE16 E5
IE17 F5
IE18 D10
IE20 A5
IE21 C5
IE22 A11
IE23 C11
IE48 H11
IE51 H5
IE91 H1
IE92 H2
IE93 I2
IE94 I1
IE96 E2
IE97 D3
IE98 C2
IEC0 A3
IEC1 A2
IEC2 A3
IEC3 B2

CHN	SETNAME		
CLASS_NO	ANA + SIDE I/O TV543 R2 LDIPNX	8204 000 8930	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 4	130 – 1	A2
CHECK	DATE 2008-01-18		

18310_542_090303.eps
090303

SSB: Analogue Externals B


B08B
ANALOGUE EXTERNALS B
VGA CONNECTOR
1226-02B-15S-FAE-02
1E05
IE19
6E54
BAT54
+5V
2ECF 100n
FE58
FE55
FE52
FE13
FE16
FE38
R-VGA
G-VGA
B-VGA
H-SYNC-VGA
V-SYNC-VGA
CDS4C12GTA 12V
6E18
6E53
6E05
6E04
6E11
2EB4 100p
2E11 100p
2E65 100p
1016
1240
1241
1012
1242
RES 3E05 75R
RES 3E01 75R
RES 3E03 75R
3E82 100R
3E90 4K7
3E42 100R
3E46 4K7
2E46 47p
3E35 4K7
2E64 47p
3E89 4K7
EDID NVM VGA
+5VDCOUT
FE19
5E05 120R
2E99 100n
2E26 4u7
6E13 BAS321
3E47 4K7
IE10
7E18 M24C02-WDW6
(256×8) EEPROM
WC SCL SDA ADR
FE39
IE32
FEB2
3E71 47K
3E70 4K7
6E17 BAS321
9E29
WRITE-PROT
9E37 RES
3E72 100R
CLK-SCL
3E65 100R
FE26
6E15 BAS321
6E16 BAS321
FEB3
DATA-SDA
AUDIO-OUT-L
A-PLOP
2E21 1u0
IE57
3E25 150R
IE68
3E58 6K8
IE62
7E10-1 BC847BS(COL)
100p 2E49 RES
100K 3E60 RES
3E33 470R
FE69
RES 2E96 1n0
6E47 CDS4C12GTA 12V
V_NOM 1026
MSP-305H-BBB-732-03 NI
1E04-2 WHITE
FE40
AUDIO-OUT-R
2E34 1u0
IE34
3E50 150R
IE33
3E56 6K8
IE35
7E10-2 BC847BS(COL)
2E28
3E53
3E48 470R
FE53
RES 2E95 1n0
6E48
1014
1E04-1 RED
MSP-305H-BBB-732-03 NI
FE54
1E04-3 GREEN
1013 V_NOM
6E40
2E27
RES 3E10 75R
*AP 3E29 68R
IE27
CVBS-MON-OUT-CINCH
*EU 9E04
IE08
AV4-Y
MSP-305H-BBB-523-03 NI
1E03-2 RED
FE42
1235
FE48
2E52
6E52
3E36 100R
2E68
75R
*EU 9E00
IE26
AV4-PR
*AP 9E11
AV1-Y_CVBS
1E03-3 BLUE
1246
FE51
6E51
3E92 100R
2E67
*EU 9E02
IE03
AV4-PB
9E01
AV2-Y_CVBS
*AP
MSP-305H-BBB-523-03 NI
1E03-1 WHITE
FE49
2E92 1n0
1255
6E38
3E96 1K0
IE29
RES 3E95 100K
2E71 100p RES
AUDIO-IN3-L
YKB11-3001V
1E10
FE50
FE43
2E93 1n0
1250
6E06
3E97 1K0
IE31
RES 3E98 100K
2E72 100p RES
AUDIO-IN3-R
2E07 100n
+3V3
2E52 10p
SPDIF-OUT
2E05 100n
IE25
3E04-2 4K7
IE24
3E04-1 4K7
3E04-3 4K7
7E03 BC847BW
3E13 180R
IE02
3E20 47R
IE01
2E08 100n
9E06
IE15
5E06 30R
FE59
2E22 12p
1011
6E46 CDS4C12GTA 12V
1E07 CON_JACK
YKB11-3004
FE41
+12V
5E02 220R
2E81 1u0
2EB1 100n
33R 3EA3
IE89
IE90
1K0 3EA2
100K 3EA1
3ED3 27K
RES 2EB3 100n
+5V
2E76 100n
BC847BPN(COL) 7E06-2
IE70
7E06-1 BC847BPN(COL)
IE60
2E78 1u0
2E79 1u0
7E16 BC847BW
IE07
3EB5 470R
IE38
3EB1 330R
IE61
RES 3EB2
330R 3EA6
22K 3EA5
3EB4 560R
9E21
Y_CVBS-MON-OUT-SC
9E28
IE13
CVBS-MON-OUT-CINCH
*AP 9E07
Y_CVBS-MON-OUT
B08B

1011	G12
1012	C4
1013	F3
1014	F11
1016	A4
1026	E11
1235	G3
1240	A5
1241	A6
1242	C5
1246	H3
1250	I3
1255	I3
1E03-1	I3
1E03-2	G3
1E03-3	H3
1E04-1	F11
1E04-2	E11
1E04-3	E3
1E05	A2
1E07	F14
1E10	I3
2E05	G8
2E07	G8
2E08	H11
2E11	A5
2E21	D8
2E22	G12
2E26	C10
2E27	F4
2E28	F9
2E34	F8
2E46	C5
2E49	E9
2E52	G8
2E64	C6
2E65	A6
2E67	H5
2E68	G5
2E71	I5
2E72	I5
2E76	I11
2E78	H14
2E79	I14
2E81	H12
2E92	I3
2E93	I3
2E95	F10
2E96	E10
2E99	C9
2EB1	H12
2EB3	H14
2EB4	A4
2ECF	B3
3E01	B6
3E03	B7
3E04-1	G8
3E04-2	G8
3E04-3	H8
3E05	A4
3E10	F4
3E13	H9
3E20	H10
3E25	D9
3E29	E5
3E33	D10
3E35	C6
3E36	G4
3E42	B7
3E46	C5
3E47	C11
3E48	F10
3E50	F9
3E53	F10
3E56	F8
3E58	E8
3E60	E10
3E65	C12
3E70	B13
3E71	B13
3E72	C13
3E82	B7
3E89	C7
3E90	B8
3E92	H4
3E95	I5
3E96	I4
3E97	I4
3E98	I5
3EA1	H14
3EA2	H13
3EA3	H13
3EA5	I14
3EA6	I13
3EB1	I13
3EB2	I13
3EB4	I11
3EB5	I12
3ED3	H14
5E02	H12
5E05	B10
5E06	F12
6E04	C4
6E05	A7
6E06	I4
6E11	C6
6E13	C10
6E15	C11
6E16	C13
6E17	B14
6E18	A4
6E38	I4
6E40	F4
6E46	G13
6E47	E10
6E48	F10
6E51	H4
6E52	G4
6E53	A5
6E54	A3
7E03	H9
7E06-1	I13
7E06-2	I13
7E10-1	E9
7E10-2	F9
7E16	I11
7E18	B12
9E00	G5
9E01	H5
9E02	H5
9E04	F5
9E06	H9
9E07	I8
9E11	G5
9E21	I12
9E28	I8
9E29	C14
9E37	C14
FE13	B4
FE16	B6
FE19	B9
FE26	C10
FE38	C4
FE39	C12
FE40	E11
FE41	G14
FE42	G3
FE43	I3
FE48	G4
FE49	I3
FE50	I3
FE51	G4
FE52	A6
FE53	F10
FE54	E3
FE55	A5
FE58	A4
FE59	F13
FE69	D10
FEB2	C13
FEB3	D13
IE01	H10
IE02	H9
IE03	G5
IE07	I12
IE08	F5
IE10	B12
IE13	I9
IE15	F11
IE19	A2
IE24	G8
IE25	G8
IE26	G5
IE27	E5
IE29	I5
IE31	I5
IE32	C13
IE33	F9
IE34	F8
IE35	F9
IE38	I12
IE57	D8
IE60	I14
IE61	I14
IE62	E9
IE68	D9
IE70	H13
IE89	H13
IE90	H13

CHN	SETNAME		
CLASS_NO	ANA + SIDE I/O TV543 R2 LDIPNX	8204 000 8930	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 4	130 – 2	A2
CHECK	DATE 2008-01-18		

PHILIPS

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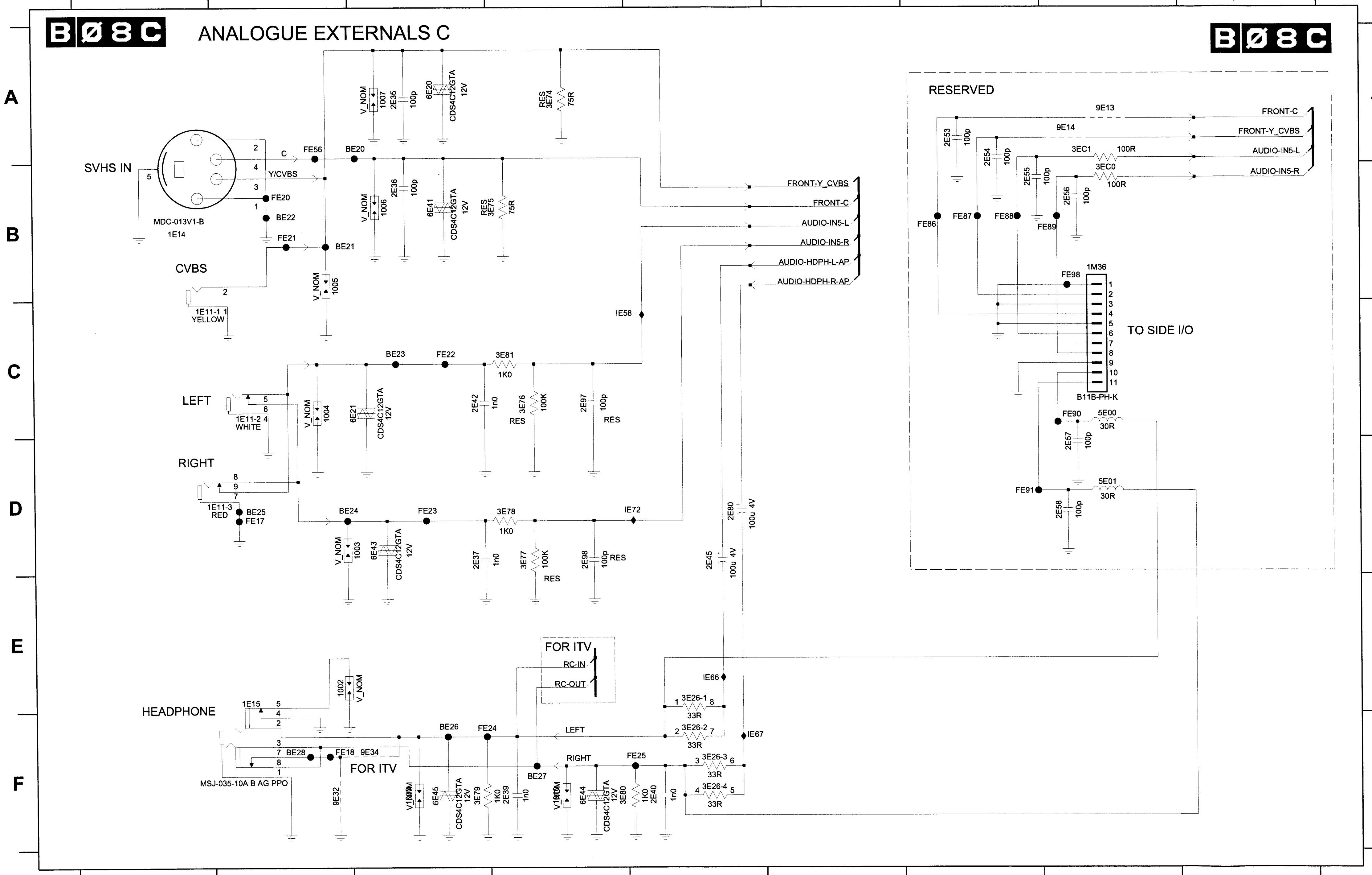
090303

SSB: Analogue Externals C


B08C
ANALOGUE EXTERNALS C
SVHS IN
MDC-013V1-B
1E14
CVBS
1E11-1 YELLOW
LEFT
1E11-2 WHITE
RIGHT
1E11-3 RED
HEADPHONE
1E15
MSJ-035-10A B AG PPO
FOR ITV
RC-IN
RC-OUT
FRONT-Y_CVBS
FRONT-C
AUDIO-IN5-L
AUDIO-IN5-R
AUDIO-HDPH-L-AP
AUDIO-HDPH-R-AP
LEFT
RIGHT
V_NOM
CDS4C12GTA 12V
RES
RESERVED
FRONT-C
FRONT-Y_CVBS
AUDIO-IN5-L
AUDIO-IN5-R
1M36
B11B-PH-K
TO SIDE I/O
5E00 30R
5E01 30R
3E26-1 33R
3E26-2 33R
3E26-3 33R
3E26-4 33R
2E80 100u 4V
2E45 100u 4V
3E81 1K0
3E78 1K0
3E76 100K
3E77 100K
3E74 75R
3E75 75R
3EC1 100R
3EC0 100R

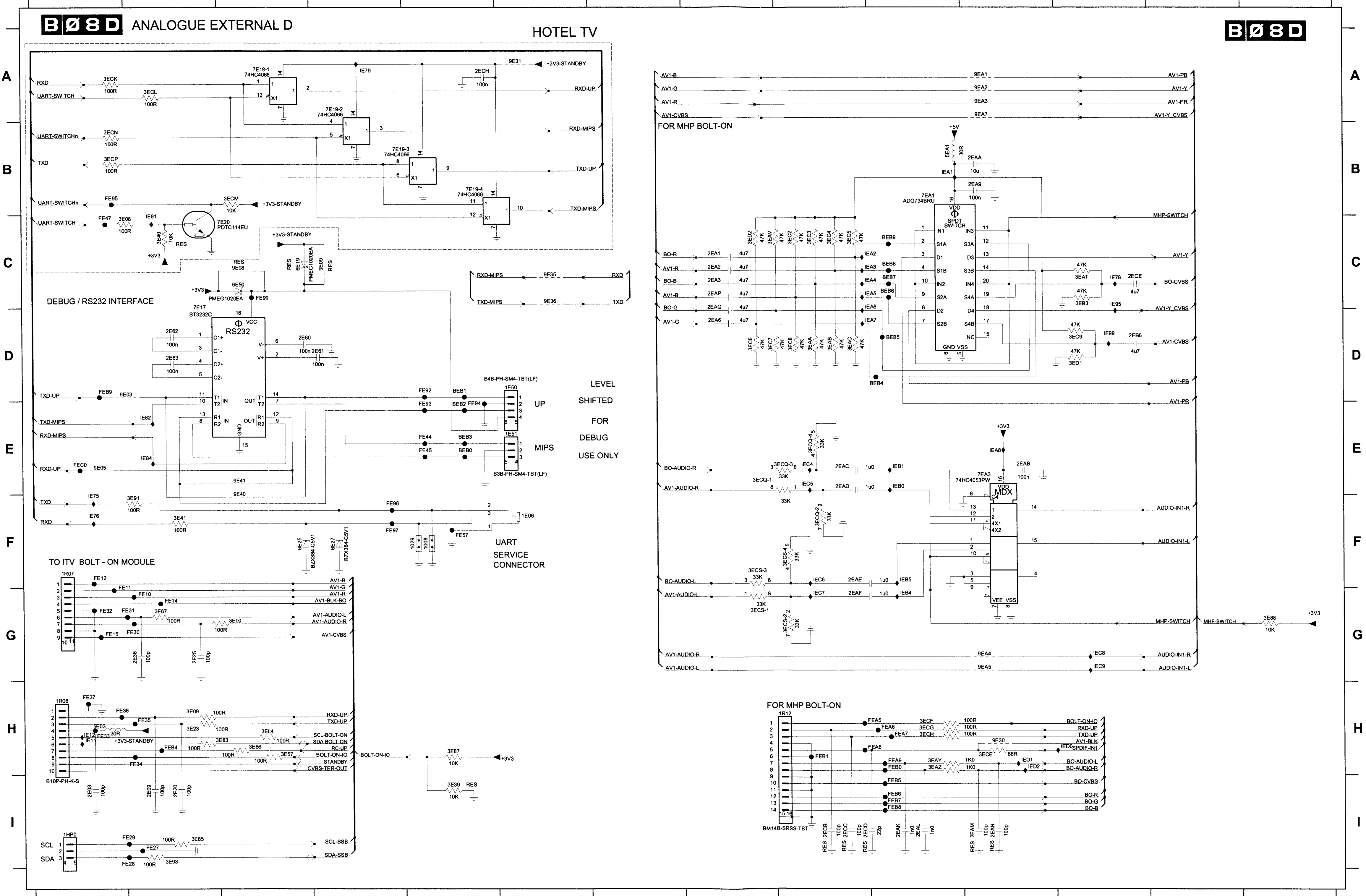
1000 F3	FE87 B7
1002 E2	FE88 B7
1003 D3	FE89 B8
1004 C2	FE90 C8
1005 B2	FE91 D7
1006 B3	FE98 B8
1007 A3	IE58 C4
1010 F4	IE66 E5
1E11-1 C1	IE67 F5
1E11-2 C2	IE72 D5
1E11-3 D2	
1E14 B1	
1E15 E2	
1M36 B8	
2E35 A3	
2E36 B3	
2E37 D3	
2E39 F4	
2E40 F5	
2E42 C3	
2E45 D5	
2E53 A7	
2E54 A7	
2E55 B7	
2E56 B8	
2E57 D8	
2E58 D8	
2E80 D5	
2E97 C4	
2E98 D4	
3E26-1 E5	
3E26-2 F5	
3E26-3 F5	
3E26-4 F5	
3E74 A4	
3E75 B4	
3E76 C4	
3E77 D4	
3E78 D4	
3E79 F3	
3E80 F4	
3E81 C4	
3EC0 B8	
3EC1 A8	
5E00 C8	
5E01 D8	
6E20 A3	
6E21 C3	
6E41 B3	
6E43 D3	
6E44 F4	
6E45 F3	
9E13 A8	
9E14 A8	
9E32 F2	
9E34 F3	
BE20 A3	
BE21 B2	
BE22 B2	
BE23 C3	
BE24 D2	
BE25 D2	
BE26 F3	
BE27 F4	
BE28 F2	
FE17 D2	
FE18 F2	
FE20 B2	
FE21 B2	
FE22 C3	
FE23 D3	
FE24 F3	
FE25 F5	
FE56 A2	
FE86 B7	

CHN
SETNAME
CLASS_NO
ANA + SIDE I/O
TV543 R2 LDIPNX
8204 000 8930
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid
SUPERS. 4
130 - 3
A3
CHECK
DATE 2008-01-18

PHILIPS

18310_544_090303.eps
090303

SSB: Analogue Externals D


B08D ANALOGUE EXTERNAL D
HOTEL TV
B08D
DEBUG / RS232 INTERFACE
RS232
7E17 ST3232C
7E19-1 74HC4066
7E19-2 74HC4066
7E19-3 74HC4066
7E19-4 74HC4066
7E20 PDTC114EU
+3V3-STANDBY
RXD
UART-SWITCH
UART-SWITCHn
TXD
RXD-UP
RXD-MIPS
TXD-UP
TXD-MIPS
LEVEL SHIFTED FOR DEBUG USE ONLY
UP
MIPS
B4B-PH-SM4-TBT(LF)
B3B-PH-SM4-TBT(LF)
UART SERVICE CONNECTOR
TO ITV BOLT - ON MODULE
AV1-B
AV1-G
AV1-R
AV1-BLK-BO
AV1-AUDIO-L
AV1-AUDIO-R
AV1-CVBS
SCL-BOLT-ON
SDA-BOLT-ON
RC-UP
BOLT-ON-IO
STANDBY
CVBS-TER-OUT
B10P-PH-K-S
SCL
SDA
SCL-SSB
SDA-SSB
FOR MHP BOLT-ON
7EA1 ADG734BRU
SPDT SWITCH
AV1-PB
AV1-Y
AV1-PR
AV1-Y_CVBS
MHP-SWITCH
BO-R
BO-B
BO-G
BO-CVBS
7EA3 74HC4053PW
MDX
BO-AUDIO-R
AV1-AUDIO-R
BO-AUDIO-L
AV1-AUDIO-L
AUDIO-IN1-R
AUDIO-IN1-L
FOR MHP BOLT-ON
BM14B-SRSS-TBT
BOLT-ON-IO
SPDIF-IN1
AV1-BLK

CHN
SETNAME
CLASS_NO
ANA + SIDE I/O
TV543 R2 LDIPNX
2008-10-10 3
8204 000 8930
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 4
130 - 4
A2
CHECK
DATE 2008-01-18

1008	F5
1029	F5
1E06	F6
1E50	D6
1E51	E6
1HP0	I1
1R07	F1
1R08	H1
1R12	H9
2E03	I1
2E09	I2
2E20	I2
2E25	G2
2E38	G2
2E60	D3
2E61	D4
2E62	D2
2E63	D2
2EA1	C8
2EA2	C8
2EA3	C8
2EA6	D8
2EA9	B11
2EAA	B11
2EAB	E11
2EAC	E9
2EAD	E9
2EAE	F9
2EAF	G9
2EAK	I10
2EAL	I10
2EAM	I11
2EAN	I11
2EAP	C8
2EAQ	D8
2EB6	D12
2ECB	I9
2ECC	I9
2ECD	I9
2ECE	C12
2ECH	A5
3E00	G3
3E08	C2
3E09	H2
3E23	H2
3E39	I5
3E40	C2
3E41	F2
3E57	H3
3E67	G2
3E83	H3
3E84	H3
3E85	I2
3E86	H3
3E87	H5
3E88	G14
3E91	F2
3E93	I2
3EAA	D9
3EAB	D9
3EAC	D9
3EAT	C12
3EAV	C8
3EAY	H10
3EAZ	H10
3EB3	C12
3EC2	C9
3EC3	C9
3EC4	C9
3EC5	C9
3EC6	D8
3EC7	D8
3EC8	D9
3EC9	D12
3ECE	H11
3ECF	H10
3ECG	H10
3ECH	H10
3ECK	A1
3ECL	A2
3ECM	B3
3ECN	B1
3ECP	B1
3ECQ-1	E8
3ECQ-2	F9
3ECQ-3	E9
3ECQ-4	E9
3ECS-1	G8
3ECS-2	G9
3ECS-3	F8
3ECS-4	F9
3ED1	D12
3ED2	C8
5E03	H1
5EA1	B10
6E19	C3
6E25	F3
6E27	F4
6E50	C3
7E17	D2
7E19-1	A3
7E19-2	A4
7E19-3	B5
7E19-4	B5
7E20	C3
7EA1	B10
7EA3	E11
9E03	D2
9E05	E1
9E08	C3
9E09	C4
9E30	H11
9E31	A6
9E35	C6
9E36	C6
9E40	F3
9E41	E3
9EA1	A11
9EA2	A11
9EA3	A11
9EA4	G11
9EA5	G11
9EA7	A11
BEB0	E5
BEB1	D5
BEB2	E5
BEB3	E5
BEB4	D10
BEB5	D10
BEB6	C10
BEB7	C10
BEB8	C10
BEB9	C10
FE10	G2
FE11	G1
FE12	F1
FE14	G2
FE15	G1
FE27	I2
FE28	I1
FE29	I2
FE30	G2
FE31	G2
FE32	G1
FE33	H1
FE34	H2
FE35	H2
FE36	H1
FE37	H1
FE44	E5
FE45	E5
FE47	C1
FE57	F5
FE92	D5
FE93	E5
FE94	E5
FE95	B1
FE96	F4
FE97	F4
FE99	C3
FEA5	H10
FEA6	H10
FEA7	H10
FEA8	H10
FEA9	H10
FEB0	H10
FEB1	H9
FEB4	H2
FEB5	I10
FEB6	I10
FEB7	I10
FEB8	I10
FEB9	D1
FEC0	E1
IE11	H1
IE12	H1
IE75	F1
IE76	F1
IE78	C12
IE79	A4
IE81	C2
IE82	E2
IE84	E2
IE95	C12
IE99	D12
IEA1	B10
IEA2	C10
IEA3	C10
IEA4	C10
IEA5	C10
IEA6	C10
IEA7	D10
IEA8	E11
IEB0	E10
IEB1	E10
IEB4	G10
IEB5	F10
IEC4	E9
IEC5	E9
IEC6	F9
IEC7	G9
IEC8	G12
IEC9	G12
IED0	H12
IED1	H11
IED2	H11

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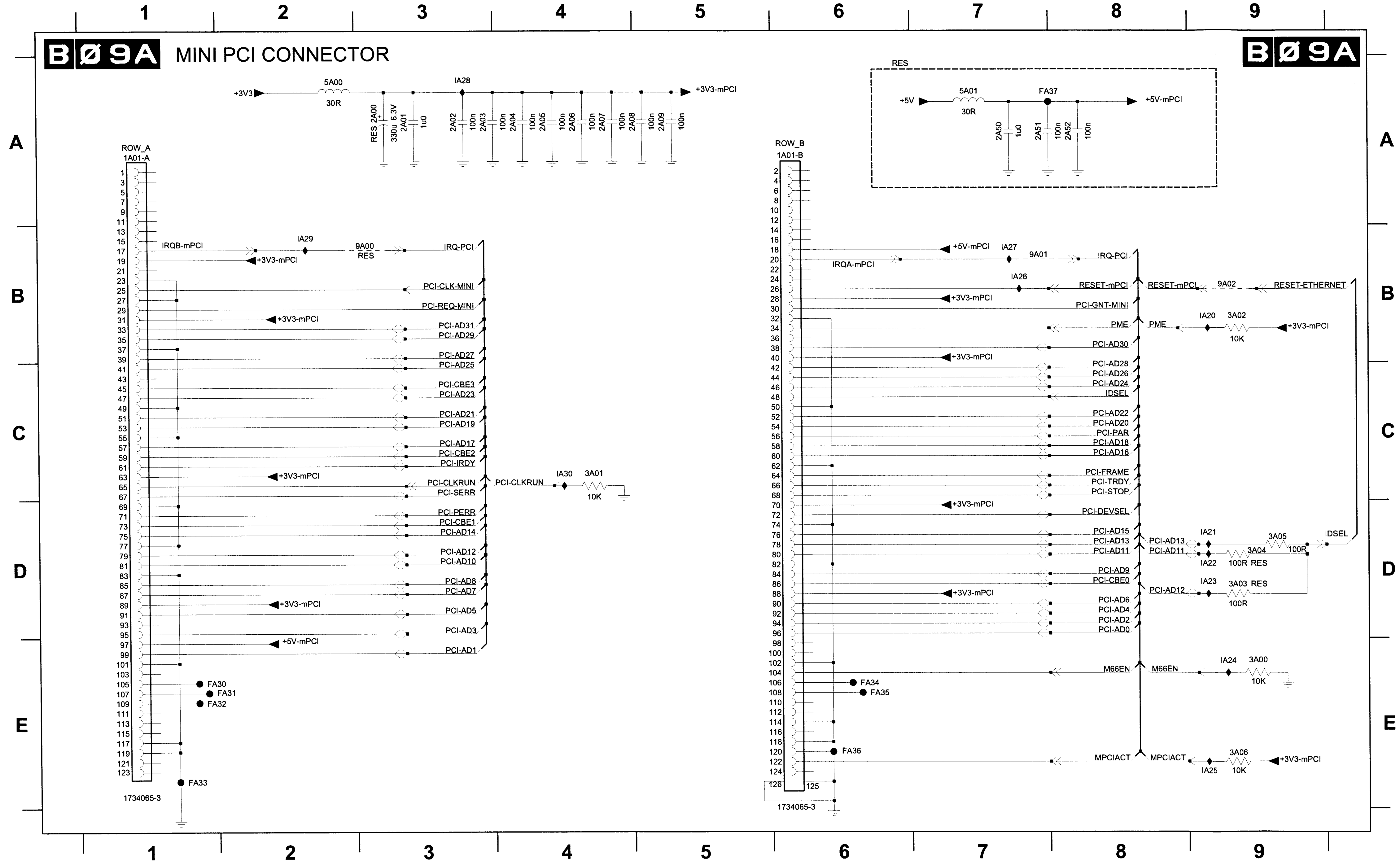
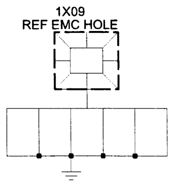
090303

SSB: Mini PCI Connector


B09A MINI PCI CONNECTOR
+3V3
5A00
30R
IA28
+3V3-mPCI
RES 2A00 330u 6.3V
2A01 1u0
2A02 100n
2A03 100n
2A04 100n
2A05 100n
2A06 100n
2A07 100n
2A08 100n
2A09 100n
RES
+5V
5A01
30R
FA37
+5V-mPCI
2A50 1u0
2A51 100n
2A52 100n
ROW_A
1A01-A
ROW_B
1A01-B
IRQB-mPCI
IA29
9A00
RES
IRQ-PCI
+3V3-mPCI
PCI-CLK-MINI
PCI-REQ-MINI
PCI-AD31
PCI-AD29
PCI-AD27
PCI-AD25
PCI-CBE3
PCI-AD23
PCI-AD21
PCI-AD19
PCI-AD17
PCI-CBE2
PCI-IRDY
PCI-CLKRUN
PCI-SERR
IA30
3A01
10K
PCI-PERR
PCI-CBE1
PCI-AD14
PCI-AD12
PCI-AD10
PCI-AD8
PCI-AD7
PCI-AD5
PCI-AD3
PCI-AD1
FA30
FA31
FA32
FA33
1734065-3
+5V-mPCI
IA27
9A01
IRQA-mPCI
IA26
RESET-mPCI
9A02
RESET-ETHERNET
PCI-GNT-MINI
PME
IA20
3A02
10K
PCI-AD30
PCI-AD28
PCI-AD26
PCI-AD24
IDSEL
PCI-AD22
PCI-AD20
PCI-PAR
PCI-AD18
PCI-AD16
PCI-FRAME
PCI-TRDY
PCI-STOP
PCI-DEVSEL
PCI-AD15
PCI-AD13
PCI-AD11
IA21
3A05
3A04
100R
IA22
100R RES
IA23
3A03 RES
100R
PCI-AD9
PCI-CBE0
PCI-AD12
PCI-AD6
PCI-AD4
PCI-AD2
PCI-AD0
M66EN
IA24
3A00
10K
FA34
FA35
FA36
MPCIACT
3A06
IA25
10K
B09A


1X09
REF EMC HOLE

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2A00	A3
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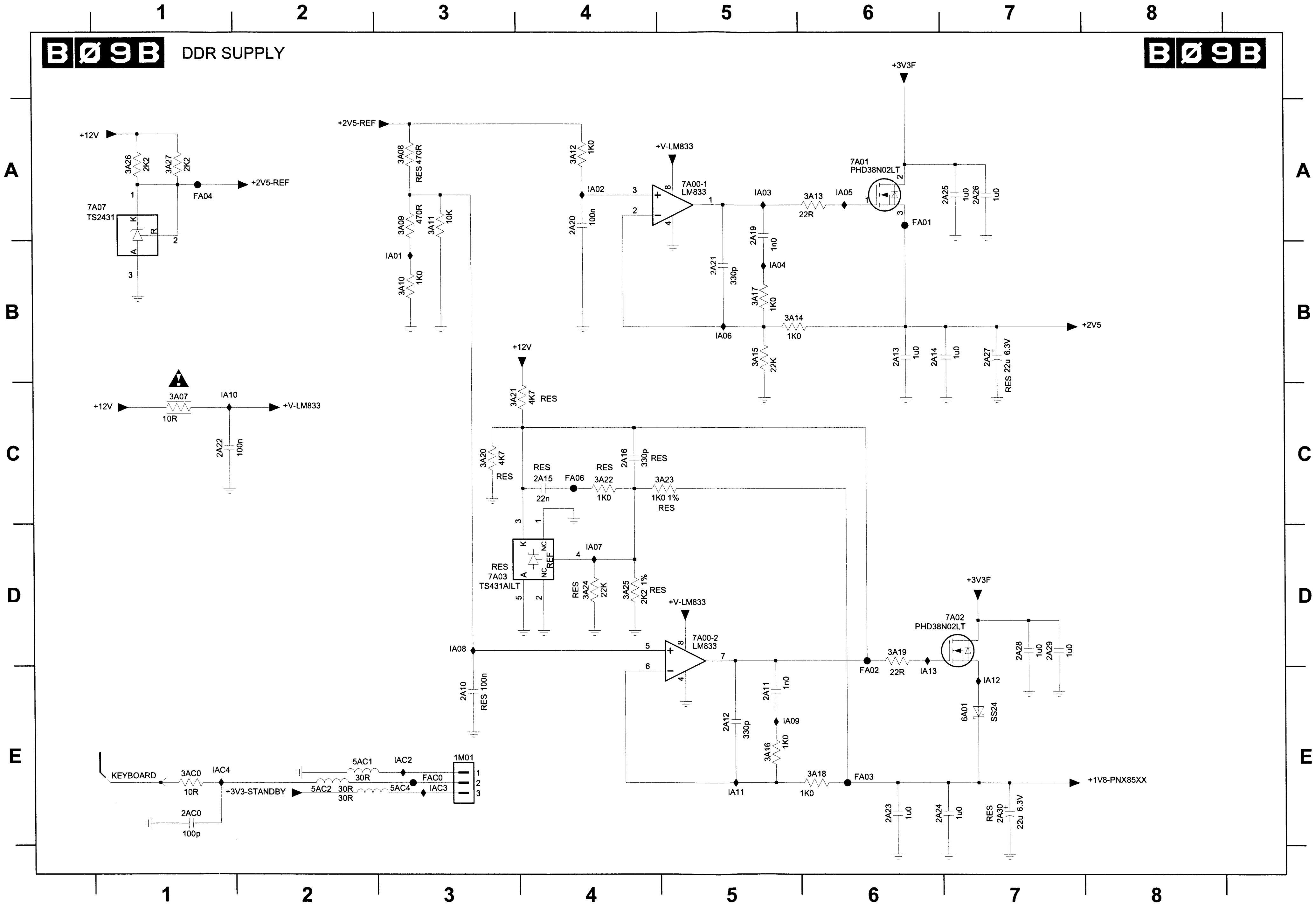
2A03	A3
2A04	A4
2A05	A4
2A06	A4
2A07	A4
2A08	A5
2A09	A5
2A50	A7
2A51	A7
2A52	A8
3A00	E9
3A01	C4
3A02	B9
3A03	D9
3A04	D9
3A05	D9
3A06	E9
5A00	A2
5A01	A7
9A00	B3
9A01	B7
9A02	B9
FA30	E1
FA31	E2
FA32	E1
FA33	E1
FA34	E6
FA35	E6
FA36	E6
FA37	A8
IA20	B9
IA21	D9
IA22	D9
IA23	D9
IA24	E9
IA25	E9
IA26	B7
IA27	B7
IA28	A3
IA29	B2
IA30	C4

CHN
SETNAME
CLASS_NO
MINI PCI
TV543 R2 LDIPNX
2008-10-10 3
8204 000 8935
2 2008-11-21
NAME Maelegheer Ingrid
SUPERS. 2
130 – 1
A3
CHECK
DATE 2007-10-16

18310_546_090303.eps
090303

SSB: DDR Supply

PHILIPS

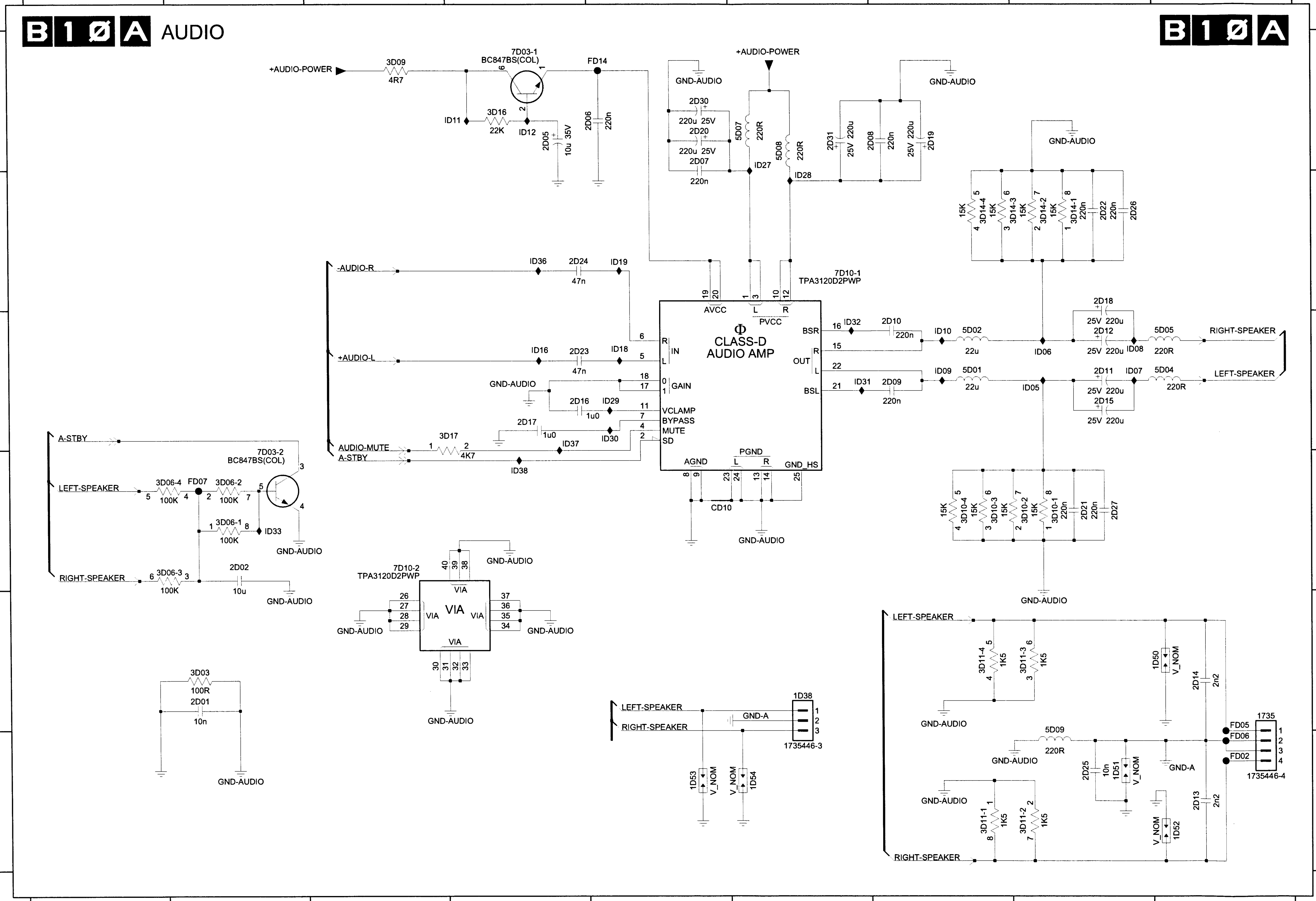

B09B
DDR SUPPLY
B09B
+12V
3A26 2K2
3A27 2K2
+2V5-REF
FA04
7A07 TS2431
K
A
R
+2V5-REF
3A08 RES 470R
3A09 470R
3A11 10K
IA01
3A10 1K0
3A12 1K0
IA02
2A20 100n
+V-LM833
7A00-1 LM833
IA03
2A21 330p
2A19 1n0
IA04
3A17 1K0
IA06
3A14 1K0
3A15 22K
3A13 22R
IA05
+3V3F
7A01 PHD38N02LT
FA01
2A25 1u0
2A26 1u0
+2V5
2A13 1u0
2A14 1u0
2A27 RES 22u 6.3V
+12V
3A07 10R
IA10
+V-LM833
2A22 100n
+12V
3A21 4K7 RES
3A20 4K7 RES
RES 2A15 22n
FA06
RES 3A22 1K0
2A16 330p RES
3A23 1K0 1% RES
RES 7A03 TS431AILT
REF
NC
IA07
RES 3A24 22K
3A25 2K2 1% RES
+V-LM833
7A00-2 LM833
IA08
2A10 RES 100n
2A12 330p
2A11 1n0
IA09
3A16 1K0
IA11
3A18 1K0
FA03
FA02
3A19 22R
IA13
+3V3F
7A02 PHD38N02LT
2A28 1u0
2A29 1u0
IA12
6A01 SS24
+1V8-PNX85XX
2A23 1u0
2A24 1u0
RES 2A30 22u 6.3V
KEYBOARD
3AC0 10R
IAC4
+3V3-STANDBY
2AC0 100p
5AC1 30R
5AC2 30R
5AC4 30R
IAC2
IAC3
FAC0
1M01

1M01 E3	IA13 E6
2A10 E3	IAC2 E3
2A11 E5	IAC3 E3
2A12 E5	IAC4 E1
2A13 B6	
2A14 B6	
2A15 C4	
2A16 C4	
2A19 A5	
2A20 A4	
2A21 B5	
2A22 C1	
2A23 E6	
2A24 E6	
2A25 A7	
2A26 A7	
2A27 B7	
2A28 D7	
2A29 D7	
2A30 E7	
2AC0 E1	
3A07 C1	
3A08 A3	
3A09 A3	
3A10 B3	
3A11 A3	
3A12 A4	
3A13 A6	
3A14 B5	
3A15 B5	
3A16 E5	
3A17 B5	
3A18 E6	
3A19 D6	
3A20 C3	
3A21 C3	
3A22 C4	
3A23 C5	
3A24 D4	
3A25 D4	
3A26 A1	
3A27 A1	
3AC0 E1	
5AC1 E2	
5AC2 E2	
5AC4 E3	
6A01 E7	
7A00-1 A5	
7A00-2 D5	
7A01 A6	
7A02 D7	
7A03 D3	
7A07 A1	
FA01 A6	
FA02 E6	
FA03 E6	
FA04 A1	
FA06 C4	
FAC0 E3	
IA01 B3	
IA02 A4	
IA03 A5	
IA04 B5	
IA05 A6	
IA06 B5	
IA07 D4	
IA08 D3	
IA09 E5	
IA10 C1	
IA11 E5	
IA12 E7	

CHN
SETNAME
CLASS_NO
MINI PCI
TV543 R2 LDIPNX
8204 000 8935
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid
SUPERS. 2
CHECK
DATE 2008-01-18
130 - 2
A3

18310_547_090303.eps
090303

SSB: Audio


B10A AUDIO
B10A
+AUDIO-POWER
3D09
4R7
7D03-1
BC847BS(COL)
FD14
ID11
3D16
22K
ID12
2D05
10u 35V
2D06
220n
GND-AUDIO
2D30
220u 25V
2D20
220u 25V
2D07
220n
5D07
220R
5D08
220R
ID27
ID28
2D31
25V 220u
2D08
220n
25V 220u
2D19
3D14-4
3D14-3
3D14-2
3D14-1
15K
2D22
220n
2D26
-AUDIO-R
ID36
2D24
47n
ID19
7D10-1
TPA3120D2PWP
AVCC
PVCC
CLASS-D
AUDIO AMP
BSR
OUT
BSL
IN
GAIN
VCLAMP
BYPASS
MUTE
SD
AGND
PGND
GND_HS
+AUDIO-L
ID16
2D23
47n
ID18
2D16
1u0
ID29
2D17
1u0
ID30
3D17
4K7
ID37
ID38
AUDIO-MUTE
A-STBY
ID32
2D10
220n
ID31
2D09
220n
ID10
5D02
22u
ID06
ID09
5D01
22u
ID05
2D18
25V 220u
2D12
25V 220u
ID08
5D05
220R
RIGHT-SPEAKER
2D11
ID07
5D04
220R
LEFT-SPEAKER
2D15
25V 220u
CD10
3D10-4
3D10-3
3D10-2
3D10-1
2D21
220n
2D27
A-STBY
7D03-2
BC847BS(COL)
LEFT-SPEAKER
3D06-4
100K
FD07
3D06-2
100K
3D06-1
100K
ID33
RIGHT-SPEAKER
3D06-3
100K
2D02
10u
7D10-2
TPA3120D2PWP
VIA
3D03
100R
2D01
10n
LEFT-SPEAKER
RIGHT-SPEAKER
GND-A
1D38
1735446-3
1D53
V_NOM
1D54
3D11-4
1K5
3D11-3
1K5
1D50
V_NOM
2D14
2n2
5D09
220R
2D25
10n
1D51
V_NOM
GND-A
FD05
FD06
FD02
1735
1735446-4
3D11-1
1K5
3D11-2
1K5
2D13
2n2
1D52
V_NOM

1735	E9
1D38	E6
1D50	E9
1D51	F8
1D52	F9
1D53	F5
1D54	F6
2D01	E2
2D02	D2
2D05	A4
2D06	A5
2D07	A5
2D08	A7
2D09	C7
2D10	C7
2D11	C8
2D12	C8
2D13	F9
2D14	E9
2D15	C8
2D16	C4
2D17	C4
2D18	B8
2D19	A7
2D20	A5
2D21	D8
2D22	B8
2D23	C4
2D24	B4
2D25	F8
2D26	B8
2D27	D8
2D30	A5
2D31	A6
3D03	E2
3D06-1	D2
3D06-2	D2
3D06-3	D2
3D06-4	D2
3D09	A3
3D10-1	D8
3D10-2	D8
3D10-3	D7
3D10-4	D7
3D11-1	F7
3D11-2	F8
3D11-3	E8
3D11-4	E7
3D14-1	B8
3D14-2	B8
3D14-3	B8
3D14-4	B7
3D16	A4
3D17	C4
5D01	C7
5D02	C7
5D04	C9
5D05	C9
5D07	A6
5D08	A6
5D09	F8
7D03-1	A4
7D03-2	C2
7D10-1	B6
7D10-2	D3
CD10	D5
FD02	F9
FD05	E9
FD06	F9
FD07	D2
FD14	A5
ID05	C8
ID06	C8
ID07	C8
ID08	C8
ID09	C7
ID10	C7
ID11	A4
ID12	A4
ID16	C4
ID18	C5
ID19	B5
ID27	A6
ID28	B6
ID29	C5
ID30	C5
ID31	C6
ID32	C6
ID33	D2
ID36	B4
ID37	C4
ID38	D4

CHN
SETNAME
CLASS_NO

CLASS D
TV543 R2 LDIPNX

8204 000 8931

2 2008-11-21

2008-10-10 3

NAME Randal De Keyzer
SUPERS. 1
130 - 1
A3
CHECK
DATE 2007-10-12

SSB: SRP List Explanation

Example

Net Name	*Diagram*
+12-15V	AP1 (4x)
+12-15V	AP4 (4x)
+12-15V	AP5 (12x)
+12-15V	AP6 (4x)
+12-15V	AP7 (8x)
+12V	AP1 (4x)
+12V_NF	AP1 (2x)
+12VAL	AP1 (2x)
+25VLP	AP1 (4x)
+25VLP	AP2 (1x)
+3V3-STANDBY	AP5 (3x)
+400V-F	AP1 (2x)
+400V-F	AP2 (2x)
+400V-F	AP3 (2x)
+5V2	AP1 (6x)
+5V2	AP2 (1x)
+5V2-NF	AP1 (1x)
+5V2-NF	AP2 (1x)
+5V-SW	AP1 (6x)
+5V-SW	AP2 (1x)
+8V6	AP1 (3x)
+AUX	AP1 (2x)
+AUX	AP2 (1x)
+DC-F	AP1 (2x)
+DC-F	AP3 (2x)
+SUB-SPEAKER	AP5 (1x)
+SUB-SPEAKER	AP6 (2x)
-12-15V	AP1 (4x)
-12-15V	AP4 (6x)
-12-15V	AP5 (14x)
-12-15V	AP6 (6x)
-12-15V	AP7 (8x)
AL-OFF	AP1 (2x)
AUDIO-L	AP4 (1x)
AUDIO-L	AP5 (1x)
AUDIO-PROT	AP5 (3x)
AUDIO-R	AP4 (1x)
AUDIO-R	AP5 (1x)
AUDIO-SW	AP5 (1x)
AUDIO-SW	AP7 (1x)
BOOST	AP1 (2x)
CPROT	AP4 (2x)
CPROT	AP5 (1x)
CPROT-SW	AP5 (1x)
CPROT-SW	AP6 (2x)
-DC-F	AP1 (2x)
-DC-F	AP3 (2x)
DC-PROT	AP1 (1x)
DC-PROT	AP5 (2x)
DIM-CONTROL	AP1 (2x)
FEEDBACK+SW	AP6 (2x)
FEEDBACK-L	AP4 (2x)
FEEDBACK-R	AP4 (2x)
FEEDBACK-SW	AP6 (2x)
GND-AL	AP1 (2x)
GNDHA	AP1 (40x)
GNDHA	AP2 (20x)
GNDHA	AP3 (2x)
GNDHOT	AP3 (2x)
GND-L	AP1 (2x)
GND-L	AP4 (4x)
GND-L	AP5 (34x)
GND-LL	AP4 (7x)
GND-LL	AP5 (1x)
GND-LR	AP4 (7x)
GND-LR	AP5 (1x)
GND-LSW	AP5 (1x)
GND-LSW	AP6 (15x)
GND-S	AP1 (11x)
GND-SA	AP4 (8x)
GND-SA	AP5 (2x)
GND-SA	AP6 (8x)
GND-SA	AP7 (6x)
GNDscrew	AP3 (2x)
GNDscrew	AP5 (2x)
GND-SSB	AP5 (3x)
GND-SSP	AP1 (51x)
GND-SSP	AP2 (15x)
IN+SW	AP6 (2x)
IN-L	AP4 (2x)
IN-R	AP4 (2x)
IN-SW	AP6 (2x)
INV-MUTE	AP4 (1x)
INV-MUTE	AP5 (1x)
INV-MUTE	AP6 (1x)
LEFT-SPEAKER	AP4 (1x)
LEFT-SPEAKER	AP5 (1x)
MUTE	AP4 (2x)
MUTE	AP5 (1x)
MUTE	AP6 (2x)
ON-OFF	AP1 (3x)
OUT	AP6 (1x)
OUT	AP7 (2x)
OUTN	AP6 (1x)
OUTN	AP7 (1x)
POWER-GOOD	AP1 (2x)
POWER-OK-PLATFORM	AP1 (2x)
RIGHT-SPEAKER	AP4 (1x)
RIGHT-SPEAKER	AP5 (1x)
SOUND-ENABLE	AP5 (3x)
STANDBY	AP1 (5x)
STANDBY	AP2 (1x)
-SUB-SPEAKER	AP5 (1x)
-SUB-SPEAKER	AP6 (2x)
V-CLAMP	AP1 (1x)
V-CLAMP	AP3 (2x)

1.1. Introduction

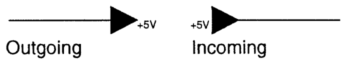
SRP (Service Reference Protocol) is a software tool that creates a list with all references to signal lines. The list contains references to the signals within all schematics of a PWB. It replaces the text references currently printed next to the signal names in the schematics. These printed references are created manually and are therefore not guaranteed to be 100% correct. In addition, in the current crowded schematics there is often none or very little place for these references.
Some of the PWB schematics will use SRP while others will still use the manual references. Either there will be an SRP reference list for a schematic, or there will be printed references in the schematic.

1.2. Non-SRP Schematics

There are several different signals available in a schematic:

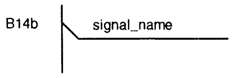
1.2.1. Power Supply Lines

All power supply lines are available in the supply line overview (see chapter 6). In the schematics (see chapter 7) is not indicated where supplies are coming from or going to.
It is however indicated if a supply is incoming (created elsewhere), or outgoing (created or adapted in the current schematic).



1.2.2. Normal Signals

For normal signals, a schematic reference (e.g. B14b) is placed next to the signals.

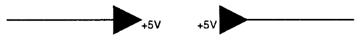


1.2.3. Grounds

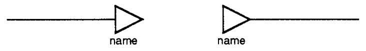
For normal and special grounds (e.g. GNDHOT or GND3V3 etc.), nothing is indicated.

1.3. SRP Schematics

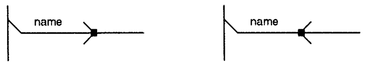
SRP is a tool, which automatically creates a list with signal references, indicating on which schematic the signals are used.
A reference is created for all signals indicated with an SRP symbol, these symbols are:



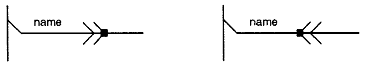
Power supply line.



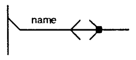
Stand alone signal or switching line (used as less as possible).



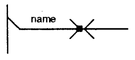
Signal line into a wire tree.



Switching line into a wire tree.



Bi-directional line (e.g. SDA) into a wire tree.



Signal line into a wire tree, its direction depends on the circuit (e.g. ingoing for PDP, outgoing for LCD sets).

Remarks:

- When there is a black dot on the "signal direction arrow" it is an SRP symbol, so there will be a reference to the signal name in the SRP list.
- All references to normal grounds (Ground symbols without additional text) are not listed in the reference list, this to keep it concise.
- Signals that are not used in multiple schematics, but only once or several times in the same schematic, are included in the SRP reference list, but only with one reference.

Additional Tip:

When using the PDF service manual file, you can very easily search for signal names and follow the signal over all the schematics. In Adobe PDF reader:

- Select the signal name you want to search for, with the "Select text" tool.
- Copy and paste the signal name in the "Search PDF" tool.
- Search for all occurrences of the signal name.
- Now you can quickly jump between the different occurrences and follow the signal over all schematics. It is advised to "zoom in" to e.g. 150% to see clearly, which text is selected. Then you can zoom out, to get an overview of the complete schematic.

PS. It is recommended to use at least Adobe PDF (reader) version 6.x, due to better search possibilities in this version.

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090121

Personal Notes:

SSB: SRP List Part 1

Netname	Schematic
B01B	+12V
B01C	+12V
B02B	+12V
B06B	+12V
B06C	+12V
B07B	+12V
B07H	+12V
B08B	+12V
B09B	+12V
B01B	+12VD
B05H	+12VD
B01A	+12VF
B01B	+12VF
B01A	+12VF1
B01C	+12VF2
B02B	+1V2
B02B	+1V2A
B06E	+1V2-FPGA
B06G	+1V2-FPGA
B06A	+1V2M
B06E	+1V2-PLL
B06G	+1V2-PLL
B01C	+1V2-PNX5100
B04A	+1V2-PNX5100
B05C	+1V2-PNX5100
B05C	+1V2-PNX5100-CLOCK
B05C	+1V2-PNX5100-DDR-PLL1
B05C	+1V2-PNX5100-DLL
B05C	+1V2-PNX5100-LVDS-PLL
B05C	+1V2-PNX5100-TRI-PLL1
B05C	+1V2-PNX5100-TRI-PLL2
B05C	+1V2-PNX5100-TRI-PLL3
B01A	+1V2-PNX85XX
B02B	+1V2-PNX85XX
B04A	+1V2-PNX85XX
B04P	+1V2-PNX85XX
B06A	+1V2-PNX85XX
B06E	+1V2-PNX85XX
B01A	+1V2-STANDBY
B01B	+1V2-STANDBY
B04P	+1V2-STANDBY
B05A	+1V8-PNX5100
B05C	+1V8-PNX5100
B06E	+1V8-PNX5100
B04G	+1V8-PNX85XX
B04P	+1V8-PNX85XX
B06E	+1V8-PNX85XX
B07D	+1V8-PNX85XX
B09B	+1V8-PNX85XX
B06A	+2V5
B06E	+2V5
B06F	+2V5
B09B	+2V5
B06F	+2V5-DDR1
B06G	+2V5-DDR1
B06E	+2V5in-FPGA
B06G	+2V5in-FPGA
B06A	+2V5M
B06E	+2V5out-FPGA
B06G	+2V5out-FPGA
B06E	+2V5-PLL
B06G	+2V5-PLL
B09B	+2V5-REF
B01B	+33VTUN
B02A	+33VTUN
B01A	+3V3
B01B	+3V3
B02B	+3V3
B04A	+3V3
B04L	+3V3
B04M	+3V3
B04N	+3V3
B04P	+3V3
B05C	+3V3
B05E	+3V3
B05F	+3V3
B05G	+3V3
B05H	+3V3
B05I	+3V3
B06A	+3V3
B06B	+3V3
B06C	+3V3
B06E	+3V3
B07A	+3V3
B07C	+3V3
B07D	+3V3
B07F	+3V3
B07G	+3V3
B07H	+3V3
B08A	+3V3
B08B	+3V3
B08D	+3V3
B09A	+3V3
B02A	+3V3A
B02B	+3V3A
B02B	+3V3D
B02B	+3V3E
B07G	+3V3-ET-ANA
B07G	+3V3-ET-DIG
B01A	+3V3F
B05H	+3V3F
B09B	+3V3F
B06E	+3V3-FPGA
B06G	+3V3-FPGA
B06A	+3V3M
B09A	+3V3-mPCI
B07F	+3V3-NAND
B04A	+3V3-PER
B04B	+3V3-PER
B04E	+3V3-PER
B04F	+3V3-PER
B04N	+3V3-PER
B04P	+3V3-PER
B05C	+3V3-PNX5100-CLOCK
B05C	+3V3-PNX5100-DDR-PLL0
B05C	+3V3-PNX5100-LVDS-IN
B05C	+3V3-PNX5100-LVDS-PLL
B01B	+3V3-STANDBY
B04A	+3V3-STANDBY
B04P	+3V3-STANDBY
B07D	+3V3-STANDBY
B08D	+3V3-STANDBY
B09B	+3V3-STANDBY
B01B	+5V
B01C	+5V
B04A	+5V
B04L	+5V
B06A	+5V
B07C	+5V
B07D	+5V
B08A	+5V
B08B	+5V
B08D	+5V
B09A	+5V
B01C	+5V5-TUN
B07H	+5V5-TUN
B07E	+5V-DDC
B07D	+5V-EDID
B07E	+5V-EDID
B09A	+5V-mPCI
B02A	+5V-TUN
B02B	+5V-TUN
B07H	+5V-TUN
B02B	+5V-TUN-CVBS
B02A	+5V-TUN-PIN
B04I	+AUDIO-L
B10	+AUDIO-L
B01B	+AUDIO-POWER
B04I	+AUDIO-POWER
B04M	+AUDIO-POWER
B10	+AUDIO-POWER
B05H	+VDISP
B06D	+VDISP
B05E	+VDISP1
B05H	+VDISP1
B05E	+VDISP2
B05H	+VDISP2
B09B	+V-LM833
B02A	+VTUN
B07D	1V8-HDMI
B04I (1×)	ADAC(1)
B04L (1×)	ADAC(1)
B04I (1×)	ADAC(2)
B04L (1×)	ADAC(2)
B04L (1×)	ADAC(3)
B04M (1×)	ADAC(3)
B04L (1×)	ADAC(4)
B04M (1×)	ADAC(4)
B04I (1×)	ADAC(5)
B04L (1×)	ADAC(5)
B04I (1×)	ADAC(6)
B04L (1×)	ADAC(6)
B04I (1×)	ADAC(7)
B04L (3×)	ADAC(7)
B04I (1×)	ADAC(8)
B04L (3×)	ADAC(8)
B07D (4×)	AIN-5V
B04A (2×)	ALE
B05D (1×)	AMBI-VS
B02B (2×)	ANTENNA-CTRL
B02A (2×)	ANTENNA-SUPPLY
B02B (1×)	ANTENNA-SUPPLY
B04M (1×)	A-PLOP
B08A (1×)	A-PLOP
B08B (2×)	A-PLOP
B08A (3×)	AP-SCART-OUT-L
B08A (3×)	AP-SCART-OUT-R
B07D (2×)	ARX0-
B07D (2×)	ARX0+
B07D (2×)	ARX1-
B07D (2×)	ARX1+
B07D (2×)	ARX2-
B07D (2×)	ARX2+
B07D (2×)	ARXC-
B07D (2×)	ARXC+
B07D (3×)	ARX-DDC-SCL
B07D (3×)	ARX-DDC-SDA
B07D (2×)	ARX-HOTPLUG
B06E (1×)	ASDO
B06G (1×)	ASDO
B04M (1×)	A-STBY
B10 (2×)	A-STBY
B04I (1×)	AUDIO-CL-L
B08A (1×)	AUDIO-CL-L
B04I (1×)	AUDIO-CL-R
B08A (1×)	AUDIO-CL-R
B04M (1×)	AUDIO-HDPH-L-AP
B08C (1×)	AUDIO-HDPH-L-AP
B04M (1×)	AUDIO-HDPH-R-AP
B08C (1×)	AUDIO-HDPH-R-AP
B04L (1×)	AUDIO-IN1-L
B08D (2×)	AUDIO-IN1-L
B04L (1×)	AUDIO-IN1-R
B08D (2×)	AUDIO-IN1-R
B04L (1×)	AUDIO-IN2-L
B08A (1×)	AUDIO-IN2-L
B04L (1×)	AUDIO-IN2-R
B08A (1×)	AUDIO-IN2-R
B04L (1×)	AUDIO-IN3-L
B08B (1×)	AUDIO-IN3-L
B04L (1×)	AUDIO-IN3-R
B08B (1×)	AUDIO-IN3-R
B04L (1×)	AUDIO-IN4-L
B07B (1×)	AUDIO-IN4-L
B04L (1×)	AUDIO-IN4-R
B07B (1×)	AUDIO-IN4-R
B04L (1×)	AUDIO-IN5-L
B08C (2×)	AUDIO-IN5-L
B04L (1×)	AUDIO-IN5-R
B08C (2×)	AUDIO-IN5-R
B04A (2×)	AUDIO-MUTE
B10 (1×)	AUDIO-MUTE
B04I (1×)	AUDIO-OUT-L
B08B (1×)	AUDIO-OUT-L
B04I (1×)	AUDIO-OUT-R
B08B (1×)	AUDIO-OUT-R
B04I (1×)	-AUDIO-R
B10 (1×)	-AUDIO-R
B04I (7×)	AUDIO-VDD
B04M (2×)	AUDIO-VDD
B08A (1×)	AV1-AUDIO-L
B08D (3×)	AV1-AUDIO-L
B08A (1×)	AV1-AUDIO-R
B08D (3×)	AV1-AUDIO-R
B08A (1×)	AV1-B
B08D (3×)	AV1-B
B04A (1×)	AV1-BLK
B08A (1×)	AV1-BLK
B08D (1×)	AV1-BLK
B08A (1×)	AV1-BLK-BO
B08D (1×)	AV1-BLK-BO
B08A (1×)	AV1-CVBS
B08D (3×)	AV1-CVBS
B08A (1×)	AV1-G
B08D (3×)	AV1-G
B04K (1×)	AV1-PB
B08D (2×)	AV1-PB
B04K (1×)	AV1-PR
B08D (2×)	AV1-PR
B08A (1×)	AV1-R
B08D (3×)	AV1-R
B04A (1×)	AV1-STATUS
B08A (1×)	AV1-STATUS
B04K (1×)	AV1-Y
B08D (2×)	AV1-Y
B04K (1×)	AV1-Y_CVBS
B08B (1×)	AV1-Y_CVBS
B08D (2×)	AV1-Y_CVBS
B04A (1×)	AV2-BLK
B08A (1×)	AV2-BLK
B04A (1×)	AV2-STATUS
B08A (1×)	AV2-STATUS
B04K (1×)	AV2-Y_CVBS
B08A (1×)	AV2-Y_CVBS
B08B (1×)	AV2-Y_CVBS
B04K (1×)	AV3-PB
B08A (1×)	AV3-PB
B04K (1×)	AV3-PR
B08A (1×)	AV3-PR
B04K (1×)	AV3-Y
B08A (1×)	AV3-Y
B04K (1×)	AV4-PB
B08A (1×)	AV4-PB
B08B (1×)	AV4-PB
B04K (1×)	AV4-PR
B08A (1×)	AV4-PR
B08B (1×)	AV4-PR
B04K (2×)	AV4-Y
B08A (1×)	AV4-Y
B08B (1×)	AV4-Y
B04K (1×)	AV5-PB
B08A (1×)	AV5-PB
B04K (1×)	AV5-PR
B08A (1×)	AV5-PR
B04K (2×)	AV5-Y
B08A (1×)	AV5-Y
B01B (1×)	BACKLIGHT-BOOST
B05H (1×)	BACKLIGHT-BOOST
B05H (1×)	BACKLIGHT-CONTROL-FPGA-IN
B06A (1×)	BACKLIGHT-CONTROL-FPGA-IN
B06G (1×)	BACKLIGHT-CONTROL-FPGA-IN
B05H (3×)	BACKLIGHT-CTRL
B01B (1×)	BACKLIGHT-OUT
B05E (1×)	BACKLIGHT-OUT
B05H (1×)	BACKLIGHT-OUT
B06G (1×)	BACKLIGHT-OUT
B05H (1×)	BACKLIGHT-OUT2
B06G (1×)	BACKLIGHT-OUT2
B01B (1×)	BACKLIGHT-PWM-ANA-DISP
B05H (1×)	BACKLIGHT-PWM-ANA-DISP
B05H (2×)	BACKLIGHT-PWM-ANA-SSB
B02A (3×)	B-IF-_N-IF-
B02A (3×)	B-IF+_N-IF+
B07D (4×)	BIN-5V
B06A (2×)	BL-CLK
B06A (2×)	BL-CS
B06A (2×)	BL-HS
B06A (2×)	BL-MISO
B06A (2×)	BL-MOSI
B05D (1×)	BL-OSCLK
B06A (1×)	BL-OSCLK
B05D (1×)	BL-SCK
B06A (1×)	BL-SCK
B05D (1×)	BL-SD0
B06A (1×)	BL-SD0
B06A (2×)	BL-VS
B05D (1×)	BL-WS
B06A (1×)	BL-WS
B08D (2×)	BO-AUDIO-L
B08D (2×)	BO-AUDIO-R
B08D (2×)	BO-B
B08D (2×)	BO-CVBS
B08D (2×)	BO-G
B04A (2×)	BOLT-ON-IO
B04N (1×)	BOLT-ON-IO
B08D (3×)	BOLT-ON-IO
B04A (2×)	BOLT-ON-TS-ENn
B04N (1×)	BOLT-ON-TS-ENn
B05H (3×)	BOOST-CTRL
B04E (2×)	BOOTMODE
B08D (2×)	BO-R
B07D (2×)	BRX0-
B07D (2×)	BRX0+
B07D (2×)	BRX1-
B07D (2×)	BRX1+
B07D (2×)	BRX2-
B07D (2×)	BRX2+
B07D (2×)	BRXC-
B07D (2×)	BRXC+
B07D (3×)	BRX-DDC-SCL
B07D (3×)	BRX-DDC-SDA
B07D (2×)	BRX-HOTPLUG
B04K (1×)	B-VGA
B08B (1×)	B-VGA
B04N (1×)	CA-ADDEN
B07H (3×)	CA-ADDEN
B04N (1×)	CA-CD1
B07A (2×)	CA-CD1
B04N (1×)	CA-CD2
B07A (2×)	CA-CD2
B07A (1×)	CA-CE1
B07H (1×)	CA-CE1
B07A (1×)	CA-CE2
B07H (1×)	CA-CE2
B04N (1×)	CA-DATADIR
B07H (1×)	CA-DATADIR
B04N (1×)	CA-DATAEN
B07H (1×)	CA-DATAEN
B07A (2×)	CA-INPACK
B07A (1×)	CA-IORD
B07H (1×)	CA-IORD
B07A (1×)	CA-IOWR
B07H (1×)	CA-IOWR
B04N (1×)	CA-MDI0
B07A (1×)	CA-MDI0
B04N (1×)	CA-MDI1
B07A (1×)	CA-MDI1
B04N (1×)	CA-MDI2
B07A (1×)	CA-MDI2
B04N (1×)	CA-MDI3
B07A (1×)	CA-MDI3
B04N (1×)	CA-MDI4
B07A (1×)	CA-MDI4
B04N (1×)	CA-MDI5
B07A (1×)	CA-MDI5
B04N (1×)	CA-MDI6
B07A (1×)	CA-MDI6
B04N (1×)	CA-MDI7
B07A (1×)	CA-MDI7
B04N (1×)	CA-MDO0
B07A (2×)	CA-MDO0
B04N (1×)	CA-MDO1
B07A (2×)	CA-MDO1
B04N (1×)	CA-MDO2
B07A (2×)	CA-MDO2
B04N (1×)	CA-MDO3
B07A (2×)	CA-MDO3
B04N (1×)	CA-MDO4
B07A (2×)	CA-MDO4
B04N (1×)	CA-MDO5
B07A (2×)	CA-MDO5
B04N (1×)	CA-MDO6
B07A (2×)	CA-MDO6
B04N (1×)	CA-MDO7
B07A (2×)	CA-MDO7
B04N (1×)	CA-MICLK
B07A (1×)	CA-MICLK
B04N (1×)	CA-MISTRT
B07A (1×)	CA-MISTRT
B04N (1×)	CA-MIVAL
B07A (1×)	CA-MIVAL
B04N (2×)	CA-MOCLK_VS2
B07A (2×)	CA-MOCLK_VS2
B04N (1×)	CA-MOSTRT
B07A (2×)	CA-MOSTRT
B04N (1×)	CA-MOVAL
B07A (2×)	CA-MOVAL
B07A (1×)	CA-OE
B07H (1×)	CA-OE
B07A (1×)	CA-REG
B07H (1×)	CA-REG
B04N (1×)	CA-RST
B07A (2×)	CA-RST
B04N (1×)	CA-VS1
B07A (2×)	CA-VS1
B07A (2×)	CA-WAIT
B07H (1×)	CA-WAIT
B07A (1×)	CA-WE
B07H (1×)	CA-WE
B06A (3×)	CCLK
B04A (2×)	CEC-HDMI
B07D (1×)	CEC-HDMI
B07D (4×)	CIN-5V
B06G (2×)	CLK-OUT2-PNX5100
B05F (1×)	CLK-OUT-PNX5100
B06A (1×)	CLK-OUT-PNX5100
B06G (1×)	CLK-OUT-PNX5100
B06E (1×)	CON20
B06G (1×)	CON20
B06E (1×)	CON21
B06G (1×)	CON21
B06E (1×)	CON22
B06G (1×)	CON22
B06E (1×)	CON23
B06G (1×)	CON23
B06E (1×)	CON26
B06G (1×)	CON26
B06E (1×)	CON27
B06G (1×)	CON27
B06E (1×)	CONF-DONE
B06G (1×)	CONF-DONE
B07D (2×)	CRX0-
B07D (2×)	CRX0+
B07D (2×)	CRX1-
B07D (2×)	CRX1+
B07D (2×)	CRX2-
B07D (2×)	CRX2+
B07D (2×)	CRXC-
B07D (2×)	CRXC+
B07D (3×)	CRX-DDC-SCL
B07D (3×)	CRX-DDC-SDA
B07D (2×)	CRX-HOTPLUG
B06A (4×)	CSO-B
B05H (2×)	CTRL1-PNX5100
B05H (2×)	CTRL2-PNX5100
B05H (2×)	CTRL3-PNX5100
B05H (3×)	CTRL4-PNX5100
B05E (1×)	CTRL-DISP1
B05H (1×)	CTRL-DISP1
B05E (1×)	CTRL-DISP2
B05H (1×)	CTRL-DISP2
B05E (1×)	CTRL-DISP3
B05H (1×)	CTRL-DISP3
B05E (1×)	CTRL-DISP4
B05H (2×)	CTRL-DISP4
B02B (1×)	CVBS4
B04K (1×)	CVBS4
B08B (2×)	CVBS-MON-OUT-CINCH
B08A (2×)	CVBS-OUT-SC1
B02B (1×)	CVBS-TER-OUT
B08A (1×)	CVBS-TER-OUT
B08D (1×)	CVBS-TER-OUT
B06E (1×)	DATA0
B06G (1×)	DATA0
B06E (1×)	DCLK
B06G (1×)	DCLK
B04H (1×)	DDCA-SCL
B07E (1×)	DDCA-SCL
B04H (1×)	DDCA-SDA
B07E (1×)	DDCA-SDA
B04H (1×)	DDC-SCL
B07D (1×)	DDC-SCL
B04H (1×)	DDC-SDA
B07D (1×)	DDC-SDA
B04G (3×)	DDR2-A0
B04G (3×)	DDR2-A1
B04G (3×)	DDR2-A10
B04G (3×)	DDR2-A11
B04G (3×)	DDR2-A12
B04G (3×)	DDR2-A2
B04G (3×)	DDR2-A3
B04G (3×)	DDR2-A4
B04G (3×)	DDR2-A5
B04G (3×)	DDR2-A6
B04G (3×)	DDR2-A7
B04G (3×)	DDR2-A8
B04G (3×)	DDR2-A9
B04G (3×)	DDR2-BA0
B04G (3×)	DDR2-BA1
B04G (2×)	DDR2-BA2
B04G (3×)	DDR2-CAS
B04G (3×)	DDR2-CKE
B04G (4×)	DDR2-CLK_N
B04G (4×)	DDR2-CLK_P
B04G (3×)	DDR2-CS
B04G (2×)	DDR2-D0
B04G (2×)	DDR2-D1
B04G (2×)	DDR2-D10
B04G (2×)	DDR2-D11
B04G (2×)	DDR2-D12
B04G (2×)	DDR2-D13
B04G (2×)	DDR2-D14
B04G (2×)	DDR2-D15
B04G (2×)	DDR2-D16
B04G (2×)	DDR2-D17
B04G (2×)	DDR2-D18
B04G (2×)	DDR2-D19
B04G (2×)	DDR2-D2
B04G (2×)	DDR2-D20
B04G (2×)	DDR2-D21
B04G (2×)	DDR2-D22
B04G (2×)	DDR2-D23
B04G (2×)	DDR2-D24
B04G (2×)	DDR2-D25
B04G (2×)	DDR2-D26
B04G (2×)	DDR2-D27
B04G (2×)	DDR2-D28
B04G (2×)	DDR2-D29
B04G (2×)	DDR2-D3
B04G (2×)	DDR2-D30
B04G (2×)	DDR2-D31
B04G (2×)	DDR2-D4
B04G (2×)	DDR2-D5
B04G (2×)	DDR2-D6
B04G (2×)	DDR2-D7
B04G (2×)	DDR2-D8
B04G (2×)	DDR2-D9
B04G (2×)	DDR2-DQM0
B04G (2×)	DDR2-DQM1
B04G (2×)	DDR2-DQM2
B04G (2×)	DDR2-DQM3
B04G (2×)	DDR2-DQS0_N
B04G (2×)	DDR2-DQS0_P
B04G (2×)	DDR2-DQS1_N
B04G (2×)	DDR2-DQS1_P
B04G (2×)	DDR2-DQS2_N
B04G (2×)	DDR2-DQS2_P
B04G (2×)	DDR2-DQS3_N
B04G (2×)	DDR2-DQS3_P
B04G (3×)	DDR2-ODT
B04G (3×)	DDR2-RAS
B04G (2×)	DDR2-VREF-CTRL
B04G (3×)	DDR2-VREF-DDR
B04G (3×)	DDR2-WE
B04A (3×)	DETECT1
B01B (1×)	DETECT-12V
B04A (1×)	DETECT-12V
B04A (3×)	DETECT2
B07D (4×)	DIN-5V
B06A (2×)	DONE
B06F (2×)	DQ1(0)
B06F (2×)	DQ1(1)
B06F (2×)	DQ1(10)
B06F (2×)	DQ1(11)
B06F (2×)	DQ1(12)
B06F (2×)	DQ1(13)
B06F (2×)	DQ1(14)
B06F (2×)	DQ1(15)
B06F (2×)	DQ1(2)
B06F (2×)	DQ1(3)
B06F (2×)	DQ1(4)
B06F (2×)	DQ1(5)
B06F (2×)	DQ1(6)
B06F (2×)	DQ1(7)
B06F (2×)	DQ1(8)
B06F (2×)	DQ1(9)
B06F (2×)	DQS10
B06F (2×)	DQS11
B07D (2×)	DRX0-
B07D (2×)	DRX0+
B07D (2×)	DRX1-
B07D (2×)	DRX1+
B07D (2×)	DRX2-
B07D (2×)	DRX2+
B07D (2×)	DRXC-
B07D (2×)	DRXC+
B07D (3×)	DRX-DDC-SCL
B07D (3×)	DRX-DDC-SDA
B07D (2×)	DRX-HOTPLUG
B04A (2×)	EA
B07E (4×)	EIN-5V
B04A (2×)	EJTAG-DETECT
B06B (1×)	EJTAG-DETECT
B05F (1×)	EJTAG-PNX5100-TCK
B05F (1×)	EJTAG-PNX5100-TDI
B05F (1×)	EJTAG-PNX5100-TDO
B05F (1×)	EJTAG-PNX5100-TMS
B05F (1×)	EJTAG-PNX5100-TRSTn
B04E (2×)	EJTAG-TCK
B06B (1×)	EJTAG-TCK
B04E (2×)	EJTAG-TDI
B06B (1×)	EJTAG-TDI
B04E (2×)	EJTAG-TDO
B06B (1×)	EJTAG-TDO
B04E (2×)	EJTAG-TMS
B06B (1×)	EJTAG-TMS
B04E (2×)	EJTAG-TRSTN
B06B (1×)	EJTAG-TRSTN
B01B (1×)	ENABLE-3V3
B04A (2×)	ENABLE-3V3
B01A (1×)	ENABLE-3V3-5V
B01B (1×)	ENABLE-3V3-5V
B01C (1×)	ENABLE-3V3-5V
B07E (3×)	ERX-DDC-SCL
B07E (3×)	ERX-DDC-SDA
B07E (3×)	ERX-HOTPLUG
B06C (2×)	FAN1-DRV
B06C (2×)	FAN1-OUT
B06C (2×)	FAN2-DRV
B05H (1×)	FAN-CTRL-1
B06C (1×)	FAN-CTRL-1
B05H (1×)	FAN-CTRL-2
B02B (1×)	FE-CLK
B04N (3×)	FE-CLK
B02B (1×)	FE-DATA0
B04N (3×)	FE-DATA0
B02B (1×)	FE-DATA1
B04N (3×)	FE-DATA1
B02B (1×)	FE-DATA2
B04N (3×)	FE-DATA2
B02B (1×)	FE-DATA3
B04N (3×)	FE-DATA3
B02B (1×)	FE-DATA4
B04N (3×)	FE-DATA4
B02B (1×)	FE-DATA5
B04N (3×)	FE-DATA5
B02B (1×)	FE-DATA6
B04N (3×)	FE-DATA6
B02B (1×)	FE-DATA7
B04N (3×)	FE-DATA7
B04N (4×)	FE-ERR
B02B (1×)	FE-SOP
B04N (3×)	FE-SOP
B02B (1×)	FE-VALID
B04N (3×)	FE-VALID
B04K (1×)	FRONT-C
B08C (2×)	FRONT-C
B04K (1×)	FRONT-Y_CVBS
B08C (2×)	FRONT-Y_CVBS
B10 (2×)	GND-A
B01B (1×)	GND-AUDIO
B10 (16×)	GND-AUDIO
B01A (15×)	GND-SIG
B01C (15×)	GND-SIG1
B04K (1×)	G-VGA
B08B (1×)	G-VGA
B04H (1×)	HDMIA-RX0-
B07E (2×)	HDMIA-RX0-
B04H (1×)	HDMIA-RX0+
B07E (2×)	HDMIA-RX0+
B04H (1×)	HDMIA-RX1-
B07E (2×)	HDMIA-RX1-
B04H (1×)	HDMIA-RX1+
B07E (2×)	HDMIA-RX1+
B04H (1×)	HDMIA-RX2-
B07E (2×)	HDMIA-RX2-
B04H (1×)	HDMIA-RX2+
B07E (2×)	HDMIA-RX2+
B04H (1×)	HDMIA-RXC-
B07E (2×)	HDMIA-RXC-
B04H (1×)	HDMIA-RXC+
B07E (2×)	HDMIA-RXC+
B04H (1×)	HDMIB-RX0-
B07D (1×)	HDMIB-RX0-
B04H (1×)	HDMIB-RX0+
B07D (1×)	HDMIB-RX0+
B04H (1×)	HDMIB-RX1-
B07D (1×)	HDMIB-RX1-
B04H (1×)	HDMIB-RX1+
B07D (1×)	HDMIB-RX1+
B04H (1×)	HDMIB-RX2-
B07D (1×)	HDMIB-RX2-
B04H (1×)	HDMIB-RX2+
B07D (1×)	HDMIB-RX2+
B04H (1×)	HDMIB-RXC-
B07D (1×)	HDMIB-RXC-
B04H (1×)	HDMIB-RXC+
B07D (1×)	HDMIB-RXC+
B04H (1×)	HOT-PLUG
B04H (1×)	HOT-PLUG-A
B07E (1×)	HOT-PLUG-A
B04K (1×)	H-SYNC-VGA
B08B (1×)	H-SYNC-VGA
B04N (1×)	I2C-SCL
B07F (1×)	I2C-SCL
B04N (1×)	I2C-SDA
B07F (1×)	I2C-SDA
B09A (2×)	IDSEL
B02A (1×)	IF-
B02B (1×)	IF-
B02A (1×)	IF+
B02B (1×)	IF+
B02A (2×)	IF-AGC
B02B (1×)	IF-AGC
B04K (1×)	IF-N
B02B (1×)	IF-P
B04K (1×)	IF-P
B09A (1×)	IRQA-mPCI
B09A (1×)	IRQB-mPCI
B04E (2×)	IRQ-CA
B04N (1×)	IRQ-CA
B07A (2×)	IRQ-CA
B04E (2×)	IRQ-PCI
B07G (1×)	IRQ-PCI
B09A (2×)	IRQ-PCI
B01B (1×)	KEYBOARD
B04A (2×)	KEYBOARD
B09B (1×)	KEYBOARD
B04A (3×)	LAMP-ON
B01B (1×)	LAMP-ON-OUT
B04A (1×)	LAMP-ON-OUT
B05E (1×)	LAMP-ON-OUT
B05H (2×)	LCD-PWR-ON
B01B (2×)	LED1
B04A (2×)	LED1
B01B (2×)	LED2
B04A (2×)	LED2
B10 (3×)	LEFT-SPEAKER
B01B (2×)	LIGHT-SENSOR
B04A (1×)	LIGHT-SENSOR
B09A (2×)	M66EN
B07A (4×)	MDO0
B07A (4×)	MDO1
B07A (4×)	MDO2
B07A (4×)	MDO3
B07A (4×)	MDO4
B07A (4×)	MDO5
B07A (4×)	MDO6
B07A (4×)	MDO7
B04A (2×)	MHP-SWITCH
B08D (3×)	MHP-SWITCH
B06A (3×)	MISO
B06F (1×)	MM1-A0
B06G (1×)	MM1-A0
B06F (1×)	MM1-A1
B06G (1×)	MM1-A1
B06F (1×)	MM1-A10
B06G (1×)	MM1-A10
B06F (1×)	MM1-A11
B06G (1×)	MM1-A11
B06F (1×)	MM1-A12
B06G (1×)	MM1-A12
B06F (1×)	MM1-A2
B06G (1×)	MM1-A2
B06F (1×)	MM1-A3
B06G (1×)	MM1-A3
B06F (1×)	MM1-A4
B06G (1×)	MM1-A4
B06F (1×)	MM1-A5
B06G (1×)	MM1-A5
B06F (1×)	MM1-A6
B06G (1×)	MM1-A6
B06F (1×)	MM1-A7
B06G (1×)	MM1-A7
B06F (1×)	MM1-A8
B06G (1×)	MM1-A8
B06F (1×)	MM1-A9
B06G (1×)	MM1-A9
B06F (1×)	MM1-BA0
B06G (1×)	MM1-BA0
B06F (1×)	MM1-BA1
B06G (1×)	MM1-BA1
B06F (1×)	MM1-CAS
B06G (1×)	MM1-CAS
B06F (1×)	MM1-CKE
B06G (1×)	MM1-CKE
B06F (1×)	MM1-CLK-
B06G (1×)	MM1-CLK-
B06F (1×)	MM1-CLK+
B06G (1×)	MM1-CLK+
B06F (1×)	MM1-CS0
B06G (1×)	MM1-CS0
B06F (1×)	MM1-D0
B06G (1×)	MM1-D0
B06F (1×)	MM1-D1
B06G (1×)	MM1-D1
B06F (1×)	MM1-D10
B06G (1×)	MM1-D10
B06F (1×)	MM1-D11
B06G (1×)	MM1-D11
B06F (1×)	MM1-D12
B06G (1×)	MM1-D12
B06F (1×)	MM1-D13
B06G (1×)	MM1-D13
B06F (1×)	MM1-D14
B06G (1×)	MM1-D14
B06F (1×)	MM1-D15
B06G (1×)	MM1-D15
B06F (1×)	MM1-D2
B06G (1×)	MM1-D2
B06F (1×)	MM1-D3
B06G (1×)	MM1-D3
B06F (1×)	MM1-D4
B06G (1×)	MM1-D4
B06F (1×)	MM1-D5
B06G (1×)	MM1-D5
B06F (1×)	MM1-D6
B06G (1×)	MM1-D6
B06F (1×)	MM1-D7
B06G (1×)	MM1-D7
B06F (1×)	MM1-D8
B06G (1×)	MM1-D8
B06F (1×)	MM1-D9
B06G (1×)	MM1-D9
B06F (1×)	MM1-DQS0
B06G (1×)	MM1-DQS0
B06F (1×)	MM1-DQS1
B06G (1×)	MM1-DQS1
B06F (1×)	MM1-RAS
B06G (1×)	MM1-RAS

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SSB: SRP List Part 2

Netname	Schematic
B06F (1x)	MM1-WE
B06G (1x)	MM1-WE
B07A (4x)	MOCLK_VS2
B06A (3x)	MOSI
B07A (4x)	MOSTRT
B07A (4x)	MOVAL
B09A (2x)	MPCIACT
B06G (1x)	MSEL0
B06G (1x)	MSEL1
B06G (1x)	MSEL2
B06G (1x)	MSEL3
B07F (2x)	NAND-AD(0)
B07F (2x)	NAND-AD(1)
B07F (2x)	NAND-AD(2)
B07F (2x)	NAND-AD(3)
B07F (2x)	NAND-AD(4)
B07F (2x)	NAND-AD(5)
B07F (2x)	NAND-AD(6)
B07F (2x)	NAND-AD(7)
B07F (2x)	NAND-ALE
B07F (2x)	NAND-CLE
B07F (2x)	NAND-REn
B07F (2x)	NAND-WEn
B06G (2x)	nCE
B06G (2x)	nCONFIG
B06E (1x)	nCSO
B06G (1x)	nCSO
B06G (2x)	nSTATUS
B07D (6x)	PCEC-HDMI
B07E (2x)	PCEC-HDMI
B04F (1x)	PCI-AD0
B05G (1x)	PCI-AD0
B07F (1x)	PCI-AD0
B07G (1x)	PCI-AD0
B07H (1x)	PCI-AD0
B09A (1x)	PCI-AD0
B04F (1x)	PCI-AD1
B05G (1x)	PCI-AD1
B07F (1x)	PCI-AD1
B07G (1x)	PCI-AD1
B07H (2x)	PCI-AD1
B09A (1x)	PCI-AD1
B04F (1x)	PCI-AD10
B05G (1x)	PCI-AD10
B07G (1x)	PCI-AD10
B07H (1x)	PCI-AD10
B09A (1x)	PCI-AD10
B04F (1x)	PCI-AD11
B05G (1x)	PCI-AD11
B07G (1x)	PCI-AD11
B07H (1x)	PCI-AD11
B09A (2x)	PCI-AD11
B04F (1x)	PCI-AD12
B05G (1x)	PCI-AD12
B07G (1x)	PCI-AD12
B07H (1x)	PCI-AD12
B09A (2x)	PCI-AD12
B04F (1x)	PCI-AD13
B05G (1x)	PCI-AD13
B07G (1x)	PCI-AD13
B07H (1x)	PCI-AD13
B09A (2x)	PCI-AD13
B04F (1x)	PCI-AD14
B05G (1x)	PCI-AD14
B07G (1x)	PCI-AD14
B07H (1x)	PCI-AD14
B09A (1x)	PCI-AD14
B04F (1x)	PCI-AD15
B05G (1x)	PCI-AD15
B07G (1x)	PCI-AD15
B09A (1x)	PCI-AD15
B04F (1x)	PCI-AD16
B05G (1x)	PCI-AD16
B07G (1x)	PCI-AD16
B07H (1x)	PCI-AD16
B09A (1x)	PCI-AD16
B04F (1x)	PCI-AD17
B05G (1x)	PCI-AD17
B07G (1x)	PCI-AD17
B07H (1x)	PCI-AD17
B09A (1x)	PCI-AD17
B04F (1x)	PCI-AD18
B05G (1x)	PCI-AD18
B07G (1x)	PCI-AD18
B07H (1x)	PCI-AD18
B09A (1x)	PCI-AD18
B04F (1x)	PCI-AD19
B05G (1x)	PCI-AD19
B07G (1x)	PCI-AD19
B07H (1x)	PCI-AD19
B09A (1x)	PCI-AD19
B04F (1x)	PCI-AD2
B05G (1x)	PCI-AD2
B07G (1x)	PCI-AD2
B07H (1x)	PCI-AD2
B09A (1x)	PCI-AD2
B04F (1x)	PCI-AD20
B05G (1x)	PCI-AD20
B07G (1x)	PCI-AD20
B09A (1x)	PCI-AD20
B04F (1x)	PCI-AD21
B05G (1x)	PCI-AD21
B07G (1x)	PCI-AD21
B09A (1x)	PCI-AD21
B04F (1x)	PCI-AD22
B05G (1x)	PCI-AD22
B07G (1x)	PCI-AD22
B07H (1x)	PCI-AD22
B09A (1x)	PCI-AD22
B04F (1x)	PCI-AD23
B05G (1x)	PCI-AD23
B07G (2x)	PCI-AD23
B07H (1x)	PCI-AD23
B09A (1x)	PCI-AD23
B04F (2x)	PCI-AD24
B05G (1x)	PCI-AD24
B07F (1x)	PCI-AD24
B07G (1x)	PCI-AD24
B07H (1x)	PCI-AD24
B09A (1x)	PCI-AD24
B04F (1x)	PCI-AD25
B05G (2x)	PCI-AD25
B07F (1x)	PCI-AD25
B07G (1x)	PCI-AD25
B07H (1x)	PCI-AD25
B09A (1x)	PCI-AD25
B04F (1x)	PCI-AD26
B05G (1x)	PCI-AD26
B07F (1x)	PCI-AD26
B07G (1x)	PCI-AD26
B07H (1x)	PCI-AD26
B09A (1x)	PCI-AD26
B04F (1x)	PCI-AD27
B05G (1x)	PCI-AD27
B07F (1x)	PCI-AD27
B07G (1x)	PCI-AD27
B07H (1x)	PCI-AD27
B09A (1x)	PCI-AD27
B04F (1x)	PCI-AD28
B05G (1x)	PCI-AD28
B07F (1x)	PCI-AD28
B07G (1x)	PCI-AD28
B07H (1x)	PCI-AD28
B09A (1x)	PCI-AD28
B04F (1x)	PCI-AD29
B05G (1x)	PCI-AD29
B07F (1x)	PCI-AD29
B07G (1x)	PCI-AD29
B07H (1x)	PCI-AD29
B09A (1x)	PCI-AD29
B04F (1x)	PCI-AD3
B05G (1x)	PCI-AD3
B07G (1x)	PCI-AD3
B07H (1x)	PCI-AD3
B09A (1x)	PCI-AD3
B04F (1x)	PCI-AD30
B05G (1x)	PCI-AD30
B07F (1x)	PCI-AD30
B07G (1x)	PCI-AD30
B07H (1x)	PCI-AD30
B09A (1x)	PCI-AD30
B04F (1x)	PCI-AD31
B05G (1x)	PCI-AD31
B07F (1x)	PCI-AD31
B07G (1x)	PCI-AD31
B07H (1x)	PCI-AD31
B09A (1x)	PCI-AD31
B04F (1x)	PCI-AD4
B05G (1x)	PCI-AD4
B07G (1x)	PCI-AD4
B07H (1x)	PCI-AD4
B09A (1x)	PCI-AD4
B04F (1x)	PCI-AD5
B05G (1x)	PCI-AD5
B07G (1x)	PCI-AD5
B07H (1x)	PCI-AD5
B09A (1x)	PCI-AD5
B04F (1x)	PCI-AD6
B05G (1x)	PCI-AD6
B07G (1x)	PCI-AD6
B07H (1x)	PCI-AD6
B09A (1x)	PCI-AD6
B04F (1x)	PCI-AD7
B05G (1x)	PCI-AD7
B07G (1x)	PCI-AD7
B07H (1x)	PCI-AD7
B09A (1x)	PCI-AD7
B04F (1x)	PCI-AD8
B05G (1x)	PCI-AD8
B07G (1x)	PCI-AD8
B07H (1x)	PCI-AD8
B09A (1x)	PCI-AD8
B04F (1x)	PCI-AD9
B05G (1x)	PCI-AD9
B07G (1x)	PCI-AD9
B07H (1x)	PCI-AD9
B09A (1x)	PCI-AD9
B04F (1x)	PCI-CBE0
B05G (1x)	PCI-CBE0
B07G (1x)	PCI-CBE0
B09A (1x)	PCI-CBE0
B04F (1x)	PCI-CBE1
B05G (1x)	PCI-CBE1
B07F (1x)	PCI-CBE1
B07G (1x)	PCI-CBE1
B07H (1x)	PCI-CBE1
B09A (1x)	PCI-CBE1
B04F (1x)	PCI-CBE2
B05G (1x)	PCI-CBE2
B07F (1x)	PCI-CBE2
B07G (1x)	PCI-CBE2
B07H (1x)	PCI-CBE2
B09A (1x)	PCI-CBE2
B04F (1x)	PCI-CBE3
B05G (1x)	PCI-CBE3
B07G (1x)	PCI-CBE3
B09A (1x)	PCI-CBE3
B04F (2x)	PCI-CLK-ETHERNET
B07G (1x)	PCI-CLK-ETHERNET
B04F (2x)	PCI-CLK-MINI
B09A (1x)	PCI-CLK-MINI
B04E (1x)	PCI-CLK-OUT
B04F (3x)	PCI-CLK-OUT
B04F (2x)	PCI-CLK-PNX5100
B05G (1x)	PCI-CLK-PNX5100
B04F (3x)	PCI-CLK-PNX8535
B09A (2x)	PCI-CLKRUN
B04F (2x)	PCI-DEVSEL
B05G (1x)	PCI-DEVSEL
B07G (1x)	PCI-DEVSEL
B09A (1x)	PCI-DEVSEL
B04F (2x)	PCI-FRAME
B05G (1x)	PCI-FRAME
B07G (1x)	PCI-FRAME
B09A (1x)	PCI-FRAME
B04F (2x)	PCI-GNT
B04F (2x)	PCI-GNT-B
B04F (1x)	PCI-GNT-ETH
B07G (1x)	PCI-GNT-ETH
B04F (1x)	PCI-GNT-MINI
B09A (1x)	PCI-GNT-MINI
B04F (2x)	PCI-IRDY
B05G (1x)	PCI-IRDY
B07G (1x)	PCI-IRDY
B09A (1x)	PCI-IRDY
B04F (1x)	PCI-PAR
B05G (1x)	PCI-PAR
B07G (1x)	PCI-PAR
B09A (1x)	PCI-PAR
B04F (2x)	PCI-PERR
B05G (1x)	PCI-PERR
B07G (1x)	PCI-PERR
B09A (1x)	PCI-PERR
B04F (2x)	PCI-REQ
B04F (2x)	PCI-REQ-B
B04F (1x)	PCI-REQ-ETH
B07G (1x)	PCI-REQ-ETH
B04F (1x)	PCI-REQ-MINI
B09A (1x)	PCI-REQ-MINI
B04F (2x)	PCI-SERR
B05G (1x)	PCI-SERR
B07G (1x)	PCI-SERR
B09A (1x)	PCI-SERR
B04F (2x)	PCI-STOP
B05G (1x)	PCI-STOP
B07G (1x)	PCI-STOP
B09A (1x)	PCI-STOP
B04F (2x)	PCI-TRDY
B05G (1x)	PCI-TRDY
B07G (1x)	PCI-TRDY
B09A (1x)	PCI-TRDY
B07A (1x)	PCMCIA-A0
B07H (1x)	PCMCIA-A0
B07A (1x)	PCMCIA-A1
B07H (1x)	PCMCIA-A1
B07A (1x)	PCMCIA-A10
B07H (1x)	PCMCIA-A10
B07A (1x)	PCMCIA-A11
B07H (1x)	PCMCIA-A11
B07A (1x)	PCMCIA-A12
B07H (1x)	PCMCIA-A12
B07A (1x)	PCMCIA-A13
B07H (1x)	PCMCIA-A13
B07A (1x)	PCMCIA-A14
B07H (1x)	PCMCIA-A14
B07A (1x)	PCMCIA-A2
B07H (1x)	PCMCIA-A2
B07A (1x)	PCMCIA-A3
B07H (1x)	PCMCIA-A3
B07A (1x)	PCMCIA-A4
B07H (1x)	PCMCIA-A4
B07A (1x)	PCMCIA-A5
B07H (1x)	PCMCIA-A5
B07A (1x)	PCMCIA-A6
B07H (1x)	PCMCIA-A6
B07A (1x)	PCMCIA-A7
B07H (1x)	PCMCIA-A7
B07A (1x)	PCMCIA-A8
B07H (1x)	PCMCIA-A8
B07A (1x)	PCMCIA-A9
B07H (1x)	PCMCIA-A9
B07A (1x)	PCMCIA-D0
B07H (1x)	PCMCIA-D0
B07A (1x)	PCMCIA-D1
B07H (1x)	PCMCIA-D1
B07A (1x)	PCMCIA-D2
B07H (1x)	PCMCIA-D2
B07A (1x)	PCMCIA-D3
B07H (1x)	PCMCIA-D3
B07A (1x)	PCMCIA-D4
B07H (1x)	PCMCIA-D4
B07A (1x)	PCMCIA-D5
B07H (1x)	PCMCIA-D5
B07A (1x)	PCMCIA-D6
B07H (1x)	PCMCIA-D6
B07A (1x)	PCMCIA-D7
B07H (1x)	PCMCIA-D7
B07A (5x)	PCMCIA-VCC-VPP
B02A (2x)	PDN
B02B (1x)	PDN
B02A (1x)	PDP
B02B (1x)	PDP
B09A (2x)	PME
B05A (3x)	PNX5100-DDR2-A0
B05A (3x)	PNX5100-DDR2-A1
B05A (3x)	PNX5100-DDR2-A10
B05A (3x)	PNX5100-DDR2-A11
B05A (3x)	PNX5100-DDR2-A12
B05A (3x)	PNX5100-DDR2-A2
B05A (3x)	PNX5100-DDR2-A3
B05A (3x)	PNX5100-DDR2-A4
B05A (3x)	PNX5100-DDR2-A5
B05A (3x)	PNX5100-DDR2-A6
B05A (3x)	PNX5100-DDR2-A7
B05A (3x)	PNX5100-DDR2-A8
B05A (3x)	PNX5100-DDR2-A9
B05A (3x)	PNX5100-DDR2-BA0
B05A (3x)	PNX5100-DDR2-BA1
B05A (3x)	PNX5100-DDR2-CAS
B05A (3x)	PNX5100-DDR2-CKE
B05A (3x)	PNX5100-DDR2-CLK_N
B05A (3x)	PNX5100-DDR2-CLK_P
B05A (3x)	PNX5100-DDR2-CS
B05A (2x)	PNX5100-DDR2-D0
B05A (2x)	PNX5100-DDR2-D1
B05A (2x)	PNX5100-DDR2-D10
B05A (2x)	PNX5100-DDR2-D11
B05A (2x)	PNX5100-DDR2-D12
B05A (2x)	PNX5100-DDR2-D13
B05A (2x)	PNX5100-DDR2-D14
B05A (2x)	PNX5100-DDR2-D15
B05A (2x)	PNX5100-DDR2-D16
B05A (2x)	PNX5100-DDR2-D17
B05A (2x)	PNX5100-DDR2-D18
B05A (2x)	PNX5100-DDR2-D19
B05A (2x)	PNX5100-DDR2-D2
B05A (2x)	PNX5100-DDR2-D20
B05A (2x)	PNX5100-DDR2-D21
B05A (2x)	PNX5100-DDR2-D22
B05A (2x)	PNX5100-DDR2-D23
B05A (2x)	PNX5100-DDR2-D24
B05A (2x)	PNX5100-DDR2-D25
B05A (2x)	PNX5100-DDR2-D26
B05A (2x)	PNX5100-DDR2-D27
B05A (2x)	PNX5100-DDR2-D28
B05A (2x)	PNX5100-DDR2-D29
B05A (2x)	PNX5100-DDR2-D3
B05A (2x)	PNX5100-DDR2-D30
B05A (2x)	PNX5100-DDR2-D31
B05A (2x)	PNX5100-DDR2-D4
B05A (2x)	PNX5100-DDR2-D5
B05A (2x)	PNX5100-DDR2-D6
B05A (2x)	PNX5100-DDR2-D7
B05A (2x)	PNX5100-DDR2-D8
B05A (2x)	PNX5100-DDR2-D9
B05A (2x)	PNX5100-DDR2-DQM0
B05A (2x)	PNX5100-DDR2-DQM1
B05A (2x)	PNX5100-DDR2-DQM2
B05A (2x)	PNX5100-DDR2-DQM3
B05A (2x)	PNX5100-DDR2-DQS0_N
B05A (2x)	PNX5100-DDR2-DQS0_P
B05A (2x)	PNX5100-DDR2-DQS1_N
B05A (2x)	PNX5100-DDR2-DQS1_P
B05A (2x)	PNX5100-DDR2-DQS2_N
B05A (2x)	PNX5100-DDR2-DQS2_P
B05A (2x)	PNX5100-DDR2-DQS3_N
B05A (2x)	PNX5100-DDR2-DQS3_P
B05A (3x)	PNX5100-DDR2-ODT
B05A (3x)	PNX5100-DDR2-RAS
B05A (2x)	PNX5100-DDR2-VREF-CTRL
B05A (3x)	PNX5100-DDR2-VREF-DDR
B05A (3x)	PNX5100-DDR2-WE
B05F (1x)	PNX5100-RST-OUT
B05I (1x)	PNX5100-RST-OUT
B01B (1x)	POWER-OK
B04A (2x)	POWER-OK
B06A (2x)	PROG-B
B04A (2x)	PSEN
B01B (1x)	RC
B04A (2x)	RC
B04A (1x)	RC-IN
B08C (1x)	RC-IN
B04A (1x)	RC-OUT
B08C (1x)	RC-OUT
B04A (4x)	RC-UP
B08D (1x)	RC-UP
B07D (2x)	REF-3V3
B04A (2x)	REGIMBEAU_CVBS-SWITCH
B08A (1x)	REGIMBEAU_CVBS-SWITCH
B04A (2x)	RESET-AUDIO
B04M (2x)	RESET-AUDIO
B04N (1x)	RESET-BOLT-ON
B07F (1x)	RESET-BOLT-ON
B04A (2x)	RESET-ETHERNET
B07G (2x)	RESET-ETHERNET
B09A (1x)	RESET-ETHERNET
B09A (2x)	RESET-mPCI
B04A (3x)	RESET-NVM
B04A (2x)	RESET-PNX5100
B05F (1x)	RESET-PNX5100
B04A (2x)	RESET-STBY
B02B (1x)	RESET-SYSTEM
B04A (2x)	RESET-SYSTEM
B04B (1x)	RESET-SYSTEM
B04E (1x)	RESET-SYSTEM
B02A (4x)	RF-AGC
B02B (1x)	RF-AGC
B10 (3x)	RIGHT-SPEAKER
B04H (1x)	RREF-PNX85XX
B04P (2x)	RREF-PNX85XX
B04K (1x)	R-VGA
B08B (1x)	R-VGA
B05B (1x)	RX51001A-
B06D (3x)	RX51001A-
B05B (1x)	RX51001A+
B06D (3x)	RX51001A+
B05B (1x)	RX51001B-
B06D (3x)	RX51001B-
B05B (1x)	RX51001B+
B06D (3x)	RX51001B+
B05B (1x)	RX51001C-
B06D (3x)	RX51001C-
B05B (1x)	RX51001C+
B06D (3x)	RX51001C+
B05B (1x)	RX51001CLK-
B06D (3x)	RX51001CLK-
B05B (1x)	RX51001CLK+
B06D (3x)	RX51001CLK+
B05B (1x)	RX51001D-
B06D (3x)	RX51001D-
B05B (1x)	RX51001D+
B06D (3x)	RX51001D+
B05B (1x)	RX51001E-
B06D (3x)	RX51001E-
B05B (1x)	RX51001E+
B06D (3x)	RX51001E+
B05B (1x)	RX51002A-
B06D (3x)	RX51002A-
B05B (1x)	RX51002A+
B06D (3x)	RX51002A+
B05B (1x)	RX51002B-
B06D (3x)	RX51002B-
B05B (1x)	RX51002B+
B06D (3x)	RX51002B+
B05B (1x)	RX51002C-
B06D (3x)	RX51002C-
B05B (1x)	RX51002C+
B06D (3x)	RX51002C+
B05B (1x)	RX51002CLK-
B06D (3x)	RX51002CLK-
B05B (1x)	RX51002CLK+
B06D (3x)	RX51002CLK+
B05B (1x)	RX51002D-
B06D (3x)	RX51002D-
B05B (1x)	RX51002D+
B06D (3x)	RX51002D+
B05B (1x)	RX51002E-
B06D (3x)	RX51002E-
B05B (1x)	RX51002E+
B06D (3x)	RX51002E+
B08D (3x)	RXD
B04E (2x)	RXD-MIPS
B08D (3x)	RXD-MIPS
B04E (2x)	RXD-MIPS2
B06B (1x)	RXD-MIPS2
B04A (2x)	RXD-UP
B08D (4x)	RXD-UP
B04E (2x)	SCL1
B04E (3x)	SCL2
B04E (2x)	SCL3
B05F (1x)	SCL-AMBI-3V3
B06A (1x)	SCL-AMBI-3V3
B06G (1x)	SCL-AMBI-3V3
B04N (1x)	SCL-BOLT-ON
B06A (3x)	SCL-BOLT-ON
B08D (1x)	SCL-BOLT-ON
B05E (2x)	SCL-DISP
B06A (3x)	SCL-DISP
B06D (1x)	SCL-DISP
B01B (1x)	SCL-SET
B04E (2x)	SCL-SET
B06A (5x)	SCL-SET
B06C (2x)	SCL-SET
B06A (2x)	SCL-SET0
B06A (2x)	SCL-SET1
B02B (2x)	SCL-SSB
B04E (2x)	SCL-SSB
B05F (2x)	SCL-SSB
B06A (1x)	SCL-SSB
B06G (1x)	SCL-SSB
B07D (1x)	SCL-SSB
B08D (1x)	SCL-SSB
B04A (3x)	SCL-UP-MIPS
B04E (3x)	SCL-UP-MIPS
B04E (2x)	SDA1
B04E (3x)	SDA2
B04E (2x)	SDA3
B05F (1x)	SDA-AMBI-3V3
B06A (1x)	SDA-AMBI-3V3
B06G (1x)	SDA-AMBI-3V3
B04N (1x)	SDA-BOLT-ON
B06A (3x)	SDA-BOLT-ON
B08D (1x)	SDA-BOLT-ON
B05E (2x)	SDA-DISP
B06A (3x)	SDA-DISP
B06D (1x)	SDA-DISP
B01B (1x)	SDA-SET
B04E (2x)	SDA-SET
B06A (5x)	SDA-SET
B06C (2x)	SDA-SET
B06A (2x)	SDA-SET0
B06A (2x)	SDA-SET1
B02B (2x)	SDA-SSB
B04E (2x)	SDA-SSB
B05F (2x)	SDA-SSB
B06A (1x)	SDA-SSB
B06G (1x)	SDA-SSB
B07D (1x)	SDA-SSB
B08D (1x)	SDA-SSB
B04A (3x)	SDA-UP-MIPS
B04E (3x)	SDA-UP-MIPS
B04A (2x)	SDM
B04B (1x)	SDM
B04P (2x)	SENSE+1V2-PNX85XX
B04L (1x)	SPDIF-IN1
B08D (1x)	SPDIF-IN1
B04L (1x)	SPDIF-OUT
B08B (1x)	SPDIF-OUT
B04A (2x)	SPI-CLK
B04A (2x)	SPI-CSB
B04A (2x)	SPI-PROG
B04B (1x)	SPI-PROG
B04A (3x)	SPI-SDI
B04A (2x)	SPI-SDO
B04A (3x)	SPI-WP
B01B (1x)	STANDBY
B04A (2x)	STANDBY
B08D (1x)	STANDBY
B04A (2x)	SUPPLY-FAULT
B06C (2x)	TACHO1
B06C (2x)	TACHO1-INV
B06C (2x)	TACHO2
B06C (2x)	TACHO2-INV
B06E (1x)	TCK
B06G (1x)	TCK
B06E (1x)	TDI
B06G (1x)	TDI
B06E (1x)	TDO
B06G (1x)	TDO
B06E (1x)	TMS
B06G (1x)	TMS
B04N (2x)	TSINO-DATA0
B07F (1x)	TSINO-DATA0
B04N (2x)	TSINO-DATA1
B07F (1x)	TSINO-DATA1
B04N (2x)	TSINO-DATA2
B07F (1x)	TSINO-DATA2
B04N (2x)	TSINO-DATA3
B07F (1x)	TSINO-DATA3
B04N (2x)	TSINO-DATA4
B07F (1x)	TSINO-DATA4
B04N (2x)	TSINO-DATA5
B07F (1x)	TSINO-DATA5
B04N (2x)	TSINO-DATA6
B07F (1x)	TSINO-DATA6
B04N (2x)	TSINO-DATA7
B07F (1x)	TSINO-DATA7
B04N (2x)	TSO-BIT-CLK
B07F (1x)	TSO-BIT-CLK
B04N (2x)	TSO-BIT-ERR
B04N (2x)	TSO-BIT-VALID
B07F (1x)	TSO-BIT-VALID
B04N (2x)	TSO-SYNC
B07F (1x)	TSO-SYNC
B02A (5x)	TUN-P1
B02A (5x)	TUN-P10
B02A (4x)	TUN-P11
B02A (5x)	TUN-P2
B02A (6x)	TUN-P3
B02A (5x)	TUN-P4
B02A (5x)	TUN-P5
B02A (5x)	TUN-P6
B02A (5x)	TUN-P7
B02A (5x)	TUN-P8
B02A (6x)	TUN-P9
B02A (2x)	TUN-SCL
B02B (2x)	TUN-SCL
B02A (2x)	TUN-SDA
B02B (2x)	TUN-SDA
B05E (3x)	TX1A-
B05E (3x)	TX1A+
B05E (3x)	TX1B-
B05E (3x)	TX1B+
B05E (3x)	TX1C-
B05E (3x)	TX1C+
B05E (3x)	TX1CLK-
B05E (3x)	TX1CLK+
B05E (3x)	TX1D-
B05E (3x)	TX1D+
B05E (3x)	TX1E-
B05E (3x)	TX1E+
B05E (3x)	TX2A-
B05E (3x)	TX2A+
B05E (3x)	TX2B-
B05E (3x)	TX2B+
B05E (3x)	TX2C-
B05E (3x)	TX2C+
B05E (3x)	TX2CLK-
B05E (3x)	TX2CLK+
B05E (3x)	TX2D-
B05E (3x)	TX2D+
B05E (3x)	TX2E-
B05E (3x)	TX2E+
B05E (3x)	TX3A-
B05E (3x)	TX3A+
B05E (3x)	TX3B-
B05E (3x)	TX3B+
B05E (3x)	TX3C-
B05E (3x)	TX3C+
B05E (3x)	TX3CLK-
B05E (3x)	TX3CLK+
B05E (3x)	TX3D-
B05E (3x)	TX3D+
B05E (3x)	TX3E-
B05E (3x)	TX3E+
B05E (3x)	TX4A-
B05E (3x)	TX4A+
B05E (3x)	TX4B-
B05E (3x)	TX4B+
B05E (3x)	TX4C-
B05E (3x)	TX4C+
B05E (3x)	TX4CLK-
B05E (3x)	TX4CLK+
B05E (3x)	TX4D-
B05E (3x)	TX4D+
B05E (3x)	TX4E-
B05E (3x)	TX4E+
B04O (1x)	TX851A-
B06D (1x)	TX851A-
B06G (1x)	TX851A-
B04O (1x)	TX851A+
B06D (1x)	TX851A+
B06G (1x)	TX851A+
B04O (1x)	TX851B-
B06D (1x)	TX851B-
B06G (1x)	TX851B-
B04O (1x)	TX851B+
B06D (1x)	TX851B+
B06G (2x)	TX851B+
B04O (1x)	TX851C-
B06D (1x)	TX851C-
B06G (1x)	TX851C-
B04O (1x)	TX851C+
B06D (1x)	TX851C+
B06G (1x)	TX851C+
B04O (1x)	TX851CLK-
B06D (1x)	TX851CLK-
B06G (1x)	TX851CLK-
B04O (1x)	TX851CLK+
B06D (1x)	TX851CLK+
B06G (1x)	TX851CLK+
B04O (1x)	TX851D-
B06D (1x)	TX851D-
B06G (1x)	TX851D-
B04O (1x)	TX851D+
B06D (1x)	TX851D+
B06G (1x)	TX851D+
B04O (1x)	TX851E-
B06D (1x)	TX851E-
B06G (1x)	TX851E-
B04O (1x)	TX851E+
B06D (1x)	TX851E+
B06G (1x)	TX851E+
B04O (1x)	TX852A-
B06D (1x)	TX852A-
B06G (1x)	TX852A-
B04O (1x)	TX852A+
B06D (1x)	TX852A+
B06G (1x)	TX852A+
B04O (1x)	TX852B-
B06D (1x)	TX852B-
B06G (1x)	TX852B-
B04O (1x)	TX852B+
B06D (1x)	TX852B+
B06G (1x)	TX852B+
B04O (1x)	TX852C-
B06D (1x)	TX852C-
B06G (1x)	TX852C-
B04O (1x)	TX852C+
B06D (1x)	TX852C+
B06G (1x)	TX852C+
B04O (1x)	TX852CLK-
B06D (1x)	TX852CLK-
B06G (1x)	TX852CLK-
B04O (1x)	TX852CLK+
B06D (1x)	TX852CLK+
B06G (1x)	TX852CLK+
B04O (1x)	TX852D-
B06D (1x)	TX852D-
B06G (1x)	TX852D-
B04O (1x)	TX852D+
B06D (1x)	TX852D+
B06G (1x)	TX852D+
B04O (1x)	TX852E-
B06D (1x)	TX852E-
B06G (1x)	TX852E-
B04O (1x)	TX852E+
B06D (1x)	TX852E+
B06G (1x)	TX852E+
B05E (1x)	TXCLK-
B06A (1x)	TXCLK-
B05E (1x)	TXCLK+
B06A (1x)	TXCLK+
B08D (3x)	TXD
B05E (1x)	TXDAT-
B06A (1x)	TXDAT-
B05E (1x)	TXDAT+
B06A (1x)	TXDAT+
B04E (2x)	TXD-MIPS
B08D (3x)	TXD-MIPS
B04E (2x)	TXD-MIPS2
B06B (1x)	TXD-MIPS2
B04A (2x)	TXD-UP
B08D (4x)	TXD-UP
B06D (1x)	TXF1A-
B06G (1x)	TXF1A-
B06D (1x)	TXF1A+
B06G (1x)	TXF1A+
B06D (1x)	TXF1B-
B06G (1x)	TXF1B-
B06D (1x)	TXF1B+
B06G (1x)	TXF1B+
B06D (1x)	TXF1C-
B06G (1x)	TXF1C-
B06D (1x)	TXF1C+
B06G (1x)	TXF1C+
B06D (1x)	TXF1CLK-
B06G (1x)	TXF1CLK-
B06D (1x)	TXF1CLK+
B06G (1x)	TXF1CLK+
B06D (1x)	TXF1D-
B06G (1x)	TXF1D-
B06D (1x)	TXF1D+
B06G (1x)	TXF1D+
B06D (1x)	TXF1E-
B06G (1x)	TXF1E-
B06D (1x)	TXF1E+
B06G (1x)	TXF1E+
B06D (1x)	TXF2A-
B06G (1x)	TXF2A-
B06D (1x)	TXF2A+
B06G (1x)	TXF2A+
B06D (1x)	TXF2B-
B06G (1x)	TXF2B-
B06D (1x)	TXF2B+
B06G (1x)	TXF2B+
B06D (1x)	TXF2C-
B06G (1x)	TXF2C-
B06D (1x)	TXF2C+
B06G (1x)	TXF2C+
B06D (1x)	TXF2CLK-
B06G (1x)	TXF2CLK-
B06D (1x)	TXF2CLK+
B06G (1x)	TXF2CLK+
B06D (1x)	TXF2D-
B06G (1x)	TXF2D-
B06D (1x)	TXF2D+
B06G (1x)	TXF2D+
B06D (1x)	TXF2E-
B06G (1x)	TXF2E-
B06D (1x)	TXF2E+
B06G (1x)	TXF2E+
B04A (2x)	UART-SWITCH
B08D (2x)	UART-SWITCH
B08D (2x)	UART-SWITCHn
B04E (2x)	USB20-DM
B07C (1x)	USB20-DM
B04E (2x)	USB20-DP
B07C (1x)	USB20-DP
B04E (1x)	USB-OC
B07C (1x)	USB-OC
B04P (2x)	VDDA-ADC
B04L (4x)	VDDA-AUDIO
B04P (2x)	VDDA-AUDIO
B04L (1x)	VDDA-DAC
B04P (2x)	VDDA-DAC
B04O (1x)	VDDA-LVDS
B04P (1x)	VDDA-LVDS
B06F (2x)	VREF-DDR1
B06F (1x)	VREF-FPGA1
B06G (16x)	VREF-FPGA1
B01A (1x)	VSW
B01B (1x)	VSW
B04K (1x)	V-SYNC-VGA
B08B (1x)	V-SYNC-VGA
B04E (1x)	WC-EEPROM-PNX5100
B05F (2x)	WC-EEPROM-PNX5100
B07D (1x)	WC-EEPROM-PNX5100
B04A (2x)	WP-NANDFLASH
B07F (2x)	WP-NANDFLASH
B07D (1x)	WRITE-PROT
B07E (1x)	WRITE-PROT
B08B (1x)	WRITE-PROT
B04F (1x)	XIO-ACK
B07F (2x)	XIO-ACK
B04F (1x)	XIO-SEL-NAND
B07F (2x)	XIO-SEL-NAND
B04K (1x)	Y_CVBS-MON-OUT
B08B (1x)	Y_CVBS-MON-OUT
B08A (1x)	Y_CVBS-MON-OUT-SC
B08B (1x)	Y_CVBS-MON-OUT-SC

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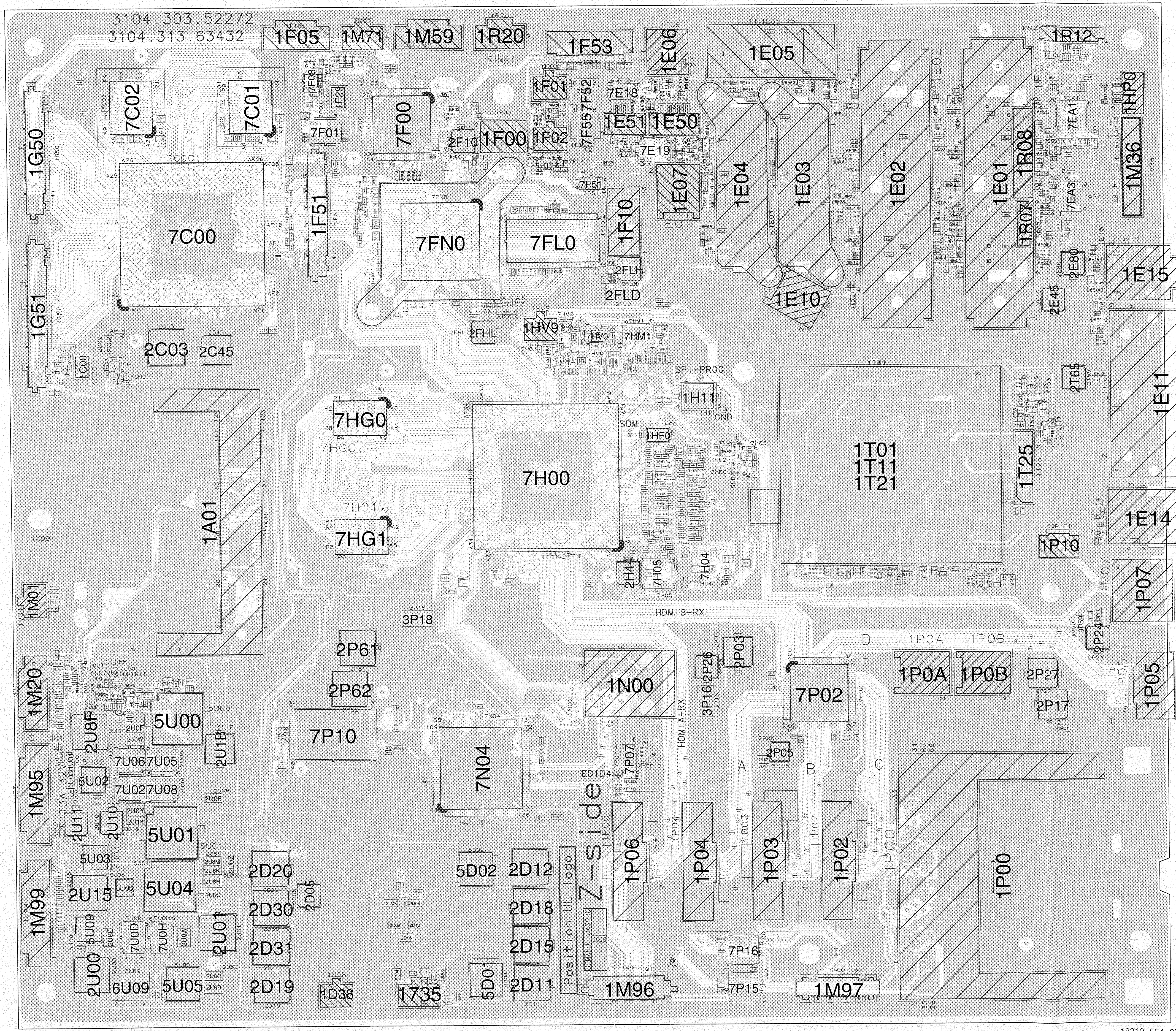
Layout Small Signal Board (Top Side)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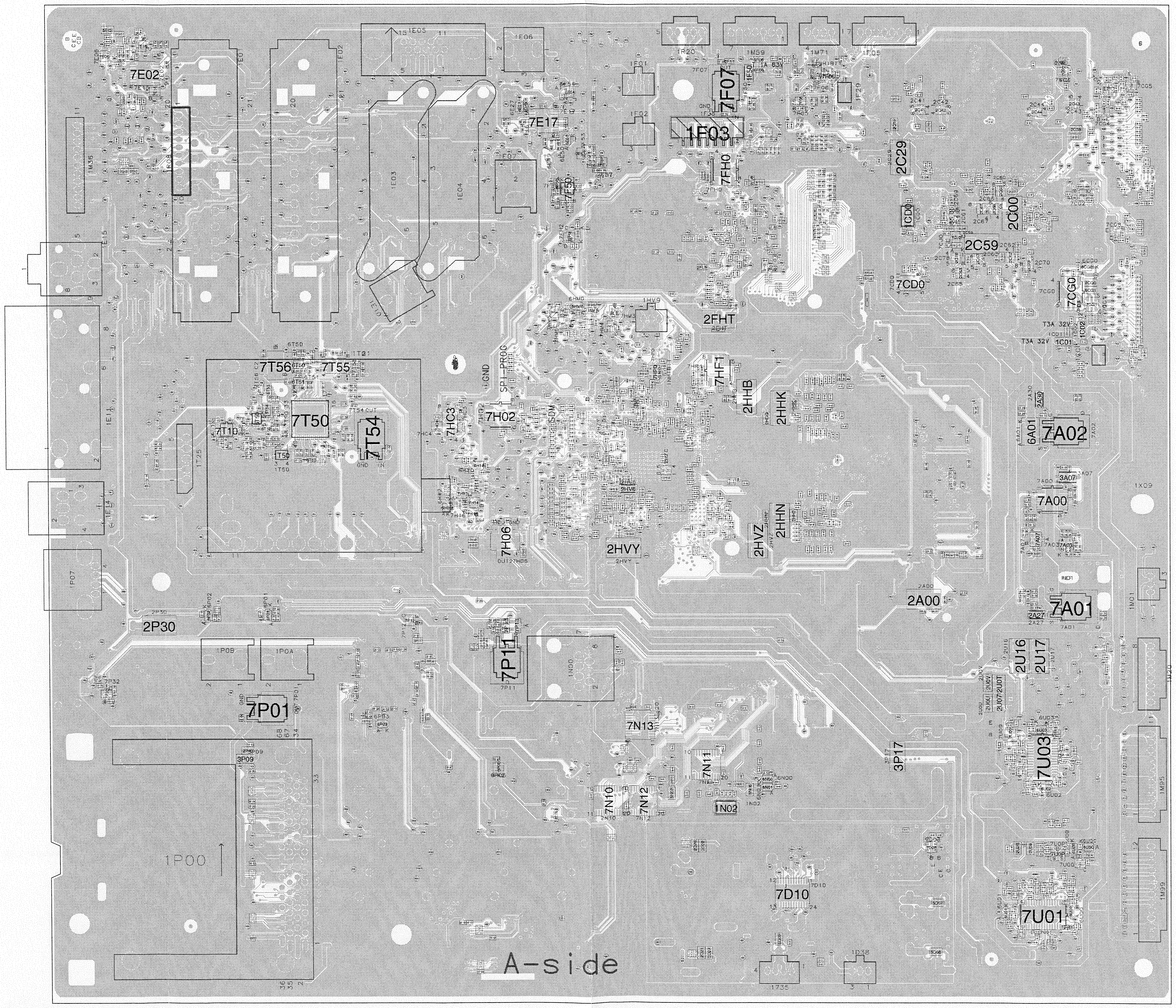
1F01
7E18
1E51
1E50
1HP0
1G50
2F10
1F00
1F02
7F55
7F52
7E19
1M36
7C00
1F51
7FN0
7FL0
1F10
1E07
1E04
1E03
1E02
1E01
1R08
1R07
7EA1
7EA3
2FLH
2FLD
1E10
2E80
2E45
1E15
1G51
2FHL
1HV9
7HV0
7HM1
2C03
2C45
SPI-PROG
1H11
GND
2T65
1E11
7HG0
SDM
1HF0
7H00
1T01
1T11
1T21
1T25
1A01
7HG1
1E14
1P10
2H44
7H05
7H04
1M01
3P18
HDMIB-RX
1P07
2P24
2P61
2P03
2P26
1P0A
1P0B
2P27
1M20
2P62
1N00
3P16
7P02
2P17
1P05
2U8F
5U00
7P10
7N04
HDMIA-RX
2U1B
7U06
7U05
2P05
5U02
7U02
7U08
EDID4
7P07
1M95
2U11
2U10
5U01
Z-side
1P06
1P04
1P03
1P02
1P00
5U03
2D20
5D02
2D12
2U15
5U04
2D05
2D30
2D18
1M99
5U09
7U0D
7U0H
2U01
2D31
Position UL logo
2D15
7P16
2U00
6U09
5U05
2D19
1D38
1735
5D01
2D11
1M96
7P15
1M97

3104 313 6343.2

18310_554_0900309.eps
090309

Layout Small Signal Board (Bottom Side)


7E02
7E17
1F03
7F07
7FH0
2C29
1CD0
2C00
2C59
7CD0
7CG0
2FHT
7HF1
2HHB
2HHK
7T56
7T55
7T50
7T54
7T10
7HC3
7H02
SPI-PROG
7A02
6A01
7A00
2HHN
2HVZ
2HVY
7H06
2A00
7A01
2U16
2U17
2P30
7P11
7P01
7N13
7N11
7N10
7N12
1N02
3P17
7U03
7D10
7U01
1P00
A-side

3104 313 6343.2

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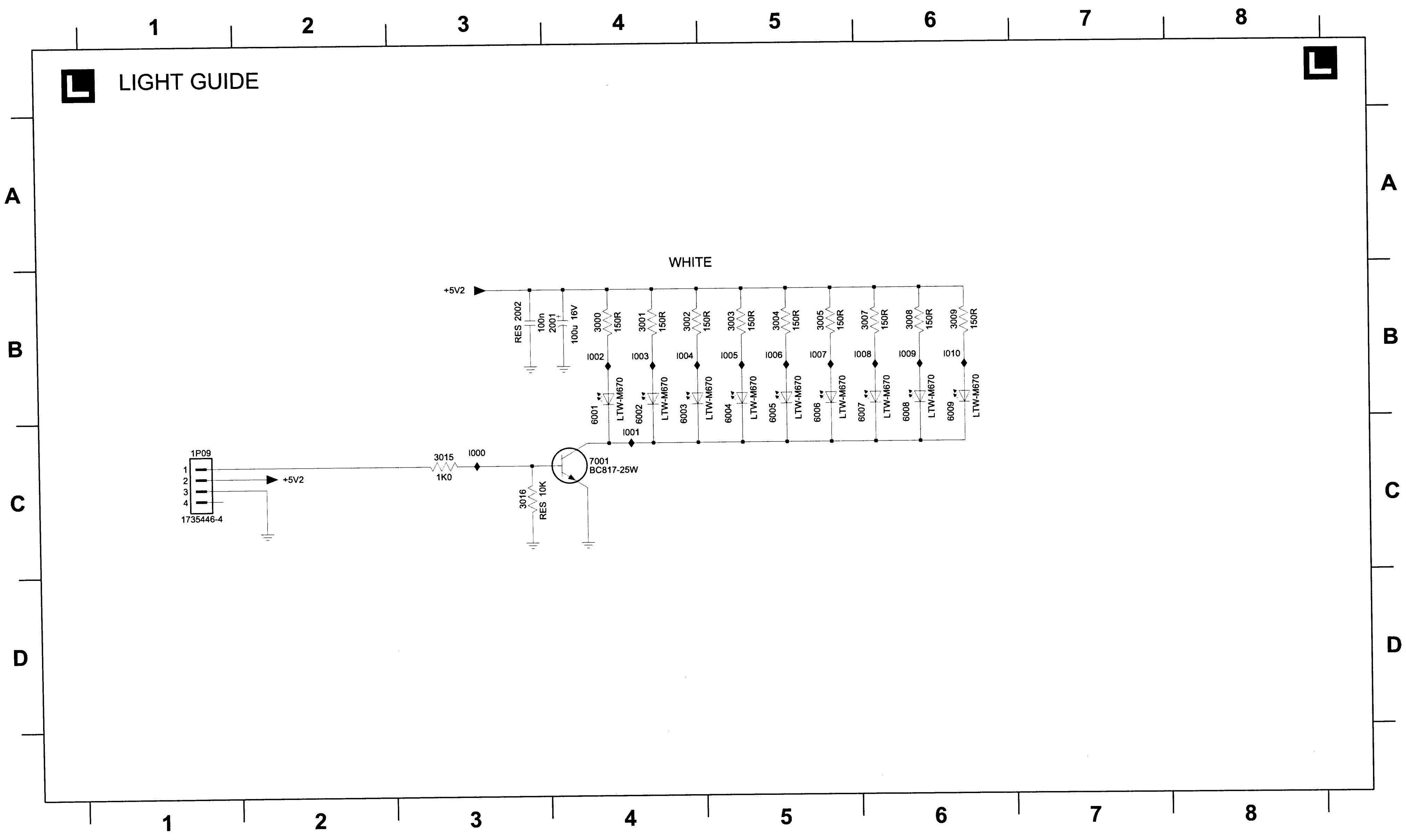
090309

2009-May-08

Light guide


L
LIGHT GUIDE
WHITE
+5V2
RES 2002
100n
2001
100u 16V
3000 150R
3001 150R
3002 150R
3003 150R
3004 150R
3005 150R
3007 150R
3008 150R
3009 150R
I002
I003
I004
I005
I006
I007
I008
I009
I010
6001 LTW-M670
6002 LTW-M670
6003 LTW-M670
6004 LTW-M670
6005 LTW-M670
6006 LTW-M670
6007 LTW-M670
6008 LTW-M670
6009 LTW-M670
I001
1P09
1
2
3
4
1735446-4
+5V2
3015
1K0
I000
3016
RES 10K
7001
BC817-25W

1P09	C1
2001	B4
2002	B3
3000	B4
3001	B4
3002	B4
3003	B5
3004	B5
3005	B5
3007	B6
3008	B6
3009	B6
3015	C3
3016	C3
6001	B4
6002	B4
6003	B4
6004	B5
6005	B5
6006	B5
6007	B6
6008	B6
6009	B6
7001	C4
I000	C3
I001	C4
I002	B4
I003	B4
I004	B4
I005	B5
I006	B5
I007	B5
I008	B6
I009	B6
I010	B6

CHN
SETNAME 2K9
CLASS_NO
LIGHT STRIP PANEL
9 LEDS 2K9
2008-10-17 3
3104 313 6344
1 2008-10-16
NAME Luc Buffel
SUPERS. 1
130 – 1
A3
CHECK
DATE

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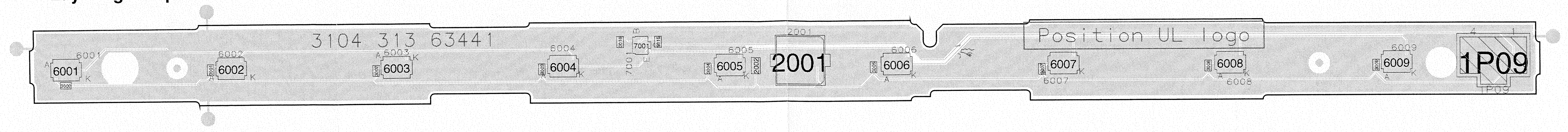
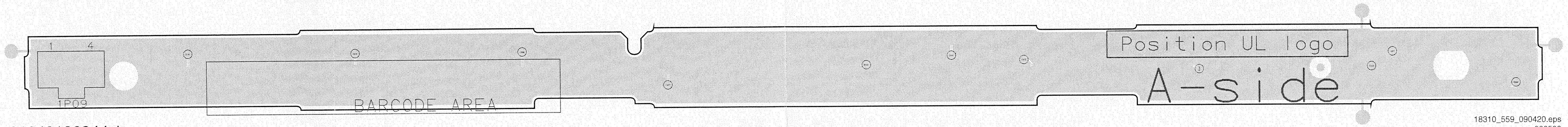
090508

Layout guide panel


3104 313 63441
6001
6002
6003
6004
7001
6005
2001
6006
Position UL logo
6007
6008
6009
1P09
A
K


1
4
1P09
BARCODE AREA
Position UL logo
A-side

31043136344.1

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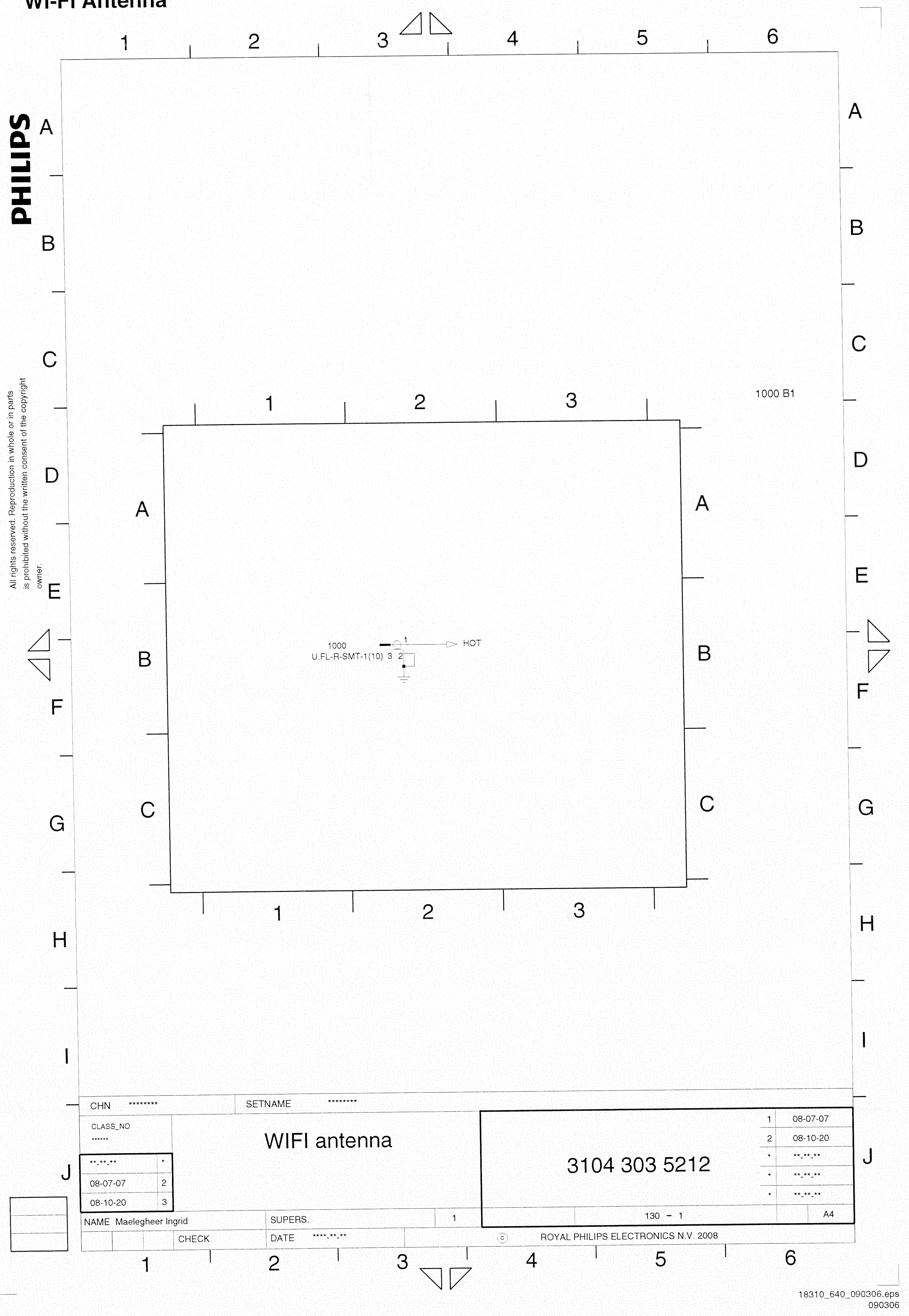
Wi-Fi Antenna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1000 B1
1000
U.FL-R-SMT-1(10)
1
2
3
HOT
CHN
SETNAME
CLASS_NO
WIFI antenna
3104 303 5212
08-07-07
08-10-20
NAME Maelegheer Ingrid
CHECK
SUPERS.
DATE
130 - 1
A4
ROYAL PHILIPS ELECTRONICS N.V. 2008

18310_640_090306.eps
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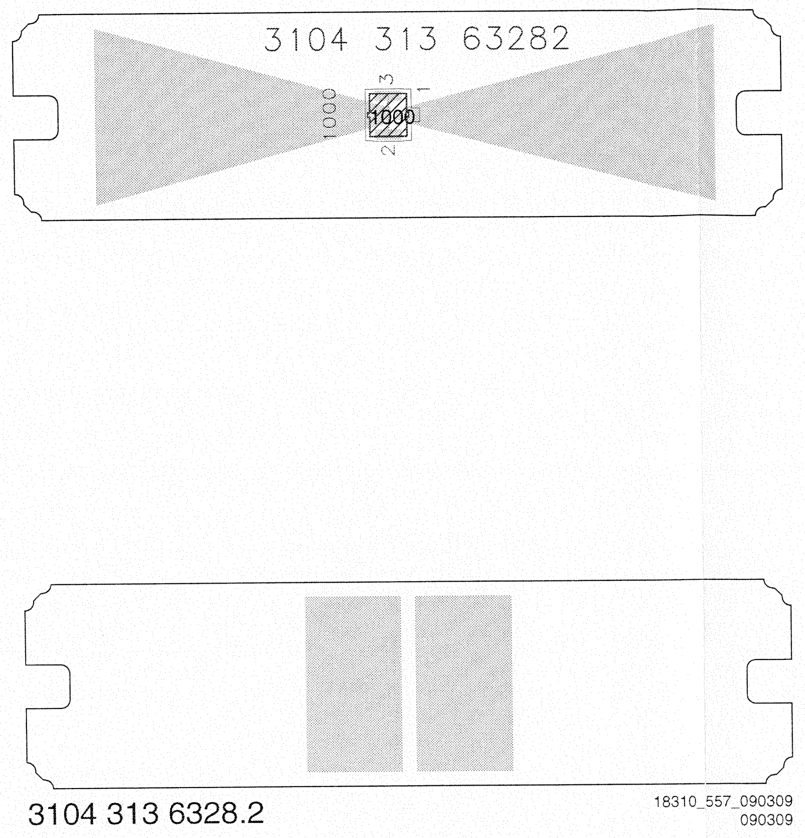
Layout Wi-Fi Antenna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3104 313 6328.2

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